Darlington Complementary Silicon Power Transistors

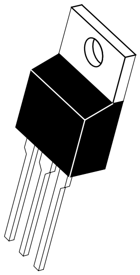
. . . designed for general purpose and low speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (typ.) at I_C = 4.0
- Collector–Emitter Sustaining Voltage at 100 mAdc
  $V_{CEO(sus)}$ = 80 Vdc (min.) — BDX33B, 34B
  100 Vdc (min.) — BDX33C, 34C
- Low Collector–Emitter Saturation Voltage
  $V_{CE(sat)}$ = 2.5 Vdc (max.) at I_C = 3.0 Adc — BDX33B, 33C/34B, 34C
- Monolithic Construction with Build–In Base–Emitter Shunt resistors
- TO–220AB Compact Package

NPN
BDX33B
BDX33C*
PNP
BDX34B
BDX34C*

*ON Semiconductor Preferred Device

DARLINGTON
10 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80–100 VOLTS
70 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BDX33B BDX34B	BDX33C BDX34C	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	10 15		Adc
Base Current	I_B	0.25		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	70 0.56		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.78	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

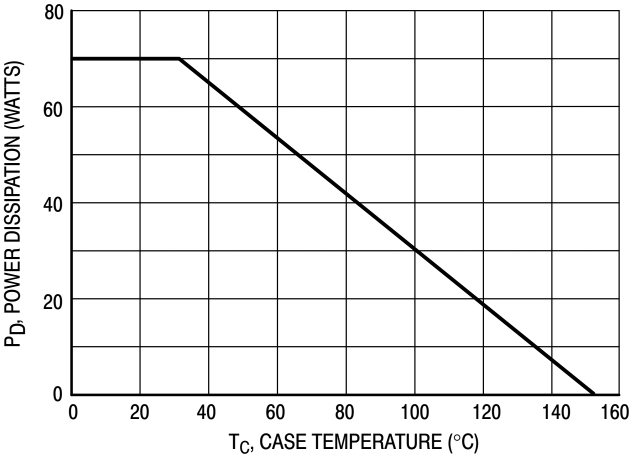


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0)		$V_{CEO(sus)}$			Vdc
	BDX33B/BDX34B		80	—	
	BDX33C/BDX34C		100	—	
Collector–Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0, R_{BE} = 100)		$V_{CER(sus)}$			Vdc
	BDX33B/BDX34B		80	—	
	BDX33C/BDX33C		100	—	
Collector–Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0, V_{BE} = 1.5 Vdc)		$V_{CEX(sus)}$			Vdc
	BDX33B/BDX34B		80	—	
	BDX33C/BDX34C		100	—	
Collector Cutoff Current (V_{CE} = 1/2 rated V_{CEO}, I_B = 0)		I_{CEO}			mAdc
	T_C = 25°C		—	0.5	
	T_C = 100°C		—	10	
Collector Cutoff Current (V_{CB} = rated V_{CBO}, I_E = 0)		I_{CBO}			mAdc
	T_C = 25°C		—	1.0	
	T_C = 100°C		—	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain[1] (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	BDX33B, 33C/34B, 34C	h_{FE}	750	—	—
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 6.0 mAdc)	BDX33B, 33C/34B, 34C	$V_{CE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	BDX33B, 33C/34B, 34C	$V_{BE(on)}$	—	2.5	Vdc
Diode Forward Voltage (I_C = 8.0 Adc)		V_F	—	4.0	Vdc

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

[2] Pulse Test non repetitive: Pulse Width = 0.25 s.

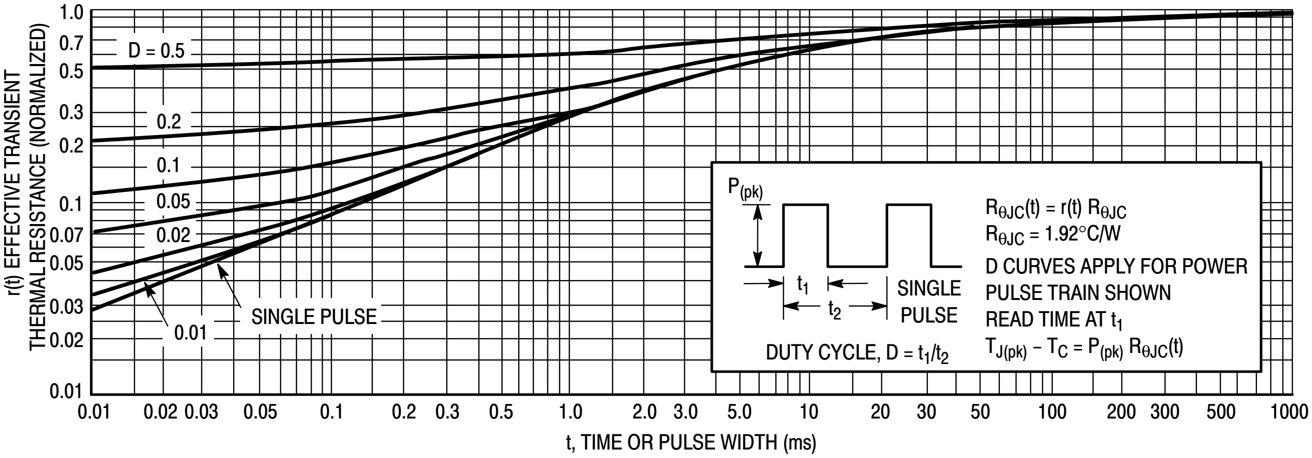


Figure 1. Thermal Response

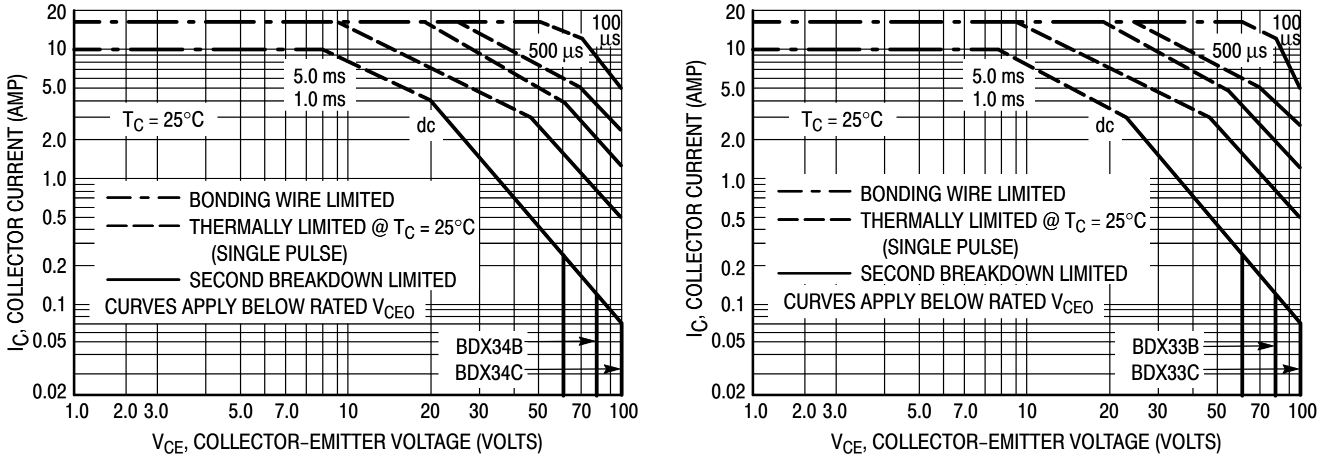


Figure 2. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Fig. 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ = 150°C. $T_{J(pk)}$ may be calculated from the data in Fig. . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

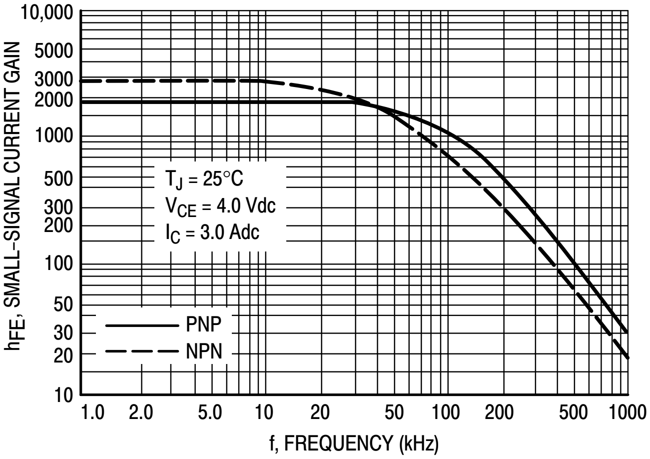


Figure 3. Small–Signal Current Gain

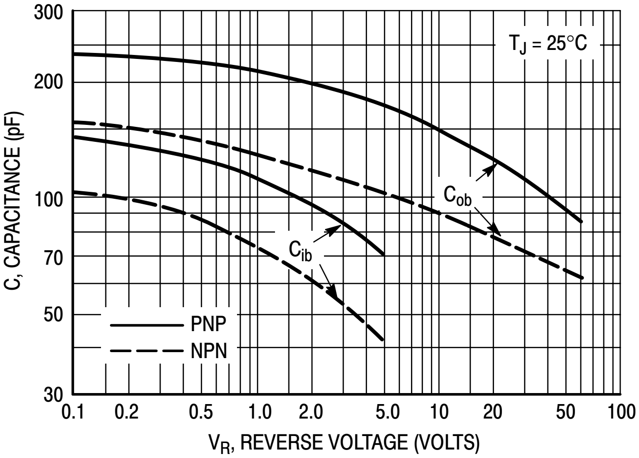


Figure 4. Capacitance

NPN
BDX33B, 33C

PNP
BDX34B, 34C

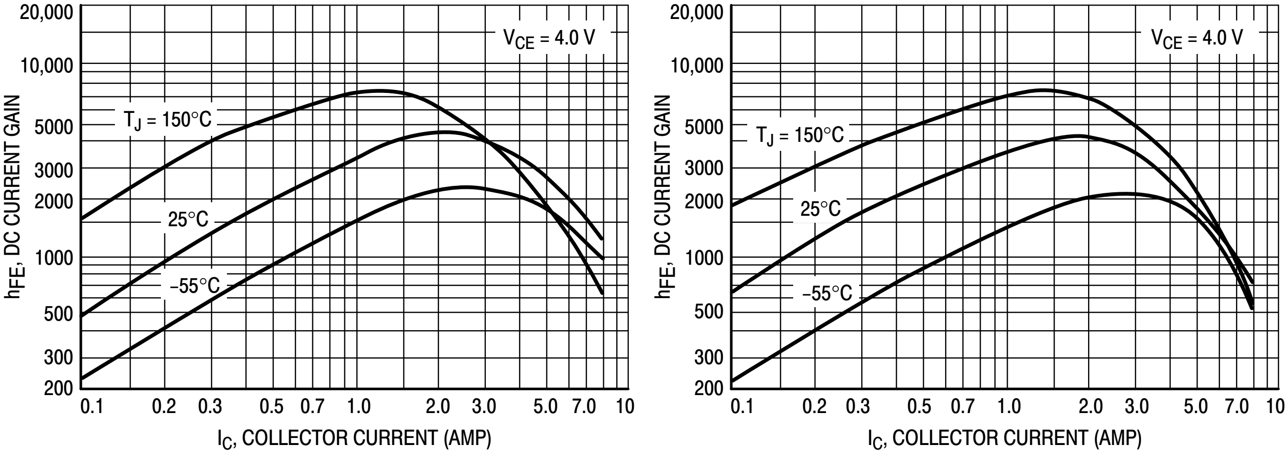


Figure 5. DC Current Gain

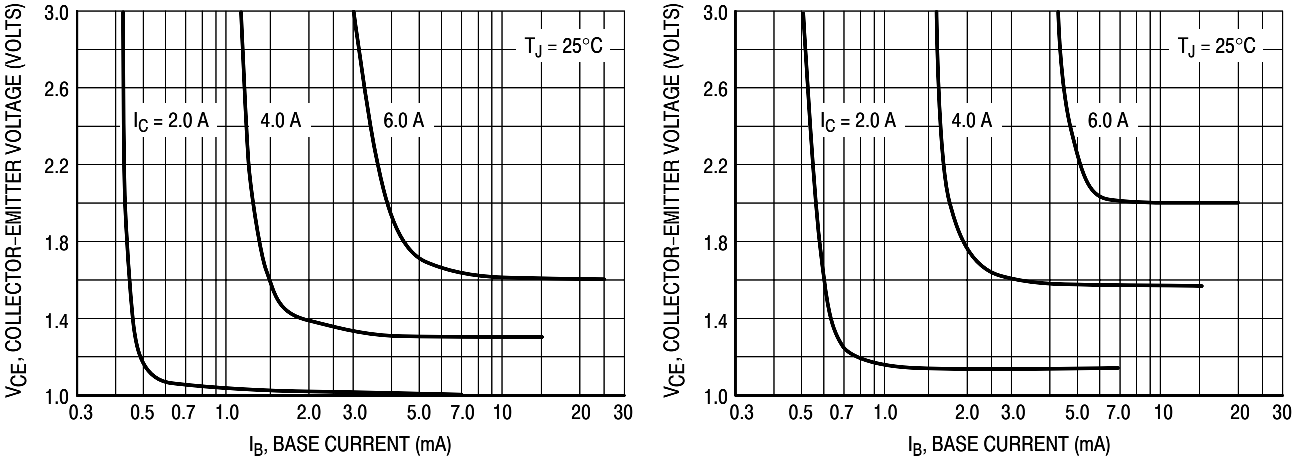


Figure 6. Collector Saturation Region

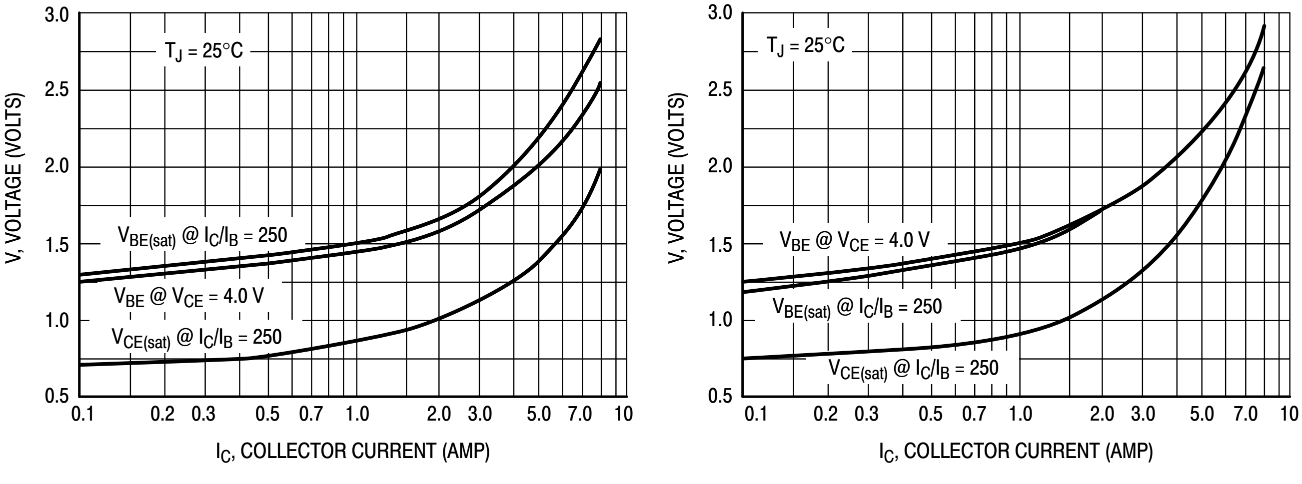
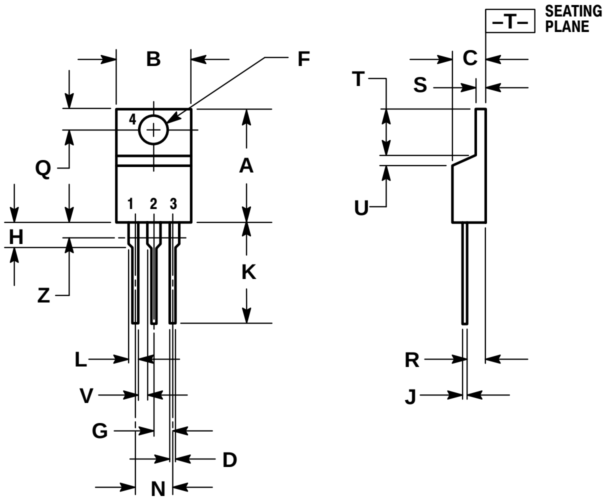


Figure 7. “On” Voltages

PACKAGE DIMENSIONS

CASE 221A–06
TO–220AB
ISSUE Y



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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