

## FEATURES

- Standard 8-Pin Packages
- High Power Factor Over Wide Load Range with Line Current Averaging
- International Operation Without Switches
- Instantaneous Overvoltage Protection
- Minimal Line Current Dead Zone
- Typical 250µA Start-Up Supply Current
- Rejects Line Switching Noise
- Synchronization Capability
- Low Quiescent Current: 9mA
- Fast 1.5A Peak Current Gate Driver

# **APPLICATIONS**

- Universal Power Factor Corrected Power Supplies
- Preregulators up to 1500W

## DESCRIPTION

The 8-pin LT1249 provides active power factor correction for universal off-line power systems with very few external parts. By using fixed high frequency PWM current averaging without the need for slope compensation, the LT1249 achieves far lower line current distortion, with a smaller magnetic element than systems that use either peak current detection or zero current switching approach, in both continuous and discontinuous modes of operation.

Power Factor Controller

The LT1249 uses a multiplier that has a square gain function from the voltage amplifier to reduce the AC gain at light output load and thus maintains low line current distortion and high system stability. The LT1249 also provides filtering capability to reject line switching noise which can cause instability when fed into the multiplier. Line current dead zone is minimized with low bias voltage at the current input to the multiplier.

The LT1249 provides many protection features including peak current limiting and overvoltage protection. The switching frequency is internally set at 100kHz.

While the LT1249 simplifies PFC design with minimal parts count, the LT1248 provides flexibilities in switching frequency, overvoltage, and current limit.

# **BLOCK DIAGRAM**



# **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	27V
GTDR Current Continuous	0.5A
GTDR Output Energy(Per Cycle)	
I <sub>AC</sub> Input Current	20mA
V <sub>SENSE</sub> Input Voltage	V <sub>MAX</sub>
M <sub>OUT</sub> Input Current	±5mA
<b>Operating Junction Temperature Range</b>	!
LT1249C	0°C to 100°C
LT1249I	-40°C to 125°C
Thermal Resistance (Junction-to-Ambie	ent)
N Package	100°C/W
S Package	120°C/W
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

# PACKAGE/ORDER INFORMATION



Consult factory for Military grade parts.

# **ELECTRICAL CHARACTERISTICS**

Maximum operating voltage ( $V_{MAX}$ ) = 25V,  $V_{CC}$  = 18V,  $I_{AC}$  = 100 $\mu$ A,  $CA_{OUT}$  = 3.5V,  $VA_{OUT}$  = 5V, no load on any outputs, unless otherwise noted.

PARAMETER	CONDITIONS		ТҮР	MAX	UNITS
Overall	ł				
Supply Current (V <sub>CC</sub> in Undervoltage Lockout)	V <sub>CC</sub> = Lockout Voltage – 0.2V	•	0.25	0.45	mA
Supply Current, On	$11.5V \le V_{CC} \le V_{MAX}$	•	8	12	mA
V <sub>CC</sub> Turn-On Threshold		• 15.5	16.5	17.5	V
V <sub>CC</sub> Turn-Off Threshold		• 9.5	10.5	11.5	V
Voltage Amplifier					
V <sub>SENSE</sub> Bias Current	V <sub>SENSE</sub> = 0V to 7V	•	-25	-250	nA
Voltage Amp Gain		70	100		dB
Voltage Amp Unity-Gain Bandwidth			1.5		MHz
Voltage Amp Output High	$0 \le Source Current \le 50\mu A$	• 10	12		V
Voltage Amp Output Low	$0 \le Sink Current \le 5\mu A$	•	0.1	0.4	V
Voltage Amp Source Current		• 130	260	450	μA
Voltage Amp Sink Current Threshold	Linear Operation, 2V < VA <sub>OUT</sub> < 10V	• 33	44	57	μA
Voltage Amp Sink Current Hysteresis	2V < VA <sub>OUT</sub> < 10V	• 14	22.5	30	μA
Current Amplifier		I.			
Current Amp Offset Voltage		•	±2	±15	mV
Current Amp Transconductance	$\Delta I_{CAOUT} = \pm 40 \mu A$	• 150	320	550	μmho
Current Amp Voltage Gain	$2.5V \le V_{CAOUT} \le 7.5V$	500	1000		V/V
Current Amp Source Current	$V_{MOUT} = 1V, I_M = 0\mu V$	100	145	220	μA
Current Amp Sink Current	$V_{MOUT} = -0.3V$ , $I_M = 0\mu A$	67	95	125	μA
Current Amp Output High		7.4	8.1		V
Current Amp Output Low			1.2	2	V



# **ELECTRICAL CHARACTERISTICS**

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PARAMETER	CONDITIONS		MIN	ТҮР	MAX	UNITS
Reference			•			
Reference Output Voltage	T <sub>A</sub> = 25°C, Measured at V <sub>SENSE</sub> Pin		7.39	7.5	7.6	V
Reference Output Voltage Worst Case	All Line, Temperature	•	7.32	7.5	7.68	V
Reference Output Voltage Line Regulation	V <sub>LOCKOUT</sub> < V <sub>CC</sub> < V <sub>MAX</sub>	•	-20	5	20	mV
Multiplier						
Multiplier Output Current	I <sub>AC</sub> = 100μA, VA <sub>OUT</sub> = 5V			35		μA
Multiplier Output Current Offset	$R_{AC}$ = 1M from $I_{AC}$ to GND	•		-0.05	-0.5	μA
Multiplier Max Output Current (I <sub>M(MAX)</sub> )	I <sub>AC</sub> = 450µA, VA <sub>OUT</sub> = 7V (Note 1)	•	- 375	-250	-150	μA
Multiplier Max Output Voltage $(I_{M(MAX)} \times R_{MOUT})$	I <sub>AC</sub> = 450µA, VA <sub>OUT</sub> = 7V (Note 1)	•	-1.25	-1.1	-0.96	V
Multiplier Gain Constant (Note 2)				0.035		V <sup>-2</sup>
I <sub>AC</sub> Input Resistance	I <sub>AC</sub> from 50μA to 1mA		15	25	35	kΩ
Oscillator						
Oscillator Frequency		•	75	100	125	kHz
Control Pin (CA <sub>OUT</sub> ) Threshold	Duty Cycle = 0	•	1.3	1.8	2.3	V
Synchronization Frequency Range	Synchronizing Pulse Low $\leq$ 0.35V on CA <sub>OUT</sub>	•	127		160	kHz
Gate Driver						
Max GTDR Output Voltage	0mA Load, 18V < V <sub>CC</sub> < V <sub>MAX</sub> (Note 3)	•	12	15	17.5	V
GTDR Output High	$-200$ mA Load, $11.5V \le V_{CC} \le 15V$	•	V <sub>CC</sub> - 3.0			V
GTDR Output Low (Device Unpowered)	V <sub>CC</sub> = 0V, 50mA Load (Sinking)	•		0.9	1.5	V
GTDR Output Low (Device Active)	200mA Load (Sinking)	•		0.5	1	V
Peak GTDR Current	10nF from GTDR to GND			2		A
GTDR Rise and Fall Time	1nF from GTDR to GND			25		ns
GTDR Max Duty Cycle			90	96		%

The  $\bullet$  denotes specifications which apply over the operating temperature range.

Note 1: Current amplifier is in linear mode with OV input common mode.

**Note 2:** Multiplier Gain Constant:  $K = \frac{I_M}{I_{AC} (VA_{OUT} - 1.5)^2}$ 

Note 3: Maximum GTDR output voltage is internally clamped for higher V<sub>CC</sub> voltages.

# **TYPICAL PERFORMANCE CHARACTERISTICS**



Transconductance of **Current Amplifier** 400 20 350 0 gm TRANSCONDUCTANCE (µmho) 300 -20 250 -40 PHASE ( 200 -80 (DEG) 150 100 -100 50 -120 0 -140 1k 10k 100k 1M 10M

FREQUENCY (Hz)

1249 G02

# TYPICAL PERFORMANCE CHARACTERISTICS





Supply Current vs Supply Voltage



**GTDR Source Current** 



**GTDR Sink Current** 







Start-Up Supply Current vs Supply Voltage



Switching Frequency





# **TYPICAL PERFORMANCE CHARACTERISTICS**



# PIN FUNCTIONS

GND (Pin 1): Ground.

**CA<sub>OUT</sub> (Pin 2):** This is the output of the current amplifier that senses and forces the line current to follow the reference signal that comes from the multiplier by commanding the pulse width modulator. When  $CA_{OUT}$  is low, the modulator has zero duty cycle.

 $M_{OUT}$  (Pin 3): The multiplier current goes out of this pin through the 4k resistor  $R_{MOUT}$ . The voltage developed across  $R_{MOUT}$  is the reference voltage of the current loop and it is limited to 1.1V. The noninverting input of the current amplifier is also tied to  $R_{MOUT}$ . In operation,  $M_{OUT}$ 

is normally at negative potential and only AC signals appear at the noninverting input of the current amplifier.

 $I_{AC}$  (Pin 4): This is the AC line voltage sensing input to the multiplier. It is a current input that is biased at 2V to minimize the crossover dead zone caused by low line voltage. A 25k resistor is in series with the current input, so that a small external capacitor can be used to filter out the switching noise from the high impedance lines.

**VA<sub>OUT</sub> (Pin 5):** This is the output of the voltage error amplifier. The output is clamped at 12V. When the output goes below 1.5V, the multiplier output current is zero.



# PIN FUNCTIONS

 $V_{\mbox{SENSE}}$  (Pin 6): This is the inverting input to the voltage amplifier.

**GTDR (Pin 7):** The MOSFET gate driver is a 1.5A fast totem pole output. It is clamped at 15V. Capacitive loads like MOSFET gates may cause overshoot. A gate series resistor of at least  $5\Omega$  will prevent the overshoot.

 $V_{CC}$  (Pin 8): This is the supply of the chip. The LT1249 has a very fast gate driver required to fast charge high power MOSFET gate capacitance. High current spikes occur during charging. For good supply bypass, a 0.1 µF ceramic capacitor in parallel with a low ESR electrolytic capacitor, 56µF or higher is required in close proximity to IC GND.

# **APPLICATIONS INFORMATION**

## **Error Amplifier**

The error amplifier has a 100dB DC gain and 1.5MHz unitygain frequency. It is internally clamped at 12V. The noninverting input is tied to the 7.5V reference.

## **Current Amplifier**

The multiplier output current  $I_M$  flows out of the  $M_{OUT}$  pin through the 4k resistor  $R_{MOUT}$  and develops the reference signal to the current loop that is controlled by the current amplifier. Current gain is the ratio of R<sub>MOUT</sub> to line current sense resistor. The current amplifier is a transconductance amplifier. Typical  $g_m$  is 320 $\mu$ mho and gain is 60dB with no load. The inverting input is internally tied to GND. The noninverting input is tied to the multiplier output. The output is internally clamped at 8V. Output resistance is about 4M; DC loading should be avoided because it will lower the gain and introduce offset voltage at the inputs which becomes a false reference signal to the current loop and can distort line current. Note that in the current averaging operation, high gain at twice the line frequency is necessary to minimize line current distortion. Because CA<sub>OUT</sub> may need to swing 5V over one line cycle at high line condition, 11mV will be present at the inputs of the current amplifier if gain is rolled off to 450 at 120Hz (1nF in series with 10k at CA<sub>OUT</sub>). At light load, when  $(I_M)(R_{MOUT})$  can be less than 100mV, lower gain will distort the current loop reference signal and line current. If signal gain at the 100kHz switching frequency is too high, the system behaves more like a current mode system and can cause subharmonic oscillation. Therefore, the current amplifier should be compensated to have a gain of less than 15 at 100kHz and more than 300 at 120Hz.

## Multiplier

The multiplier is a current multiplier with high noise immunity in a high power switching environment. The current gain is:

$$I_{M}$$
 = ( $I_{AC} \times I_{EA}{}^{2})/(200 \mu A)^{2}$ , and  $I_{EA}$  = (VA\_{OUT} - 1.5V)/25k

With a square function, because of the lower gain at light power load, system stability is maintained and line current distortion caused by the AC ripple fed back to the error amplifier is minimized. Note that switching ripple on the high impedance lines could get into the multiplier from the  $I_{AC}$  pin and cause instability. The LT1249 provides an internal 25k resistor in series with the low impedance multiplier current input so that only a capacitor from the  $I_{AC}$  pin to GND is needed to filter out the noise. Maximum multiplier output current is limited to 250µA. Figure 1 shows the multiplier transfer curves.



Figure 1. Multiplier Current  $I_{M}$  vs  $I_{AC}$  and  $VA_{OUT}$ 



## **APPLICATIONS INFORMATION**

### Line Current Limiting

Maximum voltage across  $\mathsf{R}_{MOUT}$  is internally limited to 1.1V. Therefore, line current limit is 1.1V divided by the sense resistor  $\mathsf{R}_S.$  With a 0.2 $\Omega$  sense resistor  $\mathsf{R}_S$  line current limit is 5.5A. As a general rule,  $\mathsf{R}_S$  is chosen according to:

 $R_{S} = \frac{I_{M(MAX)} \times R_{MOUT} \times V_{LINE(MIN)}}{K(1.414)P_{OUT(MAX)}}$ 

where  $P_{OUT(MAX)}$  is the maximum power output and K is usually between 1.1 and 1.3 depending on efficiency and resistor tolerance. When the output is overloaded and line current reaches limit, output voltage  $V_{OUT}$  will drop to keep line current constant. System stability is still maintained by the current loop which is controlled by the current amplifier. Further load current increase results in further  $V_{OUT}$  drop and clipping of the line current, which degrades power factor.

### Synchronization

The LT1249 can be externally synchronized in a frequency range of 127kHz to 160kHz. Figure 2 shows the synchronizing circuit. Synchronizing occurs when  $CA_{OUT}$  pin is pulled below 0.5V with an external transistor and a Schottky diode. The Schottky diode and the 10k pull-up resistor are necessary for the required fast slewing back up to the normal operating voltage on  $CA_{OUT}$  after the transistor is turned off. Positive slewing on  $CA_{OUT}$  should be faster than the oscillator ramp rate of 0.5V/µs.

The width of the synchronizing pulse should be under 60ns. The synchronizing pulses introduce an offset voltage on the current amplifier inputs, according to:

$$\Delta V_{\text{OS}} = \frac{(\text{ts})(\text{fs})\left(I_{\text{C}} + \frac{V_{\text{C}} - 0.5}{\text{R2}}\right)}{g_{\text{m}}}$$

ts = pulse width

fs = pulse frequency

 $I_{C} = CA_{OUT}$  source current ( $\approx 150\mu A$ )

$$V_{\rm C} = CA_{\rm OUT}$$
 operating voltage (1.8V to 6.8V)

R2 = resistor for the mid-frequency "zero" in the current loop  $g_m$  = current amplifier transconductance ( $\approx 320 \mu mho$ )

With ts = 30ns, fs = 130kHz,  $V_C$  = 3V, and R2 = 10k, offset voltage shift is  $\approx$ 5mV. Note that this offset voltage will add slight distortion to line current at light load.



Figure 2. Synchronizing the LT1249

### **Overvoltage Protection**

In Figure 3, R1 and R2 set the regulator output DC level:  $V_{OUT} = V_{REF}[(R1 + R2)/R2]$ . With R1 = 1M, R2 = 20k,  $V_{OUT}$  is 382V.

Because of the slow loop response necessary for power factor correction, output overshoot can occur with sudden load removal or reduction. To protect the power components and output load, the LT1249 voltage error amplifier senses the output voltage and quickly shuts off the current switch when overvoltage occurs. When overshoot occurs on V<sub>OUT</sub>, the overcurrent from R1 will go through VA<sub>OUT</sub> because amplifier feedback keeps V<sub>SENSE</sub> locked at 7.5V. When this overcurrent reaches 44µA amplifier sinking limit, the amplifier loses feedback and its output snaps low to turn the multiplier off.

Overvoltage trip level:  $\Delta V_{OUT} = 44 \mu A \times R1$ 



Figure 3. Overvoltage Protection



# **APPLICATIONS INFORMATION**

The Figure 3 circuit therefore has 382V on V<sub>OUT</sub>, and an overvoltage level = (V<sub>OUT</sub> + 44V), or 426V. With a 22 $\mu$ A hysteresis, V<sub>OUT</sub> then has to drop 22V to 404V before feedback recovers and the switch turns back on.

M<sub>OUT</sub> is a high impedance current output. In the current loop, offset line current is determined by multiplier offset current and input offset voltage of the current amplifier. A negative 4mV current amplifier  $V_{OS}$  translates into 20mA line current and 5W input power for 250V line if  $0.2\Omega$  sense resistor is used. Under no load or when the load power is less than this offset input power,  $V_{OUT}$  would slowly charge up to an overvoltage state because the overvoltage comparator can only reduce multiplier output current to zero. This does not guarantee zero output current if the current amplifier has offset. To regulate  $V_{OUT}$ under this condition, the amplifier M1 (see Block Diagram), becomes active in the current loop when VAOUT goes down to 1V. The M1 can put out up to 15µA to the 4k resistor at the inverting input to cancel the current amplifier negative  $V_{OS}$  and keep  $V_{OUT}$  error to within 2V.

### **Undervoltage Lockout**

The LT1249 turns on when  $V_{CC}$  is higher than 16V and remains on until  $V_{CC}$  falls below 10V, whereupon the chip enters the lockout state. In the lockout state, the LT1249 only draws 250µA, the oscillator is off, the  $V_{REF}$  and the GTDR pins remain low to keep the power MOSFET off.

## Start-Up and Supply Voltage

The LT1249 draws only 250 $\mu$ A before the chip starts at 16V on V<sub>CC</sub>. To trickle start, a 90k resistor from the power line to V<sub>CC</sub> supplies the trickle current and C4 holds the V<sub>CC</sub> up while switching starts (see Figure 4). Then the auxiliary winding takes over and supplies the operating current. Note that D3 and the large value C3, in both Figures 4 and 5, are only necessary for systems that have sudden large load variation down to minimum load and/or very light load conditions. Under these conditions, the loop may exhibit a start/restart mode because switching remains off long enough for C4 to discharge below 10V. The C3 will hold V<sub>CC</sub> up until switching resumes. For less severe load variations, D3 is replaced with a short and C3 is omitted. The turns ratio between the primary winding and the







Figure 5. Power Supply for LT1249

auxiliary winding determines V<sub>CC</sub> according to: V<sub>OUT</sub>/(V<sub>CC</sub> - 2V) = N<sub>P</sub>/N<sub>S</sub>. For 382V V<sub>OUT</sub> and 18V V<sub>CC</sub>, N<sub>P</sub>/N<sub>S</sub>  $\approx$  19.

In Figure 5 a new technique for supply voltage eliminates the need for an extra inductor winding. It uses capacitor charge transfer to generate a constant current source which feeds a Zener diode. Current to the Zener is equal to  $(V_{OUT} - V_Z)(C)(f)$ , where  $V_Z$  is Zener voltage and f is switching frequency. For  $V_{OUT} = 382V$ ,  $V_Z = 18V$ , C = 1000pF, and f = 100kHz, Zener current will be 36mA. This is enough to operate the LT1249, including the FET gate drive.

## **Output Capacitor**

The peak-to-peak 120Hz output ripple is determined by:

 $V_{P-P} = (2)(I_{LOAD}DC)(Z)$ 

where I<sub>LOAD</sub>DC: DC load current Z: capacitor impedance at 120Hz

For  $180\mu$ F at 300W load,  $I_{1 OAD}DC = 300W/385V = 0.78A$ ,



## **APPLICATIONS INFORMATION**

 $V_{P-P}$  = 2  $\times$  0.78A  $\times$  7.4 $\Omega$  = 11.5V. If less ripple is desired, higher capacitance should be used.

The selection of the output capacitor should also be based on the operating ripple current through the capacitor.

The ripple current can be divided into three major components. The first is at 120Hz whose RMS value is related to the DC load current as follows:

 $I_{1RMS}\approx 0.71\times I_{LOAD}DC$ 

The second component contains the PF switching frequency ripple current and its harmonics. Analysis of this ripple is complicated because it is modulated with a 120Hz signal. However, computer numerical integration and Fourier analysis approximate the RMS value reasonably close to the bench measurements. The RMS value is about 0.82A at a typical condition of 120VAC, 200W load. This ripple is line voltage dependent, and the worst case is at low line.

I<sub>2RMS</sub> = 0.82A at 120VAC, 200W

The third component is the switching ripple from the load, if the load is a switching regulator.

 $I_{3RMS} \approx I_{LOAD}DC$ 

For United Chemicon KMH 400V capacitor series, ripple current multiplier for currents at 100kHz is 1.43. The equivalent 120Hz ripple current can then be found:

$$I_{RMS} = \sqrt{\left(I_{1RMS}\right)^2 + \left(\frac{I_{2RMS}}{1.43}\right)^2 + \left(\frac{I_{3RMS}}{1.43}\right)^2}$$

For a typical system that runs at an average load of 200W and 385V output:

$$\begin{split} I_{LOAD}DC &= 0.52A\\ I_{1RMS} \approx 0.71 \times 0.52A &= 0.37A\\ I_{2RMS} \approx 0.82A \text{ at } 120VAC\\ I_{3RMS} \approx I_{LOAD}DC &= 0.52A \end{split}$$

$$H_{\rm RMS} = \sqrt{\left(0.37A\right)^2 + \left(\frac{0.82A}{1.43}\right)^2 + \left(\frac{0.52A}{1.43}\right)^2} = 0.77A$$

The 120Hz ripple current rating at  $105^{\circ}$ C ambient is 0.95A for the  $180\mu$ F KMH 400V capacitor. The expected life of the output capacitor may be calculated from the thermal stress analysis:

$$L = L_0 \times 2 \frac{(105^{\circ}C + \Delta T_K) - (T_{AMB} + \Delta T_0)}{10}$$

where

L = expected life time

 $L_0$  = hours of load life at rated ripple current and rated ambient temperature

 $\Delta T_{K}$  = capacitor internal temperature rise at rated condition.  $\Delta T_{K}$  = (I<sup>2</sup>R)/(KA), where I is the rated current, R is capacitor ESR, and KA is a volume constant.

T<sub>AMB</sub> = operating ambient temperature

 $\Delta T_0$  = capacitor internal temperature rise at operating condition

In our example,  $L_0$  = 2000 hours and  $\Delta T_K$  = 10°C at rated 0.95A.  $\Delta T_0$  can then be calculated from:

$$\Delta T_0 = \left(\frac{I_{\text{RMS}}}{0.95\text{A}}\right)^2 \times \Delta T_{\text{K}} = \left(\frac{0.77\text{A}}{0.95\text{A}}\right)^2 \times 10^{\circ}\text{C} = 6.6^{\circ}\text{C}$$

Assuming the operating ambient temperature is 60°C, the approximate life time is:

$$L_0 \approx 2000 \times 2 \frac{(105^{\circ}C + 10^{\circ}C) - (60^{\circ}C + 6.6^{\circ}C)}{10} \approx 57,000$$
 Hrs.

For longer life, capacitor with higher ripple current rating or parallel capacitors should be used.



# TYPICAL APPLICATION



### 300W, 382V Preregulator

\*\* THIS SCHOTTKY DIODE IS TO CLAMP GTDR WHEN MOS SWITCH TURNS OFF. PARASITIC INDUCTANCE AND GATE CAPACITANCE MAY TURN ON CHIP SUBSTRATE DIODE AND CAUSE ERRATIC OPERATIONS IF GTDR IS NOT CLAMPED.

 $\dagger$  SEE APPLICATIONS INFORMATION SECTION FOR CIRCUITRY TO SUPPLY POWER TO  $V_{CC}$ 

Kool  $M\mu$  is a registered trademark of Magnetics, Inc.



## PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

8-Lead Plastic DIP 0.400 (10.160) MAX 8 | 7 | 6 5 0.250 ± 0.010  $(6.350 \pm 0.254)$ ۷ 4 1 2 3  $0.130 \pm 0.005$ 0.300 - 0.320 0.045 - 0.065 > -(7.620 - 8.128) $(\overline{1.143} - 1.651)$  $(\overline{3.302 \pm 0.127})$ ᡟ  $\frac{0.065}{(1.651)}$ 4 0.009 - 0.015TYP

N8 Package



S8 Package 8-Lead Plastic SOIC



0.014 - 0.019

 $(\overline{0.355 - 0.483})$ 

0.050

(1.270)

BSC

SO8 0294

\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

0.406 - 1.270



Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

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