

Stamp9261

Technical Manual

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1. Introduction

The Stamp is intended to be used as a small size "intelligent" display module as well as a universal Linux CPU card. It can be used anywhere where restricted energy and space requirements play a role.

The Stamp9261 has all the necessary interfaces to support a huge variety of peripheral devices. Equipped with a 32-Bit parallel bus it gives fast access to a number of chips and additional devices.

The ARM architecture as a modern and widely supported processor architecture is currently the platform of choice for medium performance embedded devices. Almost all major processor manufacturers have ARM products in their portfolio.

The availability of the widespread operating system "Linux" for the ARM platform opens access to a broad range of software, including tools, drivers, and software libraries. Programs written for ARM can easily be cross-compiled for the PC platform for testing and debugging.

Examples of actual or potential applications are: terminals, measuring and test equipment, data-logging, as well as any simple or more complex control and automation tasks.

2. Scope

This document describes the most important hardware features of the SAM9261 Stamp9261. It includes all informations necessary to develop a customer specific hardware for the Stamp9261. The Operating System Linux is described in a further document.

The manual comprises only a brief description of the AT91SAM9261 processor, as this is already described in depth in the manual of the manufacturer Atmel (document 6062). Descriptions of the ARM core ARM926EJ-S are available from Atmel and also at <http://www.arm.org>. It is much recommended to have a look at these documents for a thorough understanding of the processor and its integrated peripherals.

3. Overview of Technical Characteristics

3.1. CPU

Atmel AT91SAM9261 Embedded Processor featuring an ARM926EJ-S™ ARM® Thumb® Core

- CPU clock 200+ MHz
- 16kB Instruction Cache
- 16kB Data Cache
- Memory Management Unit (MMU)
- 3.3V Supply Voltage, 1.2V Core Voltage

3.2. Memory

- 16 or 64 MB flash memory (optional 128 MB)
- 32MB or 64MB SDRAM
- 128 KB serial Dataflash
- 160 KB Fast SRAM
- 256 Bytes EEPROM

3.3. Interfaces and externals signals

- 2x 100-pin fine-pitch low-profile Connectors (Hirose FX8)
- Ethernet 10/100 Mbit MAC
- Dual USB 2.0 Full Speed (12 MBit/s) Hosts
- USB 2.0 Full Speed (12 MBit/s) Device
- 3 USARTs
- 1 UART
- 1 Synchronous Serial Controller (SSC, I²S)
- 2 Serial Peripheral Interfaces (SPI)
- 1 Two Wire Interface (TWI, I²C)
- 1 MultiMedia Card Interface
- JTAG debug port
- Digital Ports – up to 39 available
- Control Signals: IRQs, BMS, SHDN, WKUP
- 4 Programmable Clocks
- LCD/TFT-Controller up to 2048x2048 pixel, 24 Bit color depth
- 32-Bit parallel CPU-Bus

Some of the various functions are realized by multiplexing connector pins; therefore not all functions may be used at the same time (see table in chapter 11).

3.4. Miscellaneous

- Three 16-Bit Timer/Counter
- Real Time Timer (RTT), with battery backup support
- Periodic Interval Timer (PIT)
- Watchdog Timer (WDT)
- Unique Hardware Serial Number
- extended temperature range, -25°C ... +70°C

3.5. Power Supply

- 3.3V power supply
- 3V backup power supply, e.g. from a lithium battery

3.6. Dimensions

- Dimensions: 53x38x4 mm (WxDxH)

4. Hardware Description

4.1. Mechanics

The Stamp9261 was designed as a flexible CPU-Module, which can be connected to base boards via 2x 100-pin fine-pitch low profile Hirose FX8 connectors.

The size of the Stamp9261's PCB is only 53x38x4 mm fitting it in even the smallest design. While having implemented the sensible CPU, SDRAM and Flash design it still exports almost all possible CPU-Pins on it's connectors to allow a flexible design on base boards.

4.2. ARM926EJ-S™ Core

Here are some of the most important features of the SAM9261 core:

- up to 240 MHz CPU Clock
- 16 Kbyte Data Cache, 16 Kbyte Instruction Cache, Write Buffer
- 32 bit Data Bus
- Memory Management Unit
- ARM Thumb Instruction Format supported
- DSP Instruction Extensions
- ARM Jazelle® Technology for Java® Acceleration
- EmbeddedICE™ Debug Communication Channel Support
- Mid-level implementation Embedded Trace Macrocell (ETM)

Some of these features – like Jazelle – are currently not supported by the operating system of the Stamp9261.

4.3. Memory

a) Flash memory

- **Flash memory layout**

The Stamp9261 can be equipped with 16MB, 32MB, 64MB, 128MB Flash memory. This is organized in blocks of 128KB. Each block can be erased individually.

The flash memory is made up of 1 IC. In case that 128MB chips should be installed, the PIO line PC0 is used as A26, as the CPU has only 26 external address lines.

- **Limited number of erase cycles**

The Flash memory consists of "Large Sector Flash-ICs" (e.g. Spansion's S29GL256 or similar). Only a limited number of erase cycles per block are tolerable for these devices (usually one hundred thousand erase cycles are guaranteed by the manufacturer). This means that the flash memory, in particular the flash disk, is not suitable for permanent write operations of a program, since the permissible number of erase cycles per block might be exceeded in a relatively short time. A RAM disk must be used for such purposes.

b) Boot Mode Select Signal (BMS)

This pin is normally low and enables the standard boot code from the Stamp9261's flash memory. If pulled high, the Stamp9261 boots from the internal ROM of the SAM9261 processor. The ROM code initializes the CPU and tries to boot from an external DataFlash[®] memory. Currently, the Stamp9261 provides no support for using the ROM code. This ROM-boot program also supports the SAM-BA programming tool from Atmel[©]

c) EEPROM

256 Bytes within a serial EEPROM are available to store configuration data. The EEPROM is accessed via the TWI.

d) SDRAM

The Stamp9261 can be equipped with up to 64MB SDRAM. The starter-kit Stamp9261 is equipped with 64MB Mobile SDRAM.

e) SRAM

The SAM9261 processor integrates 160 KB of fast static RAM which can be used as "Tightly Coupled Memory" (TCM) with dedicated instruction and data blocks. Time-critical sections of the code, e.g. interrupt handlers, are recommended to be placed within the SRAM, as well as critical data sections like the stack.

f) DataFlash

A 128 KB Dataflash connected to the processor's SPI-Bus is provided. It can be used for booting purposes or storing configuration data in designs without further flash memory

4.4. Battery backup

The following parts of the SAM9261 Processor can be backed-up by a battery:

- the Slow Clock Oscillator;
- the Real Time Timer;
- the Reset Controller;
- the four General Purpose Backup Registers.

It is recommended to always use a backup power supply (normally a battery) in order to speed up the boot-up time and to avoid reset problems.

4.5. Reset Controller (RSTC)

The SAM9261 has an integrated Reset Controller which samples the backup and the core voltage (both typically at 1.2V). As the Stamp9261 uses an additional reset comparator to supervise the 3.3V supply, the user reset function of the RSTC should always be enabled. This requires the presence of a backup voltage (VDDBU) when the card is powered down.

4.6. Serial Number

Every Stamp9261 has a unique 48-bit hardware serial number chip which can be used by application software. A Linux driver for reading the serial number is available.

4.7. Clock Generator and Power Management Controller (PMC)

a) SAM9261 Clocks

The Stamp9261's SAM9261 Processor generates its necessary clocks based on two crystal oscillators:

- Slow Clock (SLCK) Oscillator, running at 32768 Hz,
- Main Clock Oscillator, running at 18.432 MHz.

From the Main Clock Oscillator, the Clock Generator produces two further clocks by using two PLLs:

- PLLA provides the 200 MHz Processor Clock (PCK) and the
- Master Clock (MCK) = $PCK/2 = 100$ MHz
- PLLB provides the 96 MHz USB Clock.

Apart from the USB Clock, most of the peripheral clocks are derived from MCK:

- SDRAM, LCDC, USART, SPI, TWI, SSC, PIT, TC.

The TC unit can also run on SLCK. The RTT always runs on SLCK.

b) Programmable Clocks

Four programmable clock outputs PCK0, PCK1, PCK2 and PCK3 are available on the connectors of the Stamp9261. They can individually be programmed to the SLCK, PLLA, PLLB, and Main Clock, as well as these values divided by 2, 4, 8, 16, 32, or 64.

c) PMC Control Functions

The PMC has a Peripheral Clock register which allows to enable or disable the clocks of all integrated peripherals individually using their "Peripheral Identifier" (see table Peripheral Identifiers).

The System Clock register allows to enable or disable each of the following clocks individually:

- Processor clock,
- LCD clock (HCK1)
- USB Host clock (common for both channels)
- USB Device clock
- Programmable Clocks

The HCK0 bit mentioned in the Atmel manual is not used in the SAM9261 processor.

d) PMC Supervisory Functions

The PMC provides status flags for the

- Main Oscillator
- Master Clock
- PLLA
- PLLB
- Programmable Clocks

The PMC status register provides "Clock Ready" or, respectively, "PLL Lock" status bits for each of these clocks. An interrupt is generated when any of these bits changes from 0 to 1.

The Main Oscillator frequency can be measured by using the PMC Main Clock Frequency register. The SLCK is used as reference for the measurement.

4.8. Real-time Timer (RTT)

The Real-time Timer is a 32-bit counter combined with a 16-bit prescaler running at Slow Clock (SLCK = 32768 Hz). As the RTT keeps running if only the backup supply voltage is available, it is used as a Real-time clock on the Stamp9261.

The RTT can generate an interrupt every time the prescaler rolls over. Usually the RTT is configured to generate an interrupt every second, so the prescaler will be programmed with the value 7FFFh.

The RTT can also generate an alarm if a preprogrammed 32-bit value is reached by the counter.

4.9. Timer Counter (TC)

The TC consists of three independent 16-bit Timer/Counter units. They may be cascaded to form a 32-bit or 48-bit timer/counter. On the Stamp9261, the external signals are not available as they are multiplexed on the Processor with the upper 16 bits of the data bus. The timers can therefore only run on the internal clock sources:

- MCK/2, MCK/8, MCK/32, MCK/128, SLCK,
- or the output of another timer channel.

4.10. Periodic Interval Timer (PIT)

The PIT consists of a 20-bit counter running on MCK / 16. This counter can be preloaded with any value between 1 and 2^{20} . The counter increments until the preloaded value is reached. At this stage it rolls over and generates an interrupt. An additional 12-bit counter counts the interrupts of the 20 bit counter.

The PIT is intended for use as the operating system's scheduler interrupt.

4.11. Watchdog Timer

The watchdog timer is a 12-bit timer running at 256 Hz (Slow Clock / 128). The maximum watchdog timeout period is therefore equal to 16 seconds. If enabled, the watchdog timer asserts a hardware reset at the end of the timeout period. The application program must always reset the watchdog timer before the timeout is reached. If an application program has crashed for some reason, the watchdog timer will reset the system, thereby reproducing a well defined state once again.

The Watchdog Mode Register can be written only once. After a Processor Reset, the watchdog is already activated and running with the maximum timeout period. Once the watchdog has been reconfigured or deactivated by writing to the Watchdog Mode Register, only a Processor Reset can change its mode once again.

4.12. Bus Matrix

The SAM9261 Processor's Bus Matrix consists of 5 masters and 5 slaves:

The Bus Masters are:

- ARM926EJS Core Instruction Fetch,
- ARM926EJS Core Data I/O,
- USB Host DMA,
- LCDC-DMA,
- Peripheral DMA Controller (PDC).

Bus Slaves are:

- internal ROM,
- internal SRAM,
- EBI,
- internal peripherals,
- LCDC and USB Host port.

EBI connects to external devices. In the case of the Stamp9261 these consist in the SDRAM, the flash memory and the Ethernet Controller. The LCDC and the USB Host ports share a common slave bus connection.

The Bus Matrix provides independent paths for each Master/Slave connection. For example, the LCDC-DMA can fetch video data from its video RAM (which we assume is allocated within the SDRAM) at the same time as the USART DMA (a PDC channel) stores data within the internal SRAM.

4.13. LCD Controller (LCDC)

The LCD Controller of the SAM9261 processor (theoretically) supports displays with a resolution up to 2048x2048 pixels with a color depth of 24 bit per pixel, or 8 bit per color. To implement a fitting LCD, glue hardware is necessary.

The LCD controller relies on a relatively simple frame buffer concept, which means that all graphics and character functions have to be implemented in software: character sets and graphic primitives are not integrated in the controller.

a) LCDC Initialization and LCD Power Sequencing

LCD cells (pixels) should not be subjected to DC power for prolonged periods of time, as chemical decomposition might take place. The LCD controller therefore provides for a strict AC control of the LCD pixels. To do so, the LCD controller has to be initialized appropriately. Switching on the LCD supply voltage therefore has to take place after the LCDC initialization or shortly before.

Accordingly, the LCDC should not be powered down without deactivating the LCD supply voltage. The same is true if the LCDC is stopped indirectly by stopping the respective clock source, namely the PLLA.

The LCD backlight supply is not involved in these considerations. It may be switched on or off at any time independently of the state of the LCDC.

b) LCDC Video Memory Selection

The video memory of the LCDC is part of the working memory of the processor. It might either reside in the internal SRAM, as well as in the external SDRAM. Using the internal SRAM has the advantage that the LCDC can access its video memory via an autonomous bus and does not affect the processor performance. However, as the internal SRAM has a capacity of only 160 KBytes, the color depth for a QVGA display is only 16 bit / pixel ($320 \times 240 \times 2 = 153600$ bytes are necessary). For a high quality display 16 bit per pixel might not be sufficient.

On the other hand, using the SDRAM as video memory has the advantage that there is plenty of space for all resolutions. Also the internal SRAM is now available for time critical software sections. Of course the LCDC will now be permanently scanning its video memory and might therefore reduce the overall performance to some degree.

c) LCDC Frame Buffer

The LCDC video memory is organized as a frame buffer in a straight forward way. It supports color depths of 1, 2, 4, 8, 16, or 24 bit per pixel. The video data is stored in a packed form with no unused bits in the video memory.

The color resolutions of 1, 2, 4, and 8 bpp (bits per pixel) use a palette table which is made up of 16-bit entries. The value of each pixel in the frame buffer serves as an index into the palette table. The value of the respective palette table entry is output to the display by the LCDC.

Each palette table entry has the form

Bit 15	Bit[14..10]	Bit[9..5]	Bit[4..0]
Intensity Bit	Blue[7..3]	Green[7..3]	Red[7..3]

The bits 2..0 of each color channel are not used in the palletized configuration – they are set to zero. The intensity bit sets the least significant valid bits of every color, that is, the bits 2, 10, and 18 of a 24-bit LCDC output word.

The same scheme as above is used in the 16-bit color resolution configuration, although in this case the frame buffer entry is output directly to the display instead of indexing a palette table.

In the 24-bit color resolution configuration, each frame buffer entry consists of one byte for each color:

Bit[23..16]	Bit[15..8]	Bit[7..0]
Blue[7..0]	Green[7..0]	Red[7..0]

The "BGR" (blue-green-red) sequence in the SAM9261 LCDC is not frequently used by graphics libraries or bitmaps ("RGB" is more of a standard), neither is the use of bit 15 as an intensity bit. Of course, the first problem can be circumvented by connecting the LCDC lines to the LCD in a way deviating from the Atmel designation, that is, by exchanging the "blue" against the "red" lines.

The Linux frame buffer driver offers a function which returns the information about the frame buffer structure including the assignment of each frame buffer bit to a color channel bit. It is recommended that graphics software uses this function in order to achieve a correct color representation.

4.14. LCDC DMA and FIFO

To provide for a periodic display refresh, the LCDC comprises a DMA channel and a 2 KB FIFO.

4.15. Display (TFT)

The Stamp9261 is provided without a display. The implementation of a display design is subject to the user.

4.16. Touchscreen

The SPI-based ADS7843 is implemented on the Evaluation-Board Design. It is connected to the Second SPI-Bus of the AT91SAM9261. Its Pins are multiplexed with the Knob on the Evaluation-Board so both input devices can't be used at the same time.

4.17. Advanced Interrupt Controller (AIC)

The Advanced Interrupt Controller can handle up to 32 internal or external interrupt sources. On the SAM9261 processor, only 24 of them are actually used.

The AIC integrates an 8-level priority controller.

Interrupt sources can be programmed to be level sensitive or edge triggered. The polarity can be programmed for all external interrupt sources.

There are three external interrupt signals available on the connectors of the Stamp9261:

- IRQ0, IRQ1, and IRQ2.

Moreover, all PIO lines can be used to generate a PIO interrupt. However, the PIO lines can only generate level change interrupts, that is, positive as well as negative edges will generate an interrupt. The PIO interrupt itself (PIO to AIC line) is usually programmed to be level-sensitive. Otherwise interrupts will be lost if multiple PIO lines source an interrupt simultaneously.

4.18. Peripheral DMA Controller (PDC)

The PDC provides both a receive and a transmit channel for each of the following full-duplex devices:

- USARTs
- Debug UART
- SPIs
- SSCs

The following half duplex device uses one bidirectional DMA channel:

- MCI

The DMA controllers of the USB Host interface and the LCD controller have specific characteristics and are not part of the PDC.

The address space of the DMA registers of one DMA channel as well as the interrupt of that channel are assigned to the appropriate peripheral. The PDC registers thus do not occupy a contiguous address range.

a) PDC Registers

A DMA channel consists of a

- pointer register
- counter register
- new pointer register
- new counter register
- status register (enable/disable status)
- control (enable/disable) register

The counter register has 16 bits. The maximum buffer size for a single DMA transfer is thus limited to 64kB. The PDC supports 8-bit, 16-bit and 32-bit data words. They are selected according to the requirements of the associated peripheral device.

b) PDC Interrupts

There are four kinds of interrupt generated by the PDC:

- End of Receive Buffer
- End of Transmit Buffer
- Receive Buffer Full
- Transmit Buffer Empty

The "End of Receive Buffer" / "End of Transmit Buffer" interrupts signify that the DMA counter has reached zero. The DMA pointer and counter register will be reloaded from the reload registers ("DMA new pointer register" and "DMA new counter register") provided that the "DMA new counter register" has a non-zero value. Otherwise a "Receive Buffer Full" or, respectively, a "Transmit Buffer Empty" interrupt is generated, and the DMA transfer terminates. Both reload registers are set to zero automatically after having been copied to the DMA pointer and counter registers.

4.19. Debug Unit (DBGU)

The Debug-Unit is a simple UART which provides only RX/TX lines. It is used as a simple serial console for Firmware and Operating Systems.

4.20. JTAG Unit

The JTAG unit can be used for hardware diagnostics, hardware initialization, flash memory programming, and debug purposes.

The JTAG unit supports two different modes, namely the "ICE Mode", and the "Boundary Scan" mode. The Stamp9261 is normally jumpered for "ICE Mode".

JTAG interface devices are available for the SAM9261. However, the use of the JTAG unit is not within the scope of this document.

4.21. Two-wire Interface (TWI)

The TWI is also known under the expression "I²C-Bus", which is a trademark of Philips and may therefore not be used by other manufacturers. However, interoperability is guaranteed.

The TWI uses only two lines, namely serial data (SDA) and serial clock (SCL). According to the standard, the TWI clock rate is limited to 400 kHz in fast mode and 100 kHz in normal mode. On the SAM9261, however, the baudrate can be fixed to any value between

MCK/6 and

$MCK / (255 \cdot 128 \cdot 2 + 6) \approx MCK / 64k$.

4.22. MultiMedia Card Interface (MCI)

The Stamp9261, or its SAM9261 processor, offer full support for interfacing MultiMedia Cards. The MCI ist multiplexed with the SPI-0 port.

Offering SD-Card support on devices like the Stamp9261 is not royalty-free. It is therefore not documented in this manual.

4.23. USB Host Ports (UHP)

Two independent USB 2.0 Full Speed host ports are integrated in the SAM9261 processor. According to the USB specification, the term "Full Speed" denotes a transmission rate of 12 MBit/s. A "High Speed" mode (480 MBit/s) is not available with the SAM9261.

a) External Parts

A few external parts are required for the proper operation of the UHP:

- Pull-down resistors on each line of approximately 15 k Ω . These should be installed even if the UDP is not to be used at all in order to keep the signals from floating.
- Series resistors of 27 Ω (5%) on each line.
- Small capacitors (e.g. 15pF) to ground on each line (optional).
- ESD protection devices are recommended for applications which are subject to external contact. The restrictions with regard to capacitive loading have to be applied when selecting a protection device.
- A circuit to generate the 5V V_{BUS} supply voltage.

b) V_{BUS} considerations for USB Host

A USB host port has to provide a supply voltage V_{BUS} of 5V +/- 5% which has to be able to source a maximum of 500mA, or 100mA in case of battery operation. Please refer to the appropriate rules in the USB specification. A low ESR capacitor of at least 120 μ F has to be provided on V_{BUS} in order to avoid excessive voltage drops during current spikes.

V_{BUS} has to have an over-current protection. The over-current drawn temporarily on V_{BUS} must not exceed 5A. Polymeric PTCs or solid state switches are recommended by the specification. Suitable PPTCs are "MultiFuse" (Bourns), "PolyFuse" (Wickmann/Littelfuse), "PolySwitch" (Raychem/Tyco).

It is required that the over-current condition can be detected by software, so that V_{BUS} can be switched off or be reduced in power in such a case.

c) Layout considerations

The external resistors should be placed in the vicinity of the Stamp9261 connector. The two traces of any of the differential pairs (USB-Host A+ and USB-Host A- , as well as USB-Host B+ and USB-Host B-) should not encircle large areas on the base board, in order to reduce signal distortion and noise. They are preferably routed closely in parallel from the Stamp9261 to the USB connector.

4.24. USB Device Port (UDP)

a) External Parts

A few external parts are required for the proper operation of the UDP:

- Pull-down resistors on each line of approximately 330 k Ω . These should be installed even if the UDP is not to be used at all in order to keep the signals from floating.
- Series resistors of 27 Ω (5%) on each line.
- Small capacitors (e.g. 15pF) to Ground on each line (optional).
- A voltage divider on the 5V USB supply voltage V_{BUS} converting this voltage to 3.3V, e.g. 27 k Ω / 47 k Ω , for the V_{BUS} monitoring input (USB_CNX).
- ESD protection devices are recommended for applications which are subject to external contact. The restrictions with regard to capacitive loading have to be applied when selecting a protection device.

The USB specification (revision 2.0 of April 27, 2000, chapter 7.1.1.1) demands a cable with a characteristic impedance of 90 $\Omega \pm 15\%$. Matching this impedance would require a driver output impedance of 45 Ω on both the negative and the positive driver. Nevertheless, the SAM9261 manual demands external resistors of 27 Ω . These would correspond to intrinsic resistances of the drivers of 18 Ω .

The USB specification demands a switchable pull-up resistor of 1.5 k Ω on USB-Device+ which identifies the UDP as a full speed device to the attached host controller. On the AT91SAM9261 processor, this resistor is integrated on the chip. It can be switched on or off using the "USB Pad Pull-up Control Register", which is part of the "Bus Matrix User Interface" (not the "USB Device Port User Interface", as one might expect). This pull-up resistor is required to be switchable in order not to source current to an attached but powered down host. This would otherwise constitute an irregular condition on the host. The software has to take care of this fact.

The capacitors are intended to improve the signal quality (edge rate control) in dependency of the specific design. They are not mandatory. The total capacitance to ground of each USB pin, the PCB trace to the series resistor, and the capacitor must not exceed 75pF.

b) Operation with V_{BUS} as a Supply

Special care has to be taken if the Stamp9261 is powered by the V_{BUS} supply. Please refer to the appropriate rules in the USB specification with regard to inrush current limiting and power switching. As the Stamp9261 draws more than 1W in normal mode, it is a "high-power" device according to the specification (<100mA = "low-power", 100..500mA = "high-power"). It therefore requires staged switching which means that at power-up it should draw not more than 100mA on V_{BUS} . The capacitive load of a USB device on V_{BUS} should be not higher than 10 μ F.

c) Layout considerations

The external resistors should be placed in the vicinity of the Stamp9261 connector. The traces of the differential pair (USB-Device+ and USB-Device-) should not encircle large areas on the base board, in order to reduce signal distortion and noise. They are preferably routed closely in parallel from the Stamp9261 to the USB connector.

4.25. Ethernet Controller

A Davicom DM9000A 10/100 MBit Ethernet Controller is implemented on the Stamp Adaptor Board. It serves as a reference Design and a 10/100 MBit Twisted-Pair Magnetic Module (transformer plus filter).

Software drivers are available for the DM9000A for Linux 2.4/2.6 and Windows CE 4.2/5.0/6.0.

a) MAC Address

An individual 48-bit MAC address (Ethernet hardware address) is allocated to each Stamp9261. This number is stored in flash memory as a U-Boot parameter. It is recommended not to change the MAC address in order to comply with the IEEE Ethernet standards.

b) Layout considerations

Please take care of the specific layout requirements of the Ethernet port when designing a base board. The two signals of the transmitter pair (ETX+ and ETX-) should be routed in parallel (constant distance, e.g. 0.5mm) with no vias on their way to the RJ45-jack. The same is true for the receiver pair (ERX+ and ERX-). No other signals should be crossing or get next to these lines. If a ground plane is used on the base board, it should be omitted in the vicinity of the Ethernet signals.

A 1nF / 2kV capacitor should be connected between board ground and chassis ground (which is usually connected to the shield of the RJ45-jack).

c) Ethernet LEDs

Two LED outputs from the DM9000A controller can be used on the base board. LED_S indicates the current speed of the Ethernet connection (100MBit = on, 10 MBit = off). LED_L indicates the combined link and carrier sense signal (LED mode 1 of the DM9000A), or only the carrier sense signal (LED mode 0).

4.26. Synchronous / Asynchronous Serial Interfaces (USART)

Three USARTs and one UART are integrated into the SAM9261 processor.

The UART ("Debug" UART) is used as the Stamp9261's standard input/output port. It supports only the normal mode (RS232 mode).

A receive and a transmit DMA channel is assigned to each USART / UART.

a) USART Modes

Six different modes are implemented within the USARTs:

- Normal (standard RS232 mode)
- RS485
- Hardware Handshaking
- ISO7816 Protocol: T=0
- ISO7816 Protocol: T=1
- IrDA

• *RS485 Operating Mode*

In this mode, the RTS pin is automatically driven high during transmit operations. If RTS is connected to the "enable" line of the RS485 driver, the driver will thus be enabled only during transmit operations.

• *Hardware Handshaking Operating Mode*

The hardware handshaking feature enables an out-of-band flow control by automatic management of the pins RTS and CTS. The receive DMA channel must be active for this mode. The RTS signal is driven high if the receiver is disabled or if the DMA indicates a buffer full condition. As the RTS signal is connected to the CTS line of the connected device, its transmitter is thus prevented from sending any more characters.

• *Smart Card Operating Modes*

The USARTs have an ISO7816-compatible mode which permits interfacing with smart cards and Security Access Modules (SAM). Both T=0 and T=1 protocols of the ISO7816 specification are supported.

• *IrDA Operating Mode*

The USART features an infrared (IrDA) mode supplying half-duplex point-to-point wireless communication. It includes the modulator and demodulator which allows a glueless connection to the infrared transceivers.

The modulator and demodulator are compliant with the IrDA specification version 1.1 and support data transfer speeds ranging from 2.4 kb/s to 115.2 kb/s.

b) Signals of the serial interfaces

All UARTs/USARTs have one receiver and one transmitter data line (full duplex). The UARTS #1 and #2 also have two handshake lines – RTS and CTS – as well as a clock line (SCK) for the synchronous protocols.

The Debug UART only has receiver and transmitter data lines. The same is true for USART #0 - its handshake lines are not externally available on the Stamp9261.

The RI, DTR, DSR and DCD lines of USART #1 designated in the pin description of the Stamp9261 are not really part of the USART unit of the SAM9261. They are rather implemented as standard digital ports (PIO ports).

c) Hardware Interrupts of the Serial Interfaces

There are several interrupt sources for each USART.

- Receive: RX Ready, (DMA) Buffer Full, End of Receive Buffer
- Transmit: TX Ready, (DMA) Buffer Empty, End of Transmit Buffer, Shift Register Empty
- Errors: overrun, parity, framing, and timeout errors
- Handshake: the status of CTS has changed
- Break: the receiver has detected a break condition on RXD
- NACK: non acknowledge (ISO7816 mode only)
- Iteration: the maximum number of repetitions has been reached (ISO7816 mode only)

Please refer to the chapter about the DMA unit (PDC) for a description of the "Buffer Full" and "End of Receive / Transmit Buffer" events.

4.27. Synchronous Peripheral Interface (SPI)

Two SPI ports, each of them with three chip selects, are available on the Stamp9261. The SPI baud rate is Master Clock (MCK) divided by a value between 1 and 255.

A receive and a transmit DMA channel is assigned to each of the two SPIs.

4.28. Synchronous Serial Controller (SSC)

The three Synchronous Serial Controllers of the SAM9261 processor are available which one to use depends on the multiplexing of the pins with other devices used in the application.

The SSC supports many serial synchronous communication protocols generally used in audio and telecom applications such as I2S, Short Frame Sync, Long Frame Sync, etc.

The SSC has separated receive and transmit channels. Each channel has a data, a clock and a frame synchronization signal (RD, RK, RF, resp. TD, TK, TF).

Both a receive and a transmit DMA channel are assigned to each SSC.

4.29. Parallel Input /Output Controller (PIO)

The Stamp9261 has a maximum of 39 freely programmable digital I/O ports on its connectors. They can be configured independently of each other as input or output. These pins are also used by other peripheral devices.

The SAM9261 Processor comes with 3 PIO controllers, each of them can manage up to 32 programmable I/O ports. Each I/O port is associated with a bit number in the 32 bit register of the user interface. Each I/O port may be configured for general purpose I/O or assigned to a function of an integrated peripheral device. In doing so multiplexing with 2 integrated devices is possible. That means a pin may be used as GPIO, device A or device B.

The following characteristics are individually configurable for each PIO pin:

- PIO enable
- Peripheral A or B enable
- Output enable
- Output level
- Write Enable
- Level change interrupt
- Glitch filter: pulses that are lower than a half clock cycle are ignored
- Open-drain outputs
- Pull-up resistor

All configurations as well as the pin status can be read back by using the appropriate status register. Multiple pins of each PIO can also be written simultaneously by using the synchronous output register.

A number of the PIO signals are used internally on the Stamp9261. Care has to be taken when accessing the PIO registers in order not to change the settings of these internal signals – otherwise a system crash is likely to happen.

4.30. Power Management

Using power management can dramatically reduce the power consumption of an Embedded Device. We assume that almost no application will use the maximum performance of the CPU and the peripherals all of the time. The following possibilities for power management are available on the Stamp9261:

- switching off the TFT supply voltage
- putting the SDRAM into self-refresh mode
- putting the Ethernet controller in power down mode
- stopping the PLLs (PLLA and / or PLLB)
- stopping the clocks of the various peripherals
- reducing the clock rates of peripherals, especially by changing MCK.

a) Beware of tampering with the LCDC !

It is not recommended to reduce the clock speed of the LCD controller. Instead, the LCDC clock should be stopped and the power supply for the LCD switched off, as otherwise the LCD can be damaged.

b) Idle Mode

In idle mode, the processor clock will be re-enabled by any interrupt. The peripherals, however, are only able to generate an interrupt if they still have a clock, so care has to be taken as to when a peripheral can be powered down.

It should also be taken into account that when a PLL is stopped it will take some time to restart it. Changing the PLL frequencies or stopping them can therefore be done only at a moderate rate. If short reaction times are required, this is not a choice.

c) Slowing down MCK

However, in many cases a system waits for a user action or some other rare event. In such a case, it is possible to change MCK to SLCK. Any external event which changes the state on peripheral pins (not the USB) can then be detected by the PIO controller or the AIC.

d) Low Power SDRAM

The Stamp9261 makes use of Low Power (Mobile) SDRAM. The enhanced low power features of the SDRAM controller are thus available:

- deep power down (all SDRAM data is lost)
- partial self-refresh (only part of the SDRAM is refreshed, data of all other parts is lost).

5. Stamp9261 Starter Kit

5.1. Starter Kit Contents

The Stamp9261 starter kit contains the following components:

- Stamp9261
- Stamp9261 Adaptor: Adapter board for connecting Stamp9261 and Stamp9261 Base
- Panel-Card EVB: Evaluation and Prototyping Board
- Wall Adapter Power Supply, Input AC 230V, Output DC 9 to 16V, min. 400 mA
- Serial "Null-Modem" Cable with two 9-pin D-type Connectors
- Adapter cable for accessing the Debug UART
- CD with Operating System, Toolchain, and Documentation

5.2. Panel-Card EVB

The Panel-Card EVB is designed to be both simple and universal. Some elements of the circuit board will not always be needed, but facilitate implementation for certain purposes. It was designed to serve both, the Panel-Card and the Stamp9261 as an evaluation platform.

a) First Steps

The Starter Kit board "Panel-Card EVB" makes it easy to put the Stamp9261 to use. The first steps involve the following:

- connecting the wall adapter to the main supply
- connecting the DBGU-Adapter and the serial cable to a COM port of a PC
- starting a terminal program for the selected COM port at 115200 baud, 8N1
- starting the Stamp9261 by connecting the DC plug of the wall adapter.

Boot messages of the Stamp9261 are now expected to appear on the terminal.

b) Power Supply

From an unregulated input voltage between 8 and 35V, two voltages are produced:

- 3.3V for the CPU module,
- 5V for USB and optional peripherals,

c) RS232 Interface

The RS232 port provides RS232 drivers/receivers for the RxD, TxD, RTS, CTS, RI and DCD signals of the USART1 of the Stamp9261. Instead of the usual DTR and DSR signals, the connector integrates the RxD and TxD lines of the Stamp9261's "Debug UART". To use the console port of the Stamp9261, which usually is identical to the Debug UART, the "DBGU adapter" has to be used. It connects the PC's TxD, RxD, and Ground lines to the appropriate pins of the DSUB-9 connector of the Stamp9261 Base.

d) Connectors

The following connectors are part of the Panel-Card EVB:

- Stamp9261 Adaptor slot, consisting of two 40-pin header connectors (0.1 inch pitch)
- Ethernet 10/100 MBit
- USB Host (dual)
- USB Device
- RS232
- MMC-Card Slot

-
- Matrix keyboard
 - Touch controller
 - JTAG
 - User Connector D-type 25pin
 - User Connector 26pin header (optional)
 - 2-contact terminal block for power supply
 - DC connector for power supply

e) Rotary Encoder

The Panel-Card EVB includes a rotary encoder with push-button which is a "Human Interface Device" well suited for many embedded applications. Generally spoken, it is a simplified replacement for a computer mouse, touch pad, or keyboard. The rotary encoder represents a pointing device with only one dimension, while the push-button serves as a "return" key or mouse button.

The rotary encoder is accessed by two PIO ports of the Stamp9261 (see circuit diagram). The push-button occupies another PIO port.

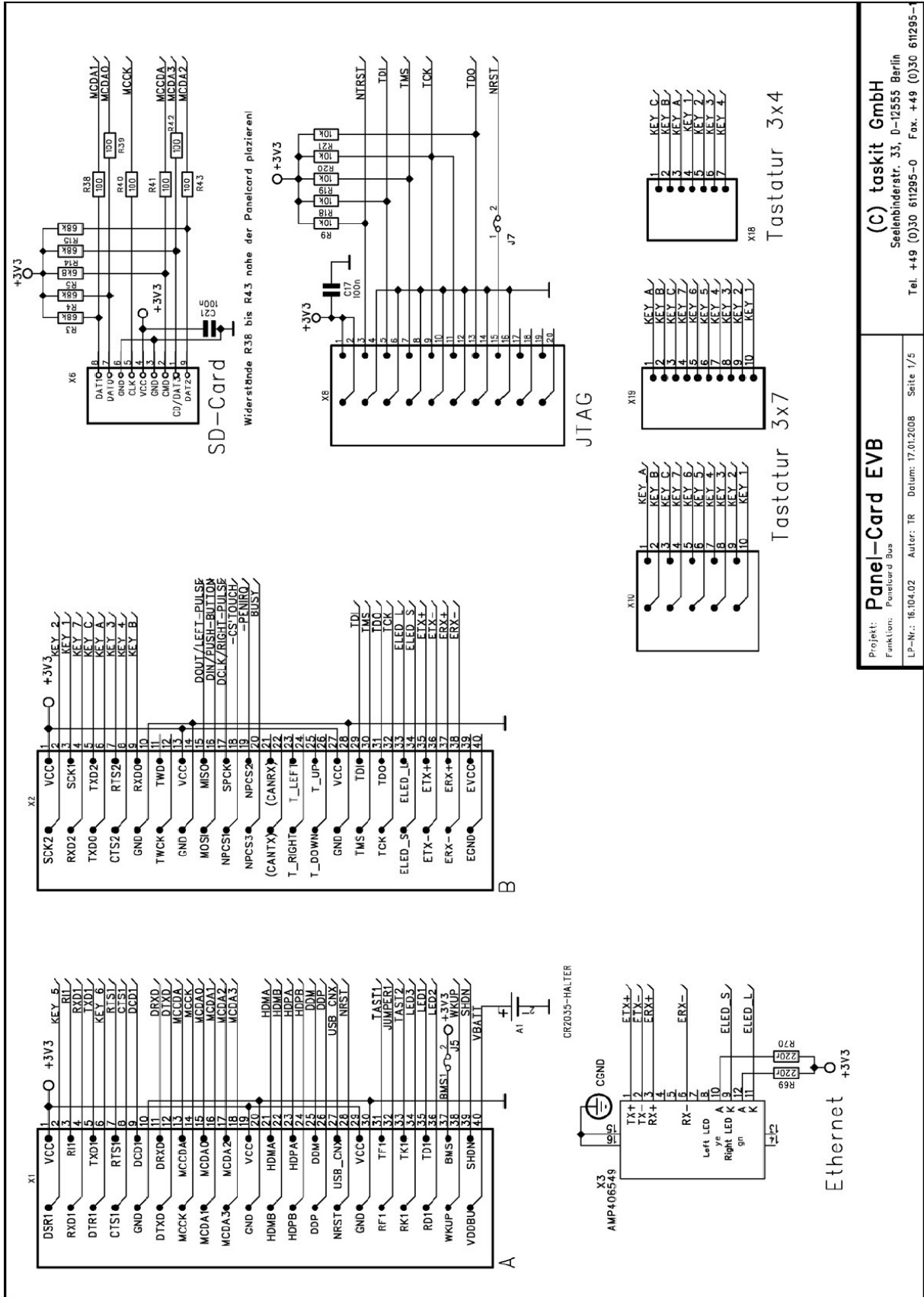
6. Schematics of "Panel-Card EVB" Evaluation and Prototyping Board

6.1. Disclaimer

The following circuit diagram is intended for reference only and does not dispense the user from checking and applying the appropriate standards. No warranty can be granted if parts of the circuit are used in customer applications.

The part of the schematics dealing with the power supply is not recommended for new designs. An updated schematics will be published in a later version of this document.

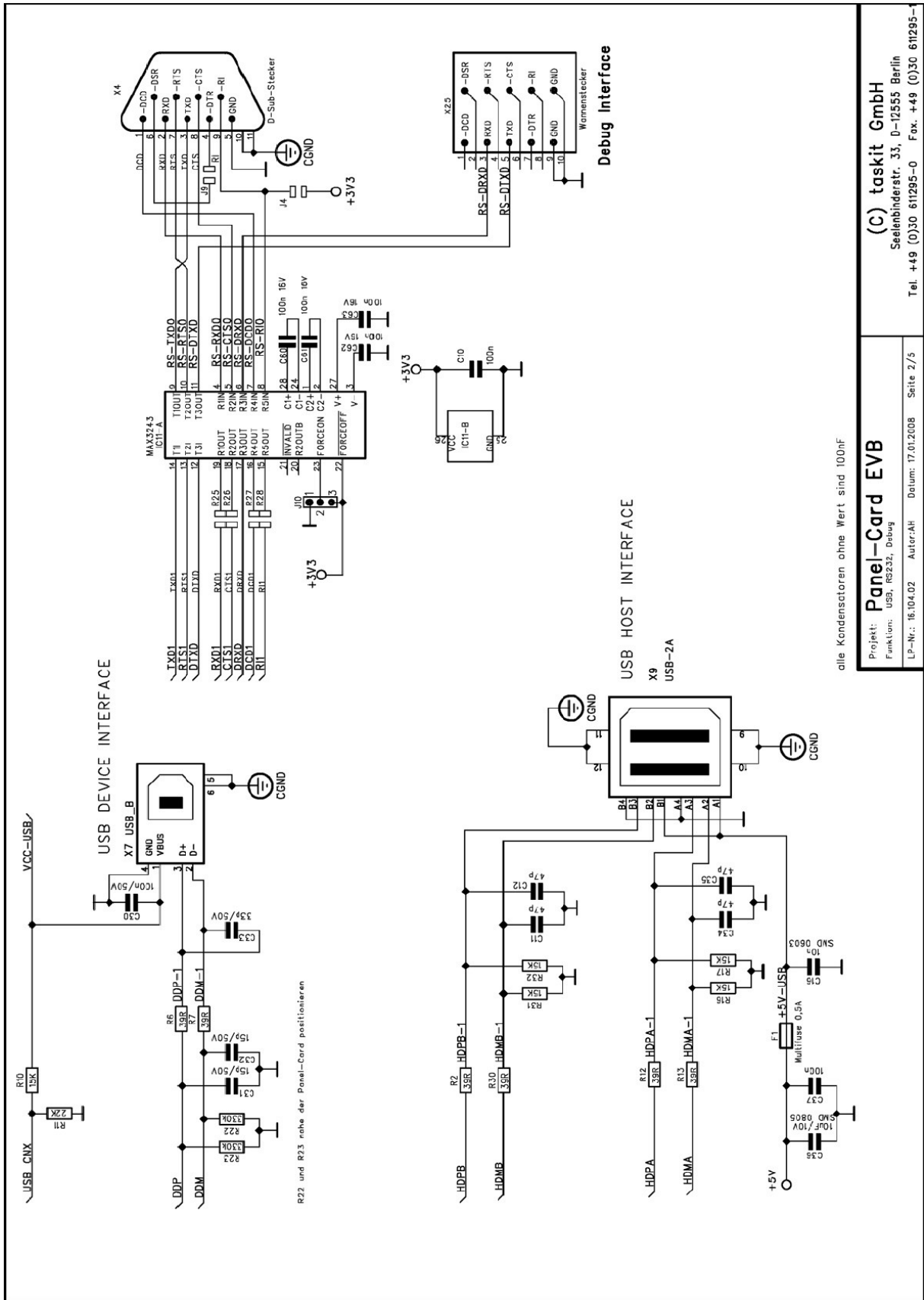
6.2. BUS Connector



Projekt: **Panel-Card EVB**
 Funktion: Panelcard Bus
 LP-Nr.: 16.104.02 Autor: TR Datum: 17.01.2008 Seite 1/5

(C) taskit GmbH
 Seelenbinderstr. 33, D-12555 Berlin
 Tel. +49 (0)30 61295-0 Fax. +49 (0)30 61295-1

6.3. Interfaces

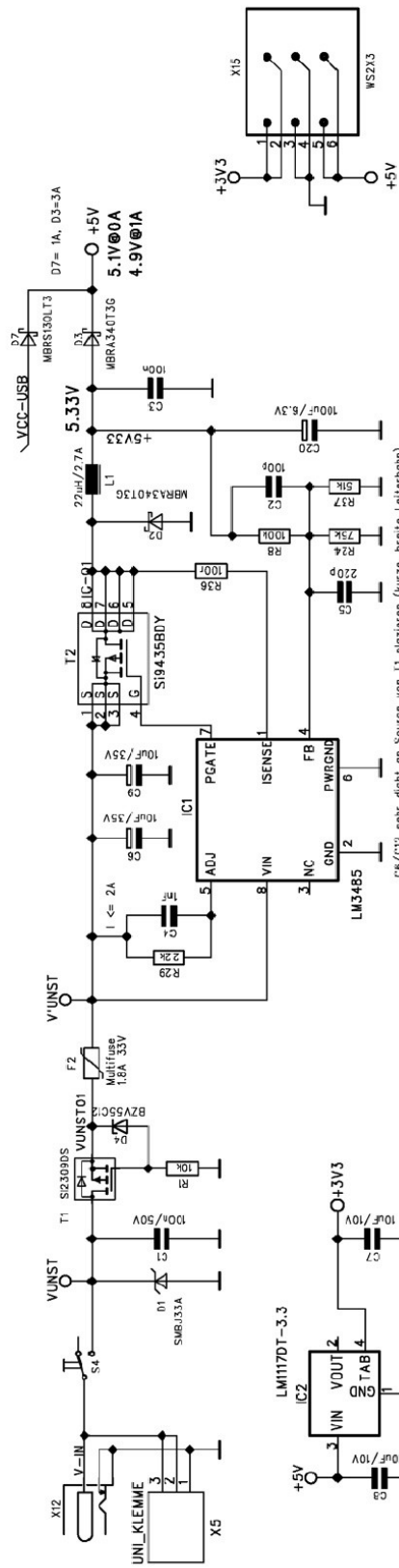


alle Kondensatoren ohne Wert sind 100nF

Projekt: **Panel-Card EVB**
 Funktion: USB, RS232, Debug
 LP-Nr.: 16.104.02 Autor:AH Datum: 17.01.2008 Seite 2/3

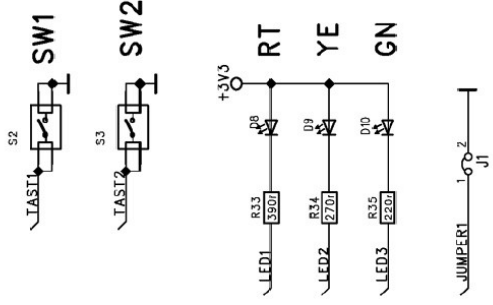
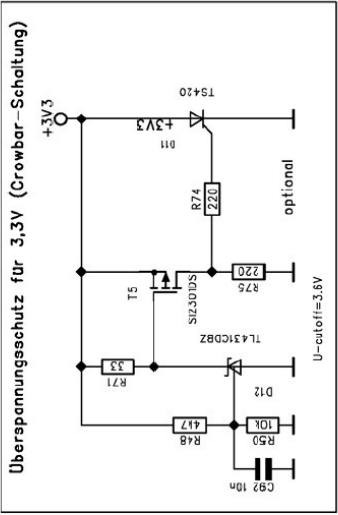
(C) taskit GmbH
 Seelenbinderstr. 33, D-12555 Berlin
 Tel. +49 (0)30 61295-0 Fax. +49 (0)30 61295-1

6.4. Power Supply

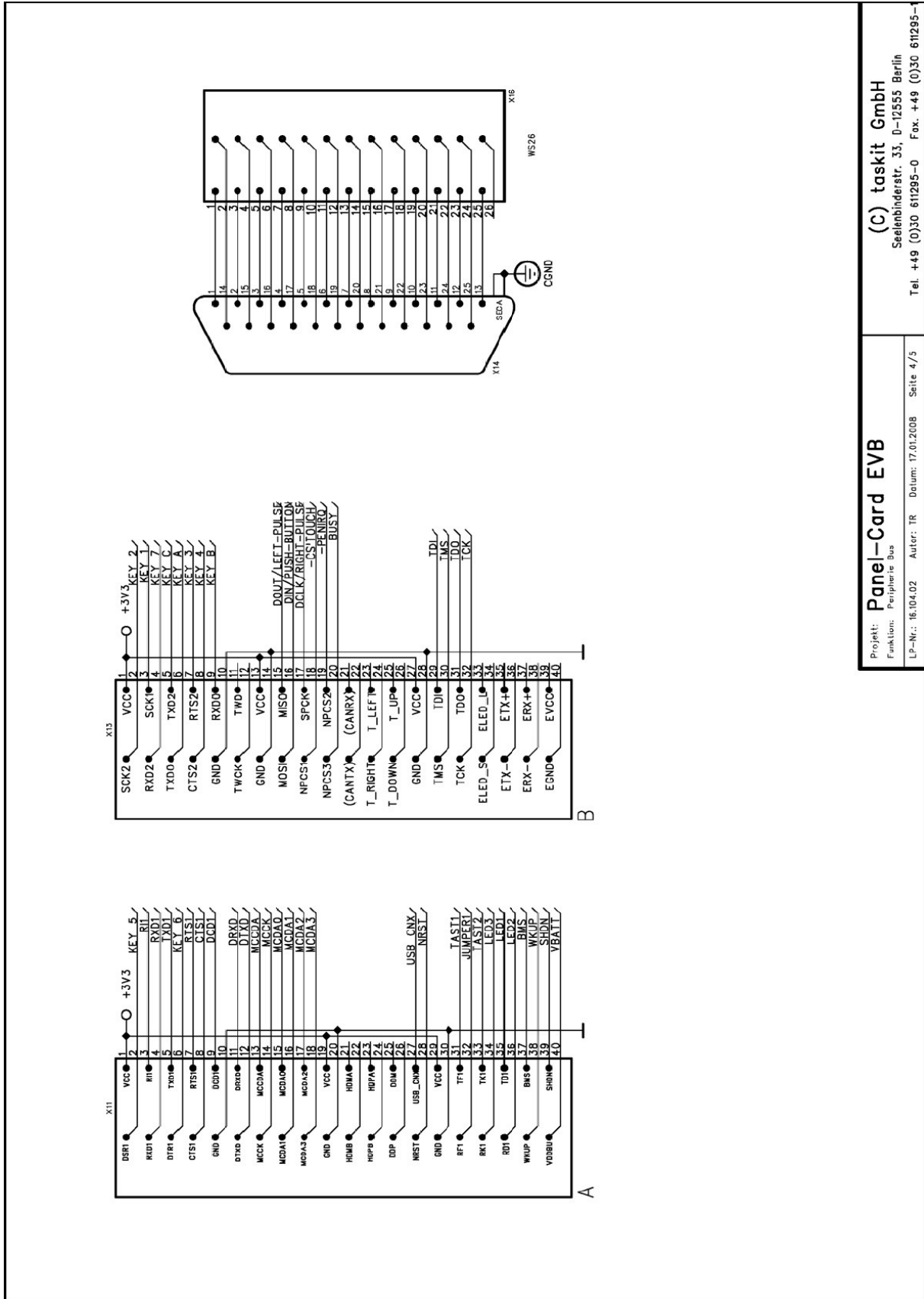


on TAB (Pin4) ca. 2cm Kupferfläche mit B bis10
verteilt, angeordnet. Vias zur FCC(+3V3)-Loge

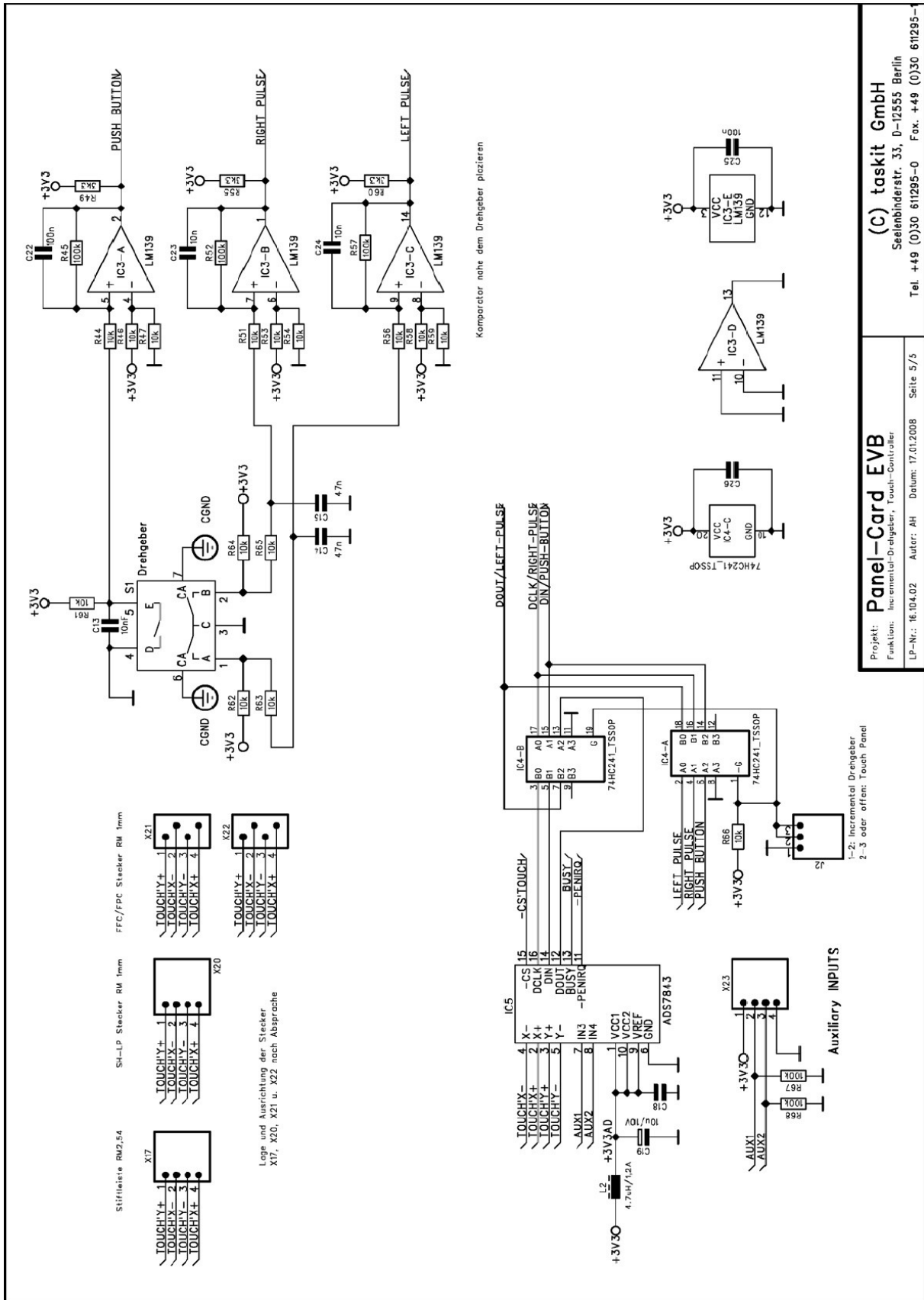
C6/C12 sehr dicht an Source von I1 platzieren (kurze breite Leiterbahn)
Alternative zu Zx Tentel 100µF: 1x SMD-Eliko 22µ (47µ) 35 V; ESR beachten!



6.5. Extension Connectors



6.6. HID Devices



Komparator nahe dem Drehgeber platzieren

1-2: Incremental Drehgeber
2-3 oder offen: Touch Panel

7. Address Map (Physical address space)

After the execution of the **remap** command the 4 GB physical address space is separated as shown in the following table. Accessing these addresses directly is only possible if the MMU (memory management unit) is deactivated. As soon as the MMU is activated the visible address space is changed completely. If absolute memory addresses should be accessed within an application, the corresponding address space has first to be mapped to the virtual address space using **mmap** or **ioremap** under Linux.

Address	Mnemonic	Function
00 0000	Boot Memory	Flash (NCS0) or internal ROM or internal SRAM
10 0000	ITCM	Instruction TCM (Tightly Coupled Memory) Internal SRAM A: 0, 16, 32 or 64 kB
20 0000	DTCM	Data TCM (Tightly Coupled Memory) Internal SRAM B: 0, 16, 32 or 64 kB
30 0000	SRAM	Internal SRAM C SRAM A + SRAM B + SRAM C = 160 kB
40 0000	ROM	Internal ROM 32 kByte
50 0000	UHP	USB Host Port
60 0000	LCD	LCD Controller
1000 0000	EBI NCS0	Chip Select 0: Flash Memory #1, up to 128 MB
2000 0000	EBI NCS1	Chip Select 1: SDRAM, up to 64 MB
3000 0000	EBI NCS2	Chip Select 2: Ethernet Controller
4000 0000	EBI NCS3	Chip Select 3: Flash Memory #2, up to 128 MB
FFFA 0000	TC0, TC1, TC2	3 Timer Counter, 16-Bit
FFFA 4000	UDP	USB Device Port
FFFA 8000	MCI	Multimedia Card / SD-Card Interface
FFFA C000	TWI	Two Wire Interface (I ² C)
FFFB 0000	USART0	Synchronous or Asynchronous Serial Port #0
FFFB 4000	USART1	Synchronous or Asynchronous Serial Port #1
FFFB 8000	USART2	Synchronous or Asynchronous Serial Port #2
FFFB C000	SSC0	Serial Synchronous Controller (I ² S) #0
FFFC 0000	SSC1	Serial Synchronous Controller (I ² S) #1
FFFC 4000	SSC2	Serial Synchronous Controller (I ² S) #2
FFFC 8000	SPI0	Serial Peripheral Interface #0
FFFC C000	SPI1	Serial Peripheral Interface #1
FFFF EA00	SDRAMC	SDRAM Controller
FFFF EC00	SMC	Static Memory Controller
FFFF EE00	MATRIX	Bus Matrix User Interface
FFFF F000	AIC	Interrupt Controller
FFFF F200	DBGU	Debug Unit, including UART
FFFF F400	PIOA	32 Bit Parallel I/O Controller A
FFFF F600	PIOB	32 Bit Parallel I/O Controller B
FFFF F800	PIOC	32 Bit Parallel I/O Controller C
FFFF FC00	PMC	Power Management Controller
FFFF FD00	RSTC	Reset Controller, Battery Powered
FFFF FD10	SHDWC	Shutdown Controller, Battery Powered
FFFF FD20	RTT	Real-time Timer 32 Bit, Battery Powered
FFFF FD30	PIT	Periodic Interval Timer 32 Bit
FFFF FD40	WDT	Watchdog Timer
FFFF FD50	GPBR	4 General Purpose Backup Registers, Battery Powered
various	PDC	Peripheral DMA Controller (each channel's address space is assigned to the address space of its respective device)

8. Peripheral Identifiers

The Peripheral Identifiers are used to address the corresponding peripheral unit in the interrupt controller (AIC) and in the power management controller (PMC).

ID	Mnemonic	Usage	External Interrupt
0	FIQ	External Fast IRQ	FIQ
1	SYSIRQ	System Interrupt: OR'ed IRQs of SDRAMC, DBGU, PIT, RTT, WDT, RST, PMC	
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	PIOC	Parallel I/O Controller C	
5		Reserved	
6	USART0	Synchronous or Asynchronous Serial Port #0	
7	USART1	Synchronous or Asynchronous Serial Port #1	
8	USART2	Synchronous or Asynchronous Serial Port #2	
9	MCI	Multi-Media Card / SD-Card	
10	UDP	USB Device	
11	TWI	Two Wire Interface (I ² C-Bus)	
2	SPIO0	Serial Peripheral Interface #0	
13	SPI1	Serial Peripheral Interface #1	
14	SSC0	Serial Synchronous Controller (I ² S) #0	
15	SSC1	Serial Synchronous Controller (I ² S) #1	
16	SSC2	Serial Synchronous Controller (I ² S) #2	
17	TC0	Timer Counter #0	
18	TC1	Timer Counter #1	
19	TC2	Timer Counter #2	
20	UHP	USB Host	
21	LCDC	LCD Controller	
22		Reserved	
23		Reserved	
24		Reserved	
25		Reserved	
26		Reserved	
27		Reserved	
28		Reserved	
29	IRQ0	External IRQ0	IRQ0
30	IRQ1	External IRQ1	IRQ1
31	IRQ2	External IRQ2	IRQ2

9. Stamp Adaptor

9.1. Connector Pin Assignment and Pin Multiplexing

40 Pin Header X21

1	VCC		DSR1		PA27	2	
3	PA23		RI1	RXD1		PC13	4
5	PC12		TXD1	DTR1		PA28	6
7	PA12		RTS1	CTS1		PA13	8
9	PA29		DCD1	GND			10
11	PA9	PCK2	DRXD	DTXD	PCK3	PA10	12
13	PA1	SPI0 MOSI	MC CDA	MC CK	SPI0 CLK	PA2	14
15	PA0	SPI0 MISO	MC DA0	MC DA1	SPI0 CS1	PA4	16
17	PA5	SPI0 CS2	MC DA2	MC DA3	SPI0 CS3	PA6	18
19	VCC		GND				20
21		USB Host A-	USB Host B-				22
23		USB Host A+	USB Host B+				24
25		USB Device-	USB Device+				26
27	PC2	IRQ0	USBCNX	/RESET			28
29	VCC		GND				30
31	PA17	TF1	RF1		PA22		32
33	PA18	TK1	RK1		PA21		34
35	PA19	TD1	RD1		PA20		36
37		BMS	WKUP				38
39		SHDN	VBATT				40

40 Pin Header X22

1	VCC		SCK2		PA14	2	
3	PA11		SCK1	RXD2		PC15	4
5	PC14		TXD2	TXD0	PCK2	PC8	6
7	PA15		RTS2	CTS2		PA16	8
9	PC9	PCK3	RXD0	GND			10
11	PA7	PCK0	TWD	TWCK	PCK1	PA8	12
13	VCC		GND				14
15	PB30	SPI1 MISO	IRQ1	PCK2	SPI1 MOSI	PB31	16
17	PB29	SPI1 CLK	IRQ2		SPI1 CS1	PA24	18
19	PA25	SPI1 CS2			SPI1 CS3	PA26	20
21							22
23							24
25							26
27	VCC		GND				28
29		TDI	TMS				30
31		TDO	TCK				32
33		ELED_L	ELED_S				34
35		ETX+	ETX-				36
37		ERX+	ERX-				38
39		POE1	POE2				40

Color Code:

USART	Power Supply / Ground
Debug UART	TWI (I2C-Bus)
SD-Card/MMC	SPI
USB	Reserved
Synchronous Serial Controller (SSC)	JTAG
Control	Ethernet
Digital I/O Port	Programmable Clock Output

9.2. Connector Pin Description

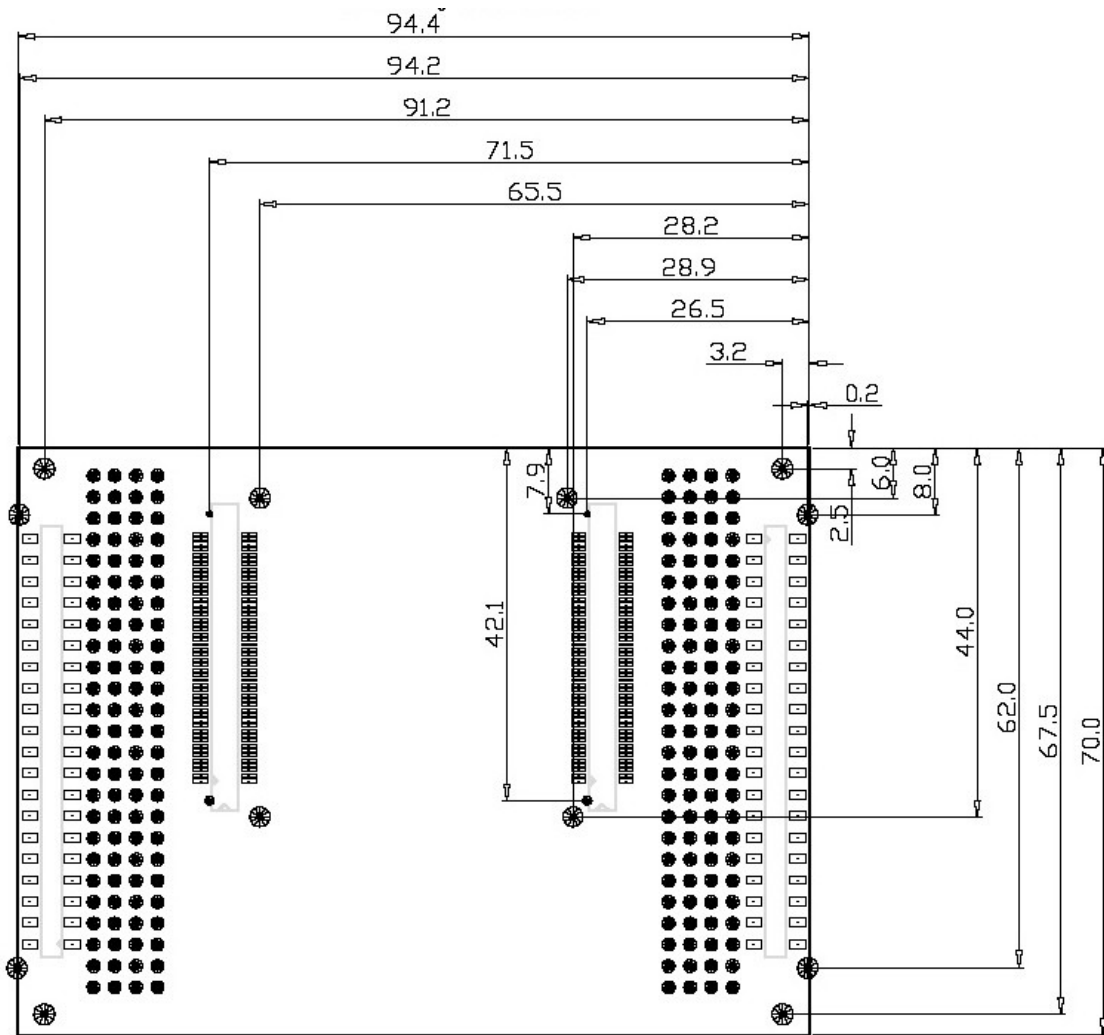
Mnemonic	Description	Type	Pin on X21	Pin on X22
VCC	System Supply 3.3V	Supply	1,19,29	1,13,27
VBATT	Backup Battery 2 ~ 3.3V. Must be connected to VCC if no battery is used.	Supply	40	
GND	System Ground	Ground	10,20,30	10,14, 28
/RESET	System Reset	OD, PU 1K	28	
BMS	Boot Mode Select: 1 = ROM Boot, 0 = Flash Boot	I, PD 1K	37	
IRQ0	Interrupt Request #1	I	27	
IRQ1	Interrupt Request #2	I	15	
IRQ2	Interrupt Request #3	I	17	
SHDN	Shutdown Controller Shutdown Output	O, 1.2V	39	
WKUP	Shutdown Controller Wakeup Input	I, 1.2V	38	
ERX-	Ethernet Receiver -	Analog I		37
ERX+	Ethernet Receiver +	Analog I		38
ETX-	Ethernet Transmitter -	Analog O		35
ETX+	Ethernet Transmitter +	Analog O		36
ELED S	Ethernet LED 1: 100MBit Indicator (speed LED, active low)	OD		34
ELED L	Ethernet LED 2: Link/Carrier Sense Indicator	OD		33
POE1	Center Tap of Transmit Transformer for Power over Ethernet	Analog I/O		39
POE2	Center Tap of Receive Transformer for Power over Ethernet	Analog I/O		40
TCK	JTAG Test Clock	I		32
TDI	JTAG Test Data In	I		29
TDO	JTAG Test Data Out	O		31
TMS	JTAG Test Mode Select	I		30
MC-CK	MultiMedia Card /SD-Card Clock	O	14	
MC-CDA	MultiMedia Card /SD-Card Command/Response	I/O	13	
MC-DA0	MultiMedia Card Data 0/ SD-Card Data[0]	I/O	15	
MC-DA1	SD-Card Data[1]	I/O	16	
MC-DA2	SD-Card Data[2]	I/O	17	
MC-DA3	SD-Card Data[3]	I/O	18	
PA00	PIO Line PA[0]	I/O	15	
PA01	PIO Line PA[1]	I/O	13	
PA02	PIO Line PA[2]	I/O	14	
PA04	PIO Line PA[4]	I/O	16	
PA05	PIO Line PA[5]	I/O	17	
PA06	PIO Line PA[6]	I/O	18	
PA07	PIO Line PA[7]	I/O		11
PA08	PIO Line PA[8]	I/O		12
PA09	PIO Line PA[9]	I/O	11	
PA10	PIO Line PA[10]	I/O	12	
PA11	PIO Line PA[11]	I/O		3
PA12	PIO Line PA[12]	I/O	7	
PA13	PIO Line PA[13]	I/O	8	
PA14	PIO Line PA[14]	I/O		2
PA15	PIO Line PA[15]	I/O		7
PA16	PIO Line PA[16]	I/O		8
PA17	PIO Line PA[17]	I/O	31	
PA18	PIO Line PA[18]	I/O	33	
PA19	PIO Line PA[19]	I/O	35	

(Connector Pin Description continued)

Mnemonic	Description	Type	Pin on X21	Pin on X22
PA20	PIO Line PA[20]	I/O	36	
PA21	PIO Line PA[21]	I/O	34	
PA22	PIO Line PA[22]	I/O	32	
PA23	PIO Line PA[23]	I/O	3	
PA24	PIO Line PA[24]	I/O		18
PA25	PIO Line PA[25]	I/O		19
PA26	PIO Line PA[26]	I/O		20
PA27	PIO Line PA[27]	I/O	2	
PA28	PIO Line PA[28]	I/O	6	
PA29	PIO Line PA[29]	I/O	9	
PB29	PIO Line PB[29]	I/O		17
PB30	PIO Line PB[30]	I/O		15
PB31	PIO Line PB[31]	I/O		16
PC02	PIO Line PC[2]	I/O	27	
PC08	PIO Line PC[8]	I/O		6
PC09	PIO Line PC[9]	I/O		9
PC12	PIO Line PC[12]	I/O	5	
PC13	PIO Line PC[13]	I/O	4	
PC14	PIO Line PC[14]	I/O		5
PC15	PIO Line PC[15]	I/O		4
PCK0	Programmable Clock #0	O		11
PCK1	Programmable Clock #1	O	12	
PCK2	Programmable Clock #2	O	11	6, 16
PCK3	Programmable Clock #3	O	12	9
SPI0-CS1	Serial Peripheral Interface #0 Chip Select 1	O	16	
SPI0-CS2	Serial Peripheral Interface #0 Chip Select 2	O	17	
SPI0-CS3	Serial Peripheral Interface #0 Chip Select 3	O	18	
SPI0-CLK	Serial Peripheral Interface #0 Clock	I/O	14	
SPI0-MISO	Serial Peripheral Interface #0 Master In / Slave Out	I/O	15	
SPI0-MOSI	Serial Peripheral Interface #0 Master Out / Slave In	I/O	13	
SPI1-CS1	Serial Peripheral Interface #1 Chip Select 1	O		18
SPI1-CS2	Serial Peripheral Interface #1 Chip Select 2	O		19
SPI1-CS3	Serial Peripheral Interface #1 Chip Select 3	O		20
SPI1-CLK	Serial Peripheral Interface #1 Clock	I/O		17
SPI1-MISO	Serial Peripheral Interface #1 Master In / Slave Out	I/O		15
SPI1-MOSI	Serial Peripheral Interface #1 Master Out / Slave In	I/O		16
RF1	Synchronous Serial Controller #1 Receive Frame Sync	I/O	32	
RK1	Synchronous Serial Controller #1 Receive Clock	I/O	34	
RD1	Synchronous Serial Controller #1 Receive Data	I	36	
TD1	Synchronous Serial Controller #1 Transmit Data		35	
TF1	Synchronous Serial Controller #1 Transmit Frame Sync		31	
TK1	Synchronous Serial Controller #1 Transmit Clock		33	
TWCK	Two Wire Bus (I ² C-Bus) Clock	OD, PU 2k7		12
TWD	Two Wire Bus (I ² C-Bus) Data	OD, PU 2k7		11

(Connector Pin Description continued)

Mnemonic	Description	Type	Pin on X21	Pin on X22
DRXD	Debug UART Receive (Console Port)	I	11	
DTXD	Debug UART Transmit (Console Port)	O	12	
RXD0	USART #0 Receive	I		9
TXD0	USART #0 Transmit	O		6
SCK1	USART #1 Clock	I/O		3
CTS1	USART #1 CTS	I	8	
DCD1	USART #1 DCD	I	9	
DSR1	USART #1 DSR	I	2	
DTR1	USART #1 DTR	O	6	
RI1	USART #1 RI	I	3	
RTS1	USART #1 RTS	I	7	
RXD1	USART #1 Receive	I	4	
TXD1	USART #1 Transmit	O	5	
SCK2	USART #2 Clock	I/O		2
CTS2	USART #2 CTS	I		8
RTS2	USART #2 RTS	I		7
RXD2	USART #2 Receive	I		4
TXD2	USART #2 Transmit	O		5
USB D-	USB Device Port Data -	Analog I/O	25	
USB D+	USB Device Port Data +	Analog I/O	26	
USB CNX	USB Device V_{BUS} (5V) Monitoring	Input	27	
USB HA-	USB Host Port A Data -	Analog I/O	21	
USB HA+	USB Host Port A Data +	Analog I/O	22	
USB HB-	USB Host Port B Data -	Analog I/O	23	
USB HB+	USB Host Port B Data +	Analog I/O	24	



Bemaßung Bohrungen

10. DC Characteristics

DC Characteristics

Ambient temperature 25°C, unless otherwise indicated.

Symbol	Description	Parameter	Min.	Typ.	Max.	Unit
V _{cc}	Operating Voltage		3.0	3.3	3.6	V
V _{res}	Reset Threshold			2.9		V
t _{res}	Duration of Reset Pulse		150		280	ms
V _{IH}	High-Level Input Voltage		2		V _{cc} +0.3	V
V _{IL}	Low-Level Input Voltage		-0.3		0.8	V
I _{cc}	Operating current in normal operation			65		mA
		max		110		mA
V _{batt}	Battery Voltage for RTC		2.0	3	V _{cc}	V
I _{batt}	Battery current with operating voltage turned off	Battery Voltage = 3V Ambient temp. = 25°C		5		μA
		Ambient temp. = 70°C			17	μA
		Ambient temp. = 85°C			22	μA

Clocks Characteristics

Symbol	Description	Dependency	Admissible Range or Tolerance	Typical Value.	Unit
MAINCK	Main Oscillator frequency			18.4320	MHz
SLCK	Slow Clock			32768	Hz
PLLACK	PLLA Clock	= MAINCK * 13		239.616	
PCK	Processor Clock	= PLLACK		239.616	MHz
MCK	Master Clock	= PCK / 2		119.808	MHz
SDCK	SDRAM Clock	= MCK		119.808	
BCK	Baudrate Clock	= MCK / 65	1.5%	1.84320	MHz
LCDCK	LCD Dot Clock				
	Sharp LQ035Q7DH03	= MCK / 25	4.5..6.8	4.7923	MHz
	EDT ET035005DM6	= MCK / 19		6.3057	MHz
PLLBACK	PLLB Clock	= MAINCK / 14*73	0,25%	96.110	MHz
USBCK	USB Clock	= PLLBACK / 2		48.055	MHz

11. Stamp9261 Pin Assignment

I/O Interface B 1-50. 100pol. Hirose FX8					
1		VCC		VCC	2
3	Reserved			Reserved	4
5	Reserved			Reserved	6
7	Reserved			Reserved	8
9	LCDVSYNC/PB0	PB00		PB01 LCDHSYNK/PB1	10
11	LCDDOTCK/PCK0/PB2	PB02		PB03 BMS/LCDDEN/PB3	12
13	LCDD1/LCDD2/PB4	PB04		PB05 LCDD0/LCDD3/PB5	14
15	LCDD1/LCDD4/PB6	PB06		PB07 LCDD2/LCDD5/PB7	16
17	LCDD3/LCDD6/PB8	PB08		PB09 LCDD4/LCDD7/PB9	18
19	LCDD5/LCDD10/PB10	PB10		PB11 LCDD6/LCDD11/PB11	20
21	LCDD7/LCDD12/PB12	PB12		PB13 LCDD8/LCDD13/PB13	22
23	LCDD9/LCDD14/PB14	PB14		PB15 LCDD10/LCDD15/PB15	24
25		GND		GND	26
27	LCDD11/LCDD19/PB16	PB16		PB17 LCDD12/LCDD20/PB17	28
29	LCDD13/LCDD21/PB18	PB18		PB19 LCDD14/LCDD22/PB19	30
31	LCDD15/LCDD23/PB20	PB20		PB21 TF0/LCDD16/PB21	32
33	TK0/LCDD17/PB22	PB22		PB23 TD0/LCDD18/PB23	34
35	RD0/LCDD19/PB24	PB24		PB25 RK0/LCDD20/PB25	36
37	RF0/LCDD21/PB26	PB26		PB27 SPI1_NPCS1/LCDD22/PB27	38
39	SPI1_NPCS0/LCDD23/PB28	NPCS0		SPCK SPI1_SPCK/IRQ2/PB29	40
41	SPI1_MISO/IRQ1/PB30	MISO		MOSI SPI1_MOSI/PCK2/PB31	42
43	PA24/TPK8/SPI1_NPCS1	NPCS1		NPCS2 PA25/TPK9/SPI1_NPCS2	44
45	PA26/TPK10/SPI1_NPCS3	NPCS3		PA3 PA3/SPI0_NPCS0	46
47	PA7/TWD/PCK0	TWD		TWCK PA8/TWCK/PCK1	48
49		GND		GND	50
51		VCC		VCC	52
53	TXD1/NCS6/PC12	TXD1		RDX1 RXD1/NCS7/PC13	54
55	PA12/TCLK/RTS1	RTS1		CTS1 PA13/TPS0/CTS1	56
57	PA28/TPK12/SPI0_NPCS2	DTR1		DSR1 PA27/TPK11/SPI0_NPCS1	58
59	PA29/TPK13/SPI0_NPCS3	DCD1		RI1 PA23/TPK7/RTS0	60
61	TXD0/PCK2/PC8	TXD0		RXD0 RXD0/PCK3/PC9	62
63	RTS0/SCK0/PC10	RTS0		CTS0 CTS0/FIQ/PC11	64
65	TXD2/SPI1_NPCS2/PC14	TXD2		RXD2 RXD2/SPI1_NPCS3/PC15	66
67	PA15/TPS2/RTS2	RTS2		CTS2 PA16/TPK0/CTS2	68
69	PA10/DTXD/PCK3	DTXD		DRXD PA9/DRXD/PCK2	70
71	PA11/TSYNK/SCK1	SCK1		SCK2 PA14/TPS1/SCK2	72
73	PA17/TPK1/TF1	TF1		RF1 PA22/TPK6/RF1	74
75	PA18/TPK2/TK1	TK1		RK1 PA21/TPK5/RK1	76
77	PA19/TPK3/TD1	TD1		RD1 PA20/TPK4/RD1	78
79	PA1/SPI0_MOSI/MCCDA	MCCDA		MCCK PA2/SPI0_SPCK/MCCK	80
81	PA0/SPI0_MISO/MCDA0	MCDA0		MCDA1 PA4/SPI0_NPCS1/MCDA1	82
83	PA5/SPI0_NPCS2/MCDA2	MCDA2		MCDA3 PA6/SPI0_NPCS3/MCDA3	84
85	HDMA	HDMA		HDPB HDPB	86
87	HDMA	HDMA		HDPB HDPB	88
89	DDM	DDM		DDP DDP	90
91		GND		GND	92
93	Reserved	ELED_L		ELED_S Reserved	94
95	Reserved	ETX+		ETX- Reserved	96
97	Reserved	ERX+		ERX- Reserved	98
99	Reserved	EVCC		EGND Reserved	100

Bus Interface 1-50. 100pol. Hirose FX8						
1		VCC		VCC		2
3	NBS0/A0	A00		A01	NWR2/NBS2/A1	4
5	A2	A02		A03	A3	6
7	A4	A04		A05	A5	8
9	A6	A06		A07	A7	10
11	A8	A08		A09	A9	12
13	A10	A10		A11	A11	14
15	A12	A12		A13	A13	16
17	A14	A14		A15	A15	18
19	BA0/A16	A16		A17	BA1/A17	20
21	A18	A18		A19	A19	22
23	A20	A20		A21	A21/NANDCLE	24
25	A22/NANDALE	A22		A23	PA30/TPK14/A23	26
27	PA31/TPK15/A24	A24		A25	A25/CFRNW/PC3	28
29		GND		GND		30
31	Reserved				Reserved	32
33	Reserved				Reserved	34
35	NCS0	NCS0		NCS1	SDCS/NCS1	36
37	NCS2	NCS2		NCS3	NANDCS/NCS3	38
39	NCS4/CFCS0/PC4	NCS4		NCS5	NCS5/CFCS1/PC5	40
41	NANDOE/NCS6/PC0	NCS6		NCS7	NANDWE/NCS7/PC1	42
43	CFOE/NRD	NRD		NWR0	CFWE/NWE/NWR0	44
45	CFIOR/NBS1/NWR1	NWR1		NWR3	CFIOW/NBS3/NWR3	46
47	CFCE1/PC6	CFCE1		CFCE2	CFCE2/PC7	48
49		GND		GND		50
51		VCC		VCC		52
53	D0	D00		D01	D1	54
55	D2	D02		D03	D3	56
57	D4	D04		D05	D5	58
59	D6	D06		D07	D7	60
61	D8	D08		D09	D9	62
63	D10	D10		D11	D11	64
65	D12	D12		D13	D13	66
67	D14	D14		D15	D15	68
69		GND		GND		70
71	D16/TCLK0/PC16	D/PC16		D/PC17	D17/TCLK1/PC17	72
73	D18/TCLK2/PC18	D/PC18		D/PC19	D19/TIOA0/PC19	74
75	D20/TIOB0/PC20	D/PC20		D/PC21	D21/TIOA1/PC21	76
77	D22/TIOB1/PC22	D/PC22		D/PC23	D23/TIOA2/PC23	78
79	D24/TIOB2/PC24	D/PC24		D/PC25	D25/TF2/PC25	80
81	D26/TK2/PC26	D/PC26		D/PC27	D27/TD2/PC27	82
83	D28/RD2/PC28	D/PC28		D/PC29	D29/RK2/PC29	84
85	D30/RF2/PC30	D/PC30		D/PC31	D31/PCK1/PC31	86
87	SHDN	SHDN		WKUP	WKUP	88
89	NRST	NRST		VBATT	VDDBU	90
91	RTCK	RTCK		NWAIT	NWAIT/IRQ0/PC2	92
93	NTRST	NTRST		JTAGSEL	JTAGSEL	94
95	TDI	TDI		TMS	TMS	96
97	TDO	TDO		TCK	TCK	98
99		GND		GND		100

13. Stamp9261 Dimensions

