Logic Analyzer Option

DS2-8LA and DS2-16A

ISO-9001 CERTIFIED MANUFACTURER   **GW INSTEK**

OVERVIEW

The DS2-8LA and the DS2-16LA Logic Analyzer options allow the GDS-2000A to be upgraded to a powerful mixed signal oscilloscope. These options include both parallel and serial bus (UART, SPI, I²C) triggering and decoding as well as powerful logic triggering.

The Logic Analyzer options also take advantage of the GDS-2000í s segmented memory, search, automatic measurements, cursor functionality and the exceptional 2M record length.

Main Features

Option	Channels	Bandwidth
DS2-16LA	16	200MHz
DS2-8LA	8	200MHz

Features	• 500MSa/s sample rate.
	• 200MHz bandwidth.
	• Parallel bus triggering.
	• Serial bus triggering (UART, SPI, I²C).
	• 2M record length.

Logic Analyzer Software Features	• Group channels.
	• Custom threshold levels for each group of digital channels.
	• Analog waveform function.
	• Labels.

Package Contents and Accessories

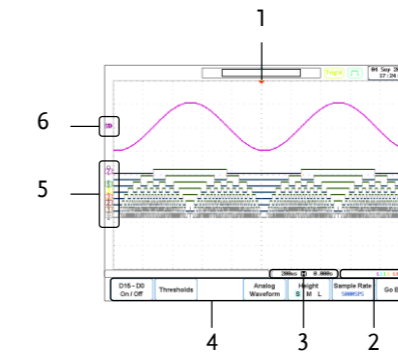### Standard Accessories for DS2-8LA

Item	Part Number
8-Channel Logic Analyzer Probe	GTL-08LA
8-Channel Logic Analyzer Card	GLA-08

Standard Accessories for DS2-16LA

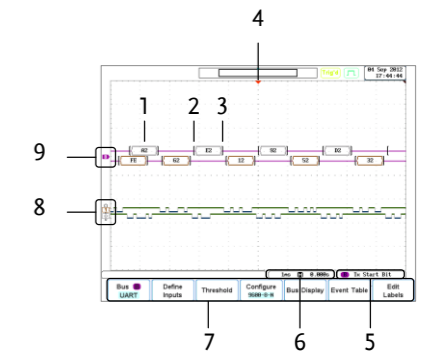| Item	Part Number
16-Channel Logic Analyzer Probe	GTL-16LA
16-Channel Logic Analyzer Card	GLA-16

Display Overview

Logic Analyzer Display Overview

Description

1. Horizontal Position
2. Trigger Status
3. Horizontal Status
4. Bottom Menu
5. Digital Channel/Bus Indicators
6. Analog Waveform Indicator

Bus Display Overview

Description

1. Bus Data
2. Start Bit
3. Stop Bit
4. Horizontal Position
5. Trigger Status
6. Horizontal Status
7. Bottom Menu
8. Digital Channel Indicators
9. Bus Indicator

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Setting up the Oscilloscope

This section describes how to set up the oscilloscope properly including installing the logic analyzer cards, using the logic analyzer probes and how to access the functions that are included with the logic analyzer option.

Installing Logic Analyzer Cards

The logic analyzer modules need to be installed into the module slots on the rear panel.

Do not insert or remove the modules with the power on.

1. Slide the tabs holding the module cover to the unlock position and then remove.

2. Install the optional module. Be sure to make sure that the groves on the module line-up to the slots in the module bay.
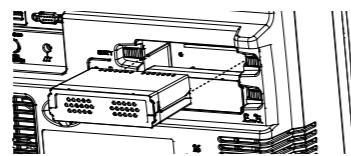
3. Slide the locking mechanisms back to the locked position.

4. Turn on the GDS-2000A.

5. The GDS-2000A is now ready to operate

Using the Logic Analyzer Probes

This section will describe how to connect the digital channels to the device under test. To use the digital channels the optional logic analyzer module must be installed.

1. Turn the DUT off to protect it from being short circuited when the probes are attached.

2. Insert the Logic Analyzer probe into the Logic Analyzer input.
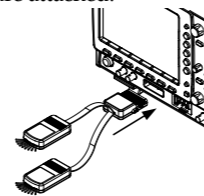
3. Connect the ground lead (black) from the logic analyzer probe to the circuit ground on the DUT.

4. Connect another probe lead to a point of interest on the circuit. Make note of which probe lead is connected to which point.

5. Repeat step 4 with any remaining probes.
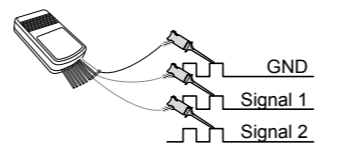
Accessing the Logic Analyzer Menu

The Logic Analyzer menu can be accessed using the Option key.

1. Press the [Option] key and select *Logic Analyzer* to access the Logic Analyzer menu.

2. Press the *D15~D0 On/Off* soft-key to activate the digital channels.

   • The position of each channel can be set in this menu.

   • Channels can be grouped in this menu.

3. Press *Thresholds* to set the thresholds.

   • Thresholds can be individually set for every 4 digital channels. I.e., D0~D3, D4~D7 and so on.

   • There are 5 pre-set threshold levels in addition to the User-defined threshold setting (TTL, 5.0V CMOS, 3.3V CMOS, 2.5V CMOS, ECL, PECL, 0V).

4. Press *Analog Waveform* to display an analog waveform of the digital channels.

   • Analog waveforms can be created from either the D0~D7 or D8~D15 digital channels.

   • Only one analog waveform can be displayed at a time.

5. Press the *Height* soft-key to toggle the scale of the digital channels.

Using the Bus Key

The Bus key configures the UART, SPI, I²C or Parallel buses.

1. Press the [BUS B] key to access the Bus menu and to display the bus on the display.

   • Only those digital channels that have been activated from the Logic Analyzer menu will be accessible from the Bus menu.

   • Pressing the *Bus* key again will remove the bus from the display.

UART Bus

The UART bus menu is designed to decode RS-232 and other common RS-232 variants such as RS-422 and RS-485.

1. Press the *Bus* soft-key and select UART.

2. Press *Define Inputs* to select the Tx and Rx inputs as well as the signal polarity.

3. Press *Thresholds* to set the thresholds.

   • There are 5 pre-set threshold levels in addition to the User-defined threshold setting (TTL, 5.0V CMOS, 3.3V CMOS, 2.5V CMOS, ECL, PECL, 0V).

4. Press the *Configure* to set the baud rate, data bits, parity and packet settings.

5. Press *Bus Display* to configure how the data is displayed, either hex or binary.

6. Press *Event Table* to view or save the decoded data in a list.

7. Press *Edit Labels* to create an on-screen label for the bus.

I²C Bus

The I2C bus is a 2 wire interface with a serial data line (SDA) and serial clock line (SCLK). The I2C protocol supports 7 or 10 bit addressing and multiple masters.

1. Press the *Bus* soft-key and select I²C.

2. Press *Define Inputs* to select the SCLK and SDA inputs.

3. Press *Thresholds* to set the thresholds.

    - There are 5 pre-set threshold levels in addition to the User-defined threshold setting (TTL, 5.0V CMOS, 3.3V CMOS, 2.5V CMOS, ECL, PECL, 0V).

4. Press the *Include R/W in Address* soft-key to set whether a read/write bit is included in the address.

5. Press *Bus Display* to configure how the data is displayed, either hex or binary.

6. Press *Event Table* to view or save the decoded data in a list.

    - The *Data Detail* option allows you to also view the data at a particular address. This is only for I²C buses.

7. Press *Edit Labels* to create an on-screen label for the bus.

SPI Bus

The serial peripheral interface (SPI) is a full duplex 4 wire synchronous serial interface. The word size is configurable from 4 to 32 bits. The SPI bus triggers on the data pattern at the start of each framing period.

1. Press the *Bus* soft-key and select SPI.

2. Press *Define Inputs* to select the SCLK, SS, MOSI and MISO inputs.

3. Press Thresholds to set the thresholds.

    - There are 5 pre-set threshold levels in addition to the User-defined threshold setting (TTL, 5.0V CMOS, 3.3V CMOS, 2.5V CMOS, ECL, PECL, 0V).

4. Press *Configure* to set the data line logic level, SCLK edge polarity, word size and bit order.

5. Press *Bus Display* to configure how the data is displayed, either hex or binary.

6. Press *Event Table* to view or save the decoded data in a list.

7. Press *Edit Labels* to create an on-screen label for the bus.

Parallel Bus

The digital channels can be configured as a parallel bus. The number of bits that define the bus as well as which bit is used as the bus clock can also be configured.

1. Press the *Bus* soft-key and select Parallel.

2. Press *Define Inputs* to select the number of bits to use in the parallel bus, which digital channels are set to which bits in the parallel bus and which bit, if any, is used for a clock signal.

3. Press *Thresholds* to set the thresholds.

    - There are 5 pre-set threshold levels in addition to the User-defined threshold setting (TTL, 5.0V CMOS, 3.3V CMOS, 2.5V CMOS, ECL, PECL, 0V).

    - Thresholds can be set for each 4 lots of digital channels, i.e., D0~D3, D4~D7 and so on.

4. Press *Bus Display* to configure how the data is displayed, either hex or binary.

5. Press *Event Table* to view or save the decoded data in a list.

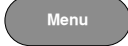6. Press *Edit Labels* to create an on-screen label for the bus.

Trigger Settings

The Logic Analyzer option adds Bus and Logic triggers to the GDS-2000A.

Note that the digital channels can also be set as the source for the traditional Edge and Pulse Width triggers, but will not be covered here as the operation is covered in the user manual.

Logic Trigger Settings

The digital channels can be set up to trigger on specified logic levels and for a specified clock edge.

1. Press the trigger [Menu] key and select *Type* > *Others* > *Logic*.

2. Press *Define Inputs* to set the digital logic to trigger on.

    - Only 1 bit can be set as the clock bit.

    - The digital logic will be reflected in the *Trigger Status* icon under the graticule.

3. Press *When* to configure the triggering conditions for the logic that was defined in the Define Inputs menu.

    - The scope can be configured to trigger when the defined logic is true or false.

    - The trigger timing for when the selected logic is true can also be configured.

4. Press *Thresholds* to set the thresholds.

    - There are 5 pre-set threshold levels in

addition to the User-defined threshold setting (TTL, 5.0V CMOS, 3.3V CMOS, 2.5V CMOS, ECL, PECL, 0V).

- Thresholds can be set for each 4 lots of digital channels, i.e., D0~D3, D4~D7 and so on.

5. Press *Clock Edge* to set the transition for the selected clock edge, if any.

6. Press *Mode* to select either Auto (untriggered roll) or Normal triggering modes.

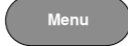7. Press *Holdoff* to set the hold off time.

Bus Trigger Settings -UART

The digital channels can be set up to trigger on UART specific conditions.

1. Configure the *Bus* key to UART.

    - The UART option needs to be set in the Bus menu *first* before the UART trigger settings can be configured.

2. Press the trigger [Menu] key and select *Type* > *Others* > *Bus*.

3. Press *Trigger On* to set triggering conditions.

    - There are 8 UART triggering conditions: Tx, Start Bit, Rx Start Bit, Tx End of Packet,, Rx End of Packet, Tx Data, Rx Data, Tx Parity Bit, Rx Parity Bit.

4. If *Tx Data* or *Rx Data* was selected, press *Data* to configure what data to trigger on.

Bus Trigger Settings –I²C

The digital channels can be set up to trigger on I²C specific conditions.

1. Configure the *Bus* key to I²C.

    - The I²C option needs to be set in the Bus menu *first* before the I²C trigger settings can be configured.

2. Press the trigger [Menu] key and select *Type* > *Others* > *Bus*.

3. Press *Trigger On* to set triggering conditions.

    - There are 7 I²C triggering conditions: Start, Repeat Start, Stop, Missing Ack, Address, Data, Data/Address.

4. If *Data* or *Data/Address* was selected as the trigger condition, press *Data* to configure what data to trigger on.

5. If *Address* or *Data/Address* was selected as the trigger condition, press *Address* to configure the address and the addressing mode to trigger on.

    - An address preset can also be chosen if *Address* was selected as the trigger condition. This option is not available for the *Data/Address* triggering condition.

    Press *Direction* to configure read/write direction.

6. Press *Mode* to select either Auto (untriggered roll) or Normal triggering modes.

S PECIFICATIONS

Logic Analyzer

Sample Rate	500MSa/s
Bandwidth	200MHz
Record Length	2M max
Input Channels	16 Digital (D15 - D0) or 8 Digital (D7~D0)
Trigger type	Edge, Pattern, Pulse Width, Serial bus (I2C, SPI, UART)
Thresholds	Quad-D0~D3, D4~D7 . . . Thresholds
Threshold selections	TTL, CMOS, ECL, PECL, User Defined
User-defined Threshold Range	±10V
Maximum Input Voltage	±40V
Minimum Voltage Swing	±500mV
Vertical Resolution	1 bit