# PIC16(L)F1512/1513 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F1512/1513 family devices that you have received conform functionally to the current Device Data Sheet (DS41624**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1512/1513 silicon.

| **Note:** | This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**). |
|---|---|

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

| **Note:** | If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance. |
|---|---|

The DEVREV values for the various PIC16(L)F1512/1513 silicon revisions are shown in Table 1.

**TABLE 1: SILICON DEVREV VALUES**

| Part Number | DEVICE ID<13:0>(1),(2) | | |
|---|---|---|---|
| | DEV<8:0> | REV<4:0> Silicon Revision | |
| | | A1 | A2 |
| PIC16F1512 | 01 0111 000 | 0 0001 | 0 0010 |
| PIC16LF1512 | 01 0111 001 | 0 0001 | 0 0010 |
| PIC16F1513 | 01 0110 010 | 0 0001 | 0 0010 |
| PIC16LF1513 | 01 0111 010 | 0 0001 | 0 0010 |

**Note 1:** The Device ID is located in the configuration memory at address 8006h.

**2:** Refer to the *"PIC16(L)F151X/152X Memory Programming Specification"* (DS41442) for detailed information on Device and Revision IDs for your specific device.

**TABLE 2: SILICON ISSUE SUMMARY**

| Module | Feature | Item Number | Issue Summary | Affected Revisions(1) | |
|---|---|---|---|---|---|
| | | | | A1 | A2 |
| Oscillator | Clock Switching | 1.1 | Clock switching can cause a single corrupted instruction. | X | |
| Oscillator | Oscillator Start-up Timer (OST) bit | 1.2 | OST bit remains set. | X | |
| ADC | ADOUT Function | 2.1 | ADOEN bit issue during ADOUT function. | X | |
| ADC | Automated CVD | 2.2 | Cannot run back-to-back conversions using FRC. | X | X |
| ADC | TRIS Control during conversions | 2.3 | No auto TRIS control, must be done manually. | X | |
| Program Flash Memory (PFM) | PFM Self Write | 3.1 | PFM self write will not work depending on clock selection. | | X |
| Fixed Voltage Reference (FVR) | Gain Amplifier Output | 4.1 | Use of FVR module can cause device Reset. | X | X |
| Fixed Voltage Reference (FVR) | FVR Output Levels | 4.2 | Large errors are possible. | X | |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

## Silicon Errata Issues

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

## 1. Module: Oscillator

### 1.1 Clock Switching

When switching clock sources between INTOSC clock source and an external clock source, one corrupted instruction may be executed after the switch occurs.

**Work around**

When switching from an external oscillator clock source, first switch to 16 MHz HFINTOSC. Once running at 16 MHz HFINTOSC, configure IRCF to run at desired internal oscillator frequency.

When switching from an internal oscillator (INTOSC) to an external oscillator clock source, first switch to HFINTOSC High-Power mode (16 MHz). Once running from HFINTOSC, switch to the external oscillator clock source.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 1.2 Oscillator Start-up Timer (OST) bit

During the Two-Speed Start-up sequence, the OST is enabled to count 1024 clock cycles. After the count is reached, the OSTS bit is set, the system clock is held low until the next falling edge of the external crystal (LP, XT or HS mode), before switching to the external clock source.

When an external oscillator is configured as the primary clock and Fail-Safe Clock mode is enabled (FCMEN = 1), any of the following conditions will result in the Oscillator Start-up Timer (OST) failing to restart:

- $\overline{\text{MCLR}}$ Reset
- Wake from Sleep
- Clock change from INTOSC to Primary Clock

This anomaly will manifest itself as a clock failure condition for external oscillators which take longer than the clock failure time-out period to start.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 2. Module: ADC

### 2.1 ADOEN Bit Issue During ADOUT Function

To operate the ADC during the pre-charge stage of conversion as stated in the data sheet, the ADOUT output-override must be disabled (ADOOEN = 0) when the ADOUT pin is not connected to the ADC conversion bus (ADOEN/ADOLEN = 0). Likewise, the ADOUT output-override should be enabled (ADOOEN = 1) when ADOUT is enabled (ADOEN/ ADOLEN = 1).

**Work around**

Stated above.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 2.2 Automated CVD

The double conversion procedure for the ADC is activated by setting the ADDSEN bit in the AADCON3 register. Double conversions do not work reliably if the FRC is selected as the ADC clock source. This is true whether or not the part is in Sleep mode. Single conversions can be performed, in Sleep mode or not, with the FRC selected.

**Work around**

Do not run double conversions with the FRC selected as the clock for the ADC.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 2.3 TRIS Control During Conversions

When running conversions using the acquisition timer feature, the TRIS control for the selected analog pin will not be automatically set to '1' if its current value is '0'. This will cause the charge on the ADC hold capacitor to be driven to $V_{SS}$ or $V_{DD}$. However, if the selected analog pin's current TRIS value is '1', the pre-charge timer will correctly override it to an output during the pre-charge stage.

**Work around**

Set the TRIS bit (TRISx = 1) to configure the pin as a digital input before starting the ADC conversion. When the conversion completes, the TRIS bit can be cleared (TRISx = 0) to return the pin as a digital output.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 3. Module: Program Flash Memory (PFM)

### 3.1 PFM Self Write

Writes to the PFM will not execute if the device's clock source is HS or ECH, or if the internal oscillator is at 16 MHz.

**Work around**

To write to the PFM, the clock source must have one of the following settings: internal oscillator set to 8 MHz or lower, ECM, ECL, XT, External RC, LP or T1OSC.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| | X | | | | | | |

## 4. Module: Fixed Voltage Reference (FVR)

### 4.1 Gain Amplifier Output

When using the FVR module, if the gain amplifier outputs are set via the CDAFVR or ADFVR bits in FVRCON, while the module is disabled (FVREN = 0), the internal oscillator frequency may shift, device current consumption can increase, and a Brown-out Reset may occur.

**Work around**

Set the FVREN bit of FVRCON to enable the module prior to adjusting the amplifier output selections with the CDAFVR and ADFVR bits. If switching from the 4x output setting to the 1x output setting, select the 2x output setting as an intermediary step. Always set the amplifier output selections to off ('00') before disabling the FVR module.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 4.2 FVR Output Levels

The output levels of the FVR are likely to contain large errors that can exceed 30% of the 1.024/ 2.048/4.096V target levels stated in the Electrical Specifications section of the data sheet.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41624**B**):

| | |
|---|---|
| **Note:** | Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity. |

### 1. Module: Electrical Specifications

#### 25.8 AC Characteristics

Outdated Freq. Tolerance range, ±4% to -12%, has been removed. In the Conditions column, VDD range changed from 2.0V to 1.8V for –11% to +7%. +/-4% frequency tolerance changed to -4% to +6%, +/-4 to -8% changed to -11% to +7%.

**TABLE 25-2: OSCILLATOR PARAMETERS**

| **Standard Operating Conditions (unless otherwise stated)**<br>Operating Temperature -40°C ≤ TA ≤ +125°C | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Freq. Tolerance** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| OS08 | HFOSC | Internal Calibrated HFINTOSC Frequency(1) | ±2% | — | 16.0 | — | MHz | 25°C; 3.2V |
| | | | –4% to +6% | — | 16.0 | — | MHz | 0°C ≤ TA ≤ +85°C<br>2.3V ≤ VDD ≤ 5.5V |
| | | | –11% to +7% | — | 16.0 | — | MHz | -40°C ≤ TA ≤ +125°C<br>**1.8V** ≤ VDD ≤ 5.5V |
| OS09 | LFOSC | Internal LFINTOSC Frequency | — | — | 31 | — | kHz | |
| OS10* | TIOSC ST | HFINTOSC Wake-up from Sleep Start-up Time | — | — | 3 | 8 | µs | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

## APPENDIX A: DOCUMENT REVISION HISTORY

### Rev A Document (03/2012)

Initial release of this document.

### Rev B Document (08/2012)

Added MPLAB X IDE; Added Silicon Revision A2; Updated Modules 1.2 and 2.2; Added Module 3, Program Flash Memory, and Module 4, Fixed Voltage Reference.

Data Sheet Clarifications: Added Module 1, Electrical Specifications.

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