SENSIRION
THE SENSOR COMPANY

Application Note: ESD, Latch-Up and EMC

For SHTxx Humidity and Temperature Sensors

Introduction

SHTxx humidity and temperature sensors (i.e. the whole humidity and temperature sensor family of Sensirion) are qualified with respect to ESD (Electrostatic Discharge) and Latch-up compliant with JESD 22 – A114, MIL Standard 883[E] and JEDEC78 Standard. All tests were successfully passed what indicates, that the sensors are well protected against electronic impact.

Due to its micro-integration and digital interface, supported by a CRC checksum, SHTxx sensors benefit from superior functional immunity against electro-magnetic immission (EMI) originated by e.g. mobile phones, machinery and other RF radiating devices.

This application note elaborates on ESD and Latch-up and provides an insight into the protection circuits of the SHTxx sensor. In case improved ESD protection is required an example of additional external ESD protection is suggested. In addition, information on electromagnetic compatible (EMC) design with the sensor is given.

ESD Protection

Electrostatic discharge (ESD) may damage SHTxx sensors as they consist of integrated circuits. Therefore, the sensors contain state of the art built-in ESD protection circuits on all pins. Functional schematics of ESD protection circuits are displayed in Fig. 1.

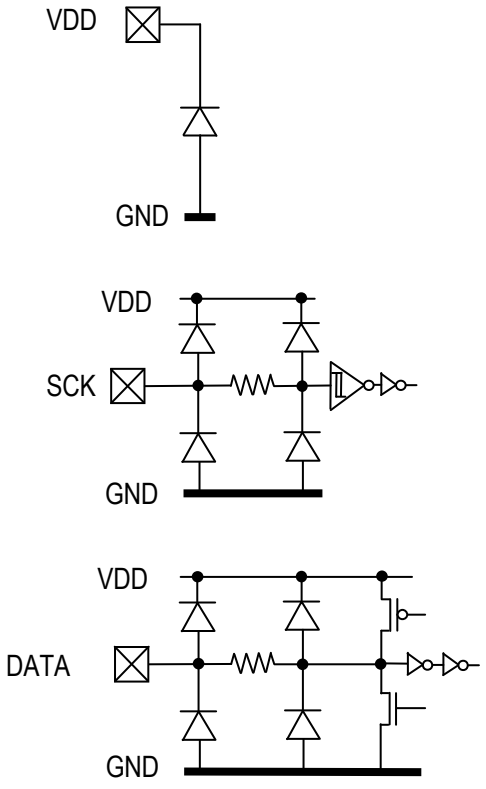

Figure 1 Functional schematic of ESD protection circuits for the pads VDD (top panel), SCK (middle panel) and DATA (bottom panel).

The sensors are tested using Human Body Model at 2kV (according to JESD 22 – A114, MIL Std 883[E]). The test circuit and waveforms are shown in Figure 2.

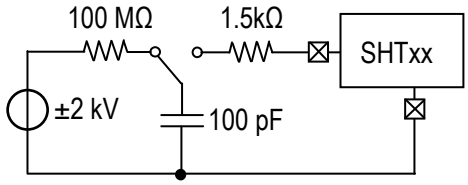

Figure 2 Human-Body Model Test Circuit. The 100pF capacitor simulates the capacitance of the human body, the 1.5 kΩ value of the discharge resistor the internal resistance of the human body. The Voltage is applied in pulses of 0.1us, positive and negative.

ESD stress test was performed using TMT Verifier II s/n 1042049 equipment according to table below:

Stress Level	Stressed Pin	Reference	Polarity
2 kV	SCK	GND	3 positive pulses then 3 negative pulses
	DATA	GND	
	SCK	VDD	
	DATA	VDD	
	GND	VDD	
	SCK	DATA	

Table 1 Summary pg the tested configurations

SHTxx sensors successfully pass the Human-Body Model test. For details please contact Sensirion. With regards to ESD protection no further tests have been performed, i.e. such with higher voltages and other models (Machine Model, Charged Device Model, Charged-Cable Model, etc.). The Human-Body Model test is well accepted in the industry and confirms that SHTxx sensors are well protected for applications and handling with normal precautions.

In case of extreme discharge protection requirements an additional protection circuit according may be implemented – compare Figure 3.

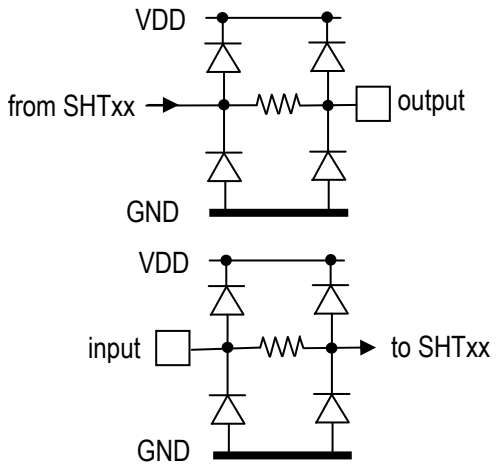

Figure 3 Additional external protection circuits for SHTxx sensors (For protection against extreme electrostatic energy, above 100 µWs).

Latch-Up

Isolation between individual diodes, transistors and capacitors on an integrated circuit is achieved by reverse-biased PN junctions. These junctions form NPN and PNP structures with adjacent junctions which result in parasitic thyristors. These parasitic thyristors may be undesirably triggered in various ways:

- In case there is a voltage at the input or output of the sensor, which is more positive than the supply or more negative than the ground connection, current flows into the gate of the parasitic thyristor. If the amplitude and duration of the current are above a certain value the thyristor is triggered. At long lines (several meters) and overshoots the probability of triggering the thyristor must be taken into account.
- An electrostatic discharge can trigger the parasitic thyristor. Even if the duration of an electrostatic discharge is only a few tens of nanoseconds long the complete chip may be flooded with charge carries. These carriers then flow off slowly resulting in triggering the thyristor.
- Eventually the parasitic thyristor may be triggered by a high supply voltage – however it must be by far higher than the value given in the datasheet.

Although these conditions violate the specification given in the SHTxx datasheets, they may occur during uncontrolled events. The sensor was designed to comply with state-of-the-art precautions to reduce the thyristors sensitivity to the maximum, and hence to avoid latch-up in all above mentioned situations.

In order to verify the latch-up immunity the SHTxx sensor has been tested according to JEDEC Std 78 –

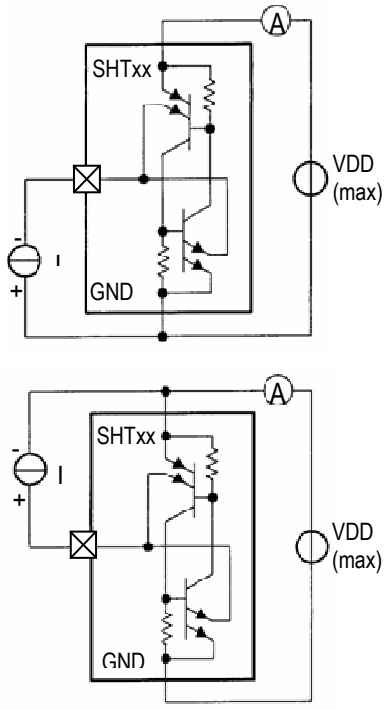

Figure 4 Latch-up test setup for respective pad and both positive and negative sign. The SHTxx is modeled here as a parasitic thyristor.

Figure 4 shows the test setup. The test was performed at 85°C using an ORYX 11000EX test system.

For that test a current I of ±100mA is injected at VDD (max) of 9V compliance. The supply current A is measured before and after the latch up trigger-pulse. In case no difference between the values is observed and functionality of the device has not degraded the test is successfully passed. The test has been performed between all pins of the SHTxx with positive result.

EMC Protection

The SHTxx sensors are designed to retain reliable functionality in demanding environments. Advantages are listed below:

- No external components (except the pull up resistor on the DATA line) are required. All susceptible circuit is integrated on the chip at micrometer scale making it inherently immune against RF radiation (originated for example by wireless devices).
- The pure digital interfacing of sensors allows for high S/N ratio on the SCK and DATA lines.
- The transmission frequency of the measurement data across SCK and DATA lines can be set arbitrarily low. Hence, the slopes of the signals can be filtered to minimize susceptibility against bursts.
- The CRC (cyclic redundancy check) allows for verifying whether the data transfer has properly been performed.

Sensirion recommends the following basic precautions when designing the circuit around the SHTxx sensors:

- A capacitor of 100nF must be used between VDD and GND as close as possible to the sensor (compare datasheets).
- For minimizing cross talk, SCK and DATA lines shall not run next to each other except a long ribbon cable or flat flexible cable is used.
- Reduce transmission frequency and slopes of the signals when using long cables. This is to reduce cross talk sensitivity, reflections and susceptibility against bursts. Slopes can be reduced by inserting a passive low pass filter, shown in Fig. 5. Best results may be achieved when using a low pass filter on either side of the cable connection.

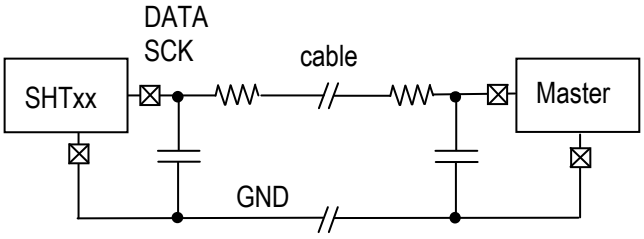

Figure 5 Reducing the slope of SCK of DATA line when using a long cable with the sensor.

Revision history

Date	Revision	Changes
17 October 2003	1.0	Initial release
25 May 2005	1.1	Changed main house address
03 October 2006	1.2	Sensirion Inc. address added
12 March 2009	1.3	Figure 5 changed, new format applied

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