Quick Start

AX_SPU

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Bearbeitungsstatus

Fachl. Version	Status	Name Bearbeiter	Art der Bearbeitung	Datum
1.0	Aab	Germersdorf	Ersterstellung	02/02/15

Mögliche Status = iA (in Arbeit)
Aab (Arbeit abgeschlossen)

Freigabestatus

Fachl. Version	Status	Freigegeben von (Name)	Bemerkungen	Datum

Mögliche Status = F (freigegeben)

Contents

1 Overview and board components

1.1 Board overview

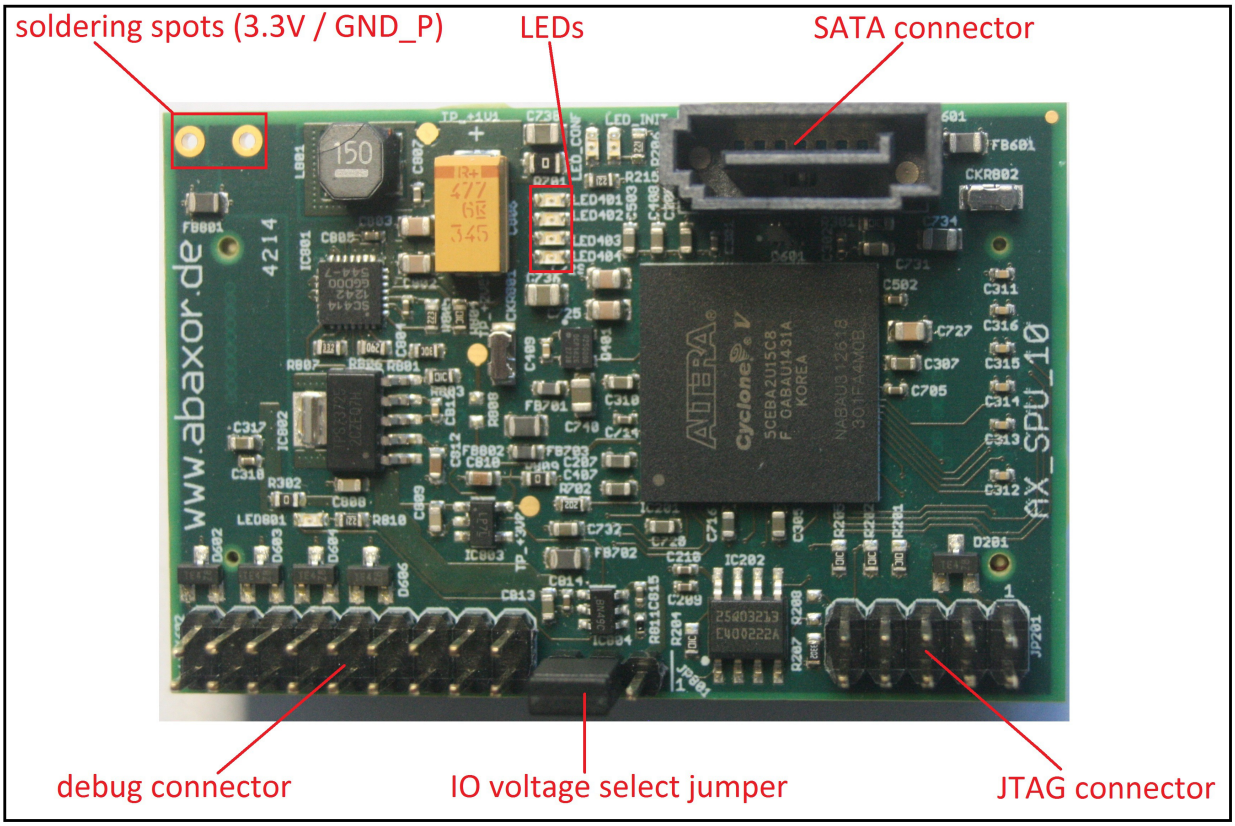

Figure 1: Board overview top

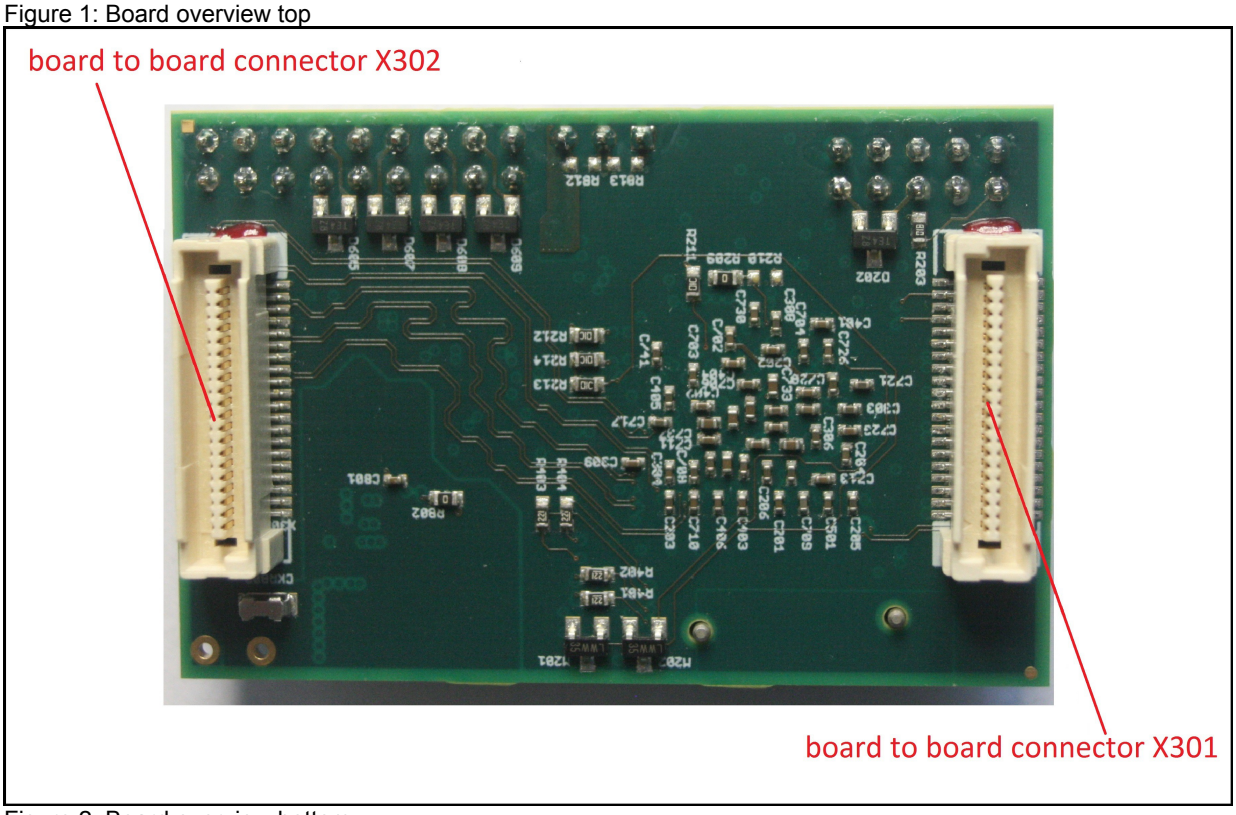

Figure 2: Board overview bottom

1.2 Processing unit

- Altera Cyclone V FPGA 5CEBA2U15 with 25 MHz clock
- Flash memory N25Q032A13ESC as FPGA configuration flash in active serial single device configuration AS x 4

1.3 IOs

- 36 single ended IOs, up to 6 differential RX and 6 TX pairs, up to 2 external clock inputs and 1 output on TE connectivity 5179031-1 board to board connectors (X301/ X302)
- 1 LVDS RX and 1 TX pair on SATA connector
- 16 IOs, 2,54 mm pin header (debug connector)

Signals	Function
LVDS_RX/ LVDS_RX_CLK	LVDS/ LVDS clock receive pair/ single ended IO
IO_T/ LVDS_TX_CLK	LVDS/ LVDS clock send pair/ single ended IO
IO	single ended IO

Table 1: Signal description

The IO voltage is accessible on the board-to-board connector it can be selected with a jumper.

I/O voltage	Jumper position
3.3 V (directly sourced from main supply)	 Pin 1 and 2 shorted
2.5 V (LDO sourced from main supply)	 Pin 2 and 3 shorted

Table 2: IO voltage select jumper

For further information concerning IO ressources refer to [CV-52005].

1.4 Further components

- 4 x LED
- Altera FPGA JTAG connector

1.5 Supply voltage and operating conditions

- 3.3 V (±5 %), TE connectivity 5179031-1 or soldering spot
- Temperature Range: Industrial (-40 .. +85 °C) or Commercial (0 .. +70 °C)

2 Getting started

2.1 Start Design

A small test project (/documentation/quickstart/AXSPU_test_fpga) is available for getting started.
You can use this project as a basis to develop your own application. In the test design all available board pins are used and the LEDs are toggled. The pinfile is located at AXSPU_test_top.qsf.

2.2 Required

- 3.3 V ± 5% power supply or Breakout board [AX_SPU_BO]
- Test Design (/documentation/quickstart/AXSPU_test_fpga)
- JTAG Programmer USB Blaster Download Cable [USB-DWLD_1] or [USB-DWLD_2]
- Altera Software Quartus II Web Edition (≥13.01) [QII5V1], [QII5V1_DWLD]

2.3 Steps to follow

1. Connect power to X302 (figure 2, ../documentation/hardware/schematic/AX_SPU_schematic.pdf) and connect the JTAG programmer to the board
2. Open the project file .../AXSPU_test_fpga/AXSPU_test_fpga.qpf in the quartus II software
3. Open the programmer (Tools/Programmer) and choose your programmer under Hardware Setup
4. The board can be programmed in JTAG mode:
   - to program the FPGA use the sof-file (.../AXSPU_test_fpga/output_files/AXSPU_test_top.sof)
   - to program the flash with JTAG indirect programming use the jic-file (.../AXSPU_test_fpga/output_files/AXSPU_test.jic). When the board is programmed repower the board. The design will now be loaded from the flash.
     The sof-file can be converted to a jic-file in the quartus II software (File/Convert programming file)
5. After the device is programmed the 4 debug LEDs start to toggle in ascending order

Further details: [AN-370], [QII5V1]

3 References

CV-52005: Altera, I/O Features in Cyclone V Devices, 2013.06.21

AX_SPU_BO: abaxor engineering, AX_SPU_BO Quickstart, 2015.02.02

USB-DWLD_1: Altera, Altera USB Blaster Download Cable, www.altera.com/products/devkits/kit-cables.html

USB-DWLD_2: Terasic, USB Blaster Download Cable Terasic Inc P0302, www.terasic.com.tw/cgi-bin/page/archive.pl?No=46

QII5V1: Altera, Quartus II Handbook Volume 1: Design and Synthesis, 2014.12.15

QII5V1_DWLD: Altera, Quartus II Web Edition, http://dl.altera.com/?edition=web

AN-370: Altera, Using the Altera Serial Flash Loader Megafunction with the Quartus II Software, 2014.08.18