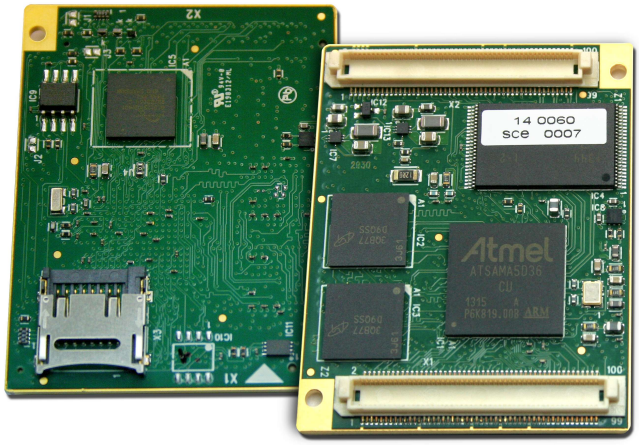

StampA5D3x/PortuxA5D3x

Technical Reference

StampA5D3x/PortuxA5D3x: Technical Reference

ZIM Zentrales Innovationsprogramm Mittelstand

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Table of Contents

List of Figures

List of Tables

1. Introduction

The StampA5D3x is intended to be used as a small size "intelligent" CPU module as well as a universal Linux CPU card. It can be used anywhere where restricted energy and space requirements play a role. The design of the StampA5D3x is limited to the processors core needs like DDRAM and Flash, thus giving the customer a wide-ranged choice of configurations of the peripherals and environment. Featuring an integrated LCD/ TFT and touch controller applications with graphical needs can be realized cost-efficient and individually.

The StampA5D3x has all the necessary interfaces to support a huge variety of peripheral devices.

Enhanced cryptographic options allow secure design with good performance. These include an encryption engine, a true random number generator, Atmel ® secure boot solution and an additional encryption chip for secure key generation and storage. All means for securing application and communication as well as prevent cloning and copying are available.

The ARM architecture as a modern and widely supported processor architecture is currently the platform of choice for medium performance embedded devices. Almost all major processor manufacturers have ARM products in their portfolio.

The availability of the widespread operating system "Linux" for the ARM platform opens access to a broad range of software, including tools, drivers, and software libraries. Programs written for ARM can easily be employed on the PC platform for testing and debugging.

Examples of actual or potential applications are: protocol converters, measuring and test equipment, data-logging, as well as simple or more complex control and automation tasks.

2. Scope

This document describes the most important hardware features of the StampA5D3x. It includes all informations necessary to develop a customer specific hardware for the StampA5D3x. The Operating System Linux is described in a further document.

The AT91SAMA5D3x processor series consists of several MPUs, like the SAMA5D31, SAMA5D35 and SAMA5D36. Not all processors will be implemented as a Stamp CPU module, but these processors only vary in their variety of peripherals. The differences in peripherals are displayed in the following table.

Peripherals	SAMA5D31	SAMA5D33	SAMA5D34	SAMA5D35	SAMA5D36
CAN0, CAN1	No	No	Yes	Yes	Yes
EMAC	Yes	No	No	Yes	Yes
GMAC	No	Yes	Yes	Yes	Yes
HSMCI2	Yes	No	Yes	Yes	Yes
LCDC	Yes	Yes	Yes	No	Yes
TC1	No	No	No	Yes	Yes
UART0, UART1	Yes	No	No	Yes	Yes

Table 2.1. SAMA5D3X Device Differences

If a peripheral relates only to a specific MPU it will be declared in it's description.

The manual comprises only a brief description of the AT91SAMA5D3x processor, as this is already described in depth in the manual of the manufacturer Atmel®. Descriptions of the ARM® core Cortex-A5 are available from Atmel® and also at *http://www.arm.com*. It is much recommended to have a look at these documents for a thorough understanding of the processor and its integrated peripherals.

3. Overview of Technical Characteristics

3.1. CPU

Atmel AT91SAMA5D3x Embedded Processor featuring an Cortex-A5™ ARM® core with ARM v7-A Thumb2® instruction set.

- CPU Frequency 528 MHz
- 32KB Instruction Cache
- 32KB Data Cache
- Memory Management Unit (MMU)
- Floating Point Unit (VFPv4)
- 3.3V Supply Voltage, 1.8V Memory Bus Voltage, 1.25V Core Voltage

3.2. Memory

- 256 MB NAND Flash Memory (optional up to 1GB)
- 256 MB Low Power Mobile DDR-RAM (optional up to 512 MB)
- 64 MB NOR Flash Memory (optional)
- 1 MB Serial Dataflash
- 128 KB SRAM
- Onboard Micro-SD Card Slot

3.3. Interfaces and external signals

- 2x 100-pin Fine-pitch Low-profile Connectors (Hirose FX8)
- Ethernet 10/100 Mbit MAC
- Ethernet 10/100/1000 GMAC (RGMII)
- 3x USB 2.0 High Speed Host
- USB 2.0 High Speed Device
- 4x USART
- 2x UART
- 2x Synchronous Serial Controller (SSC, I^2S)
- 2x Serial Peripheral Interface (SPI)

- 3x Two Wire Interface (TWI, I^2C)
- High Speed MultiMedia Card Interface
- 2x CAN Controller
- Soft Modem
- 4x PWM
- Touch Screen Analog-to-Digital Converter ADC
- LCD/TFT Controller (2048 x 2048 pixels)
- JTAG Debug Port
- Digital Ports - up to 150 available
- Control Signals: IRQs, BMS, SHDN, WKUP
- 3x Programmable Clocks
- Image Sensor Interface

Some of the various functions are realized by multiplexing connector pins; therefore not all functions may be used at the same time (see Appendix D, *StampA5D3X Pin Assignment*)).

3.4. Security

- taskit Vaultsec - Unreadable Key Storage
- ECC Public/Private and SHA-256 Encryption Chip
- Atmel Secure Boot Solution
- AES, TDES Encryption Engine
- True Random Number Generator
- Unique Hardware Serial Number

3.5. Energy Efficiency

- Shut Down Controller
- Battery Backed Registers
- Programmable Clocks
- Power Management Controller
- Very Slow Clock Operating Mode
- Low Power DDRAM

3.6. Miscellaneous

- 2x Three-channel 32-Bit Timer/Counter
- RTC Battery Backed
- Periodic Interval Timer (PIT)
- Watchdog Timer (WDT)
- Temperature Sensor

3.7. Power Supply

- 3.3V Power Supply
- 3V Backup Power Supply, e.g. from a Lithium Battery

3.8. Dimensions

- Dimensions: 53.6x42x6 mmm (WxDxH)

4. Security Characteristics

4.1. Atmel® Secure Boot Solution

The SAMA5D3 Microcontrollers can be configured to run in standard boot mode or a secure boot mode. In secure boot mode the Microcontroller only boots an image with a correct cryptographic checksum. Information on how the secure boot mode can be enabled, and how the chip operates in this mode is provided by Atmel ® only under a NDA. Please contact the taskit support on how to obtain this.

4.2. Encryption Engine

The StampA5D3x have a DMA supported encryption engine for faster en- and decryption. The Microcontrollers encryption engine is supported by a Linux driver and supports the following encryption standards:

4.2.1. Advanced Encryption Standard (AES)

The Advanced Encryption Standard(AES) specifies a FIPS 197 approved symmetric cryptographic algorithm that can be used to protect electronic data. It is a symmetric block cipher that can encrypt and decrypt information.

The AES can use 128/192/256 bit cryptographic keys to encrypt and decrypt data in blocks of 128 bits in 12/14/16 clock cycles.

4.2.2. Triple Data Encryption Standard (TDES)

The Triple Data Encryption Standard specifies a FIPS 46-3 approved symmetric cryptographic algorithm that can be used to protect electronic data. It is a symmetric block cipher that can encrypt and decrypt information. It supports DES and two-key and three-key algorithms for TDES.

The TDES can use a 64 bit cryptographic key to encrypt and decrypt data in blocks of 8/16/32/64 bits in 18 (DES) or 50 (TDES) clock cycles.

4.2.3. Secure Hash Algorithm SHA

Cryptologic hash functions compute a distinct test value of digital data. They are the base for computing digital signatures. If two messages have the same test value it should guarantee that the messages are the same. The secure Hash Algorithm is compliant with FIPS 180-2 specification.

SHA1, SHA224, SHA256, SHA384 and SHA512 algorithms are supported.

4.3. Serial Number

Every StampA5D3x has a unique 72-bit hardware serial number, which can be used by application software. A Linux driver is provided.

4.4. True Random Number Generator (TRNG)

The True Random Generator (TRNG) passes the American NIST Special Publication 800-22 and the Diehard Random Tests Suites. It provides a 32-bit value every 84 clock cycles.

4.5. taskit Vaultsec

In the Stamp series taskit has implemented a further cryptographic chip, that supports secure, unreadable storing of keys for SHA-256 hashes and ECC public/private key cryptographic algorithms.

- SHA-256 Hash Algorithm
- FIPS186-3 Elliptic Curve Algorithm
- Storage for up to 16 Keys
- Anti-clone for Accessoires and Base Boards
- Secure Boot Validation
- Network and Computer Access Control
- Software Anti-piracy
- Password Handling
- Authenticated or Encrypted Network Communications

A public/private key pair can be generated by the cryptographic chip, where the private key is stored unreadable on the chip and is not known even to the user himself. The public key can be distributed and used for client/server authentication or for cloning prevention, when combined with the same chip on a base board.

The ECC public/private key pair can be used to negotiate an AES session key securely for using the microcontroller's AES engine resulting in a performant communication encryption and decryption. Likewise an AES key can be encrypted by the public key and stored in the filesystem. It can then be used to en- and decrypt files and applications fast.

The ECC public/private key pair can also be used directly to en- and decrypt low volume communication, files and applications.

The SHA algorithm enables to create unique checksums of your applications or configuration files ensuring their integrity.

The taskit Vaultsec solution is supported by a Linux driver. More information about this feature is available via our support.

5. Hardware Description

5.1. Mechanics

The StampA5D3x series was designed as a flexible CPU-Module, which can be connected to base boards via 2x 100-pin fine pitch low profile Hirose ® FX8 connectors.

The size of the StampA5D3x's PCB is only 53.6x42x6.0 mm fitting it in even the smallest design. While having implemented the sensible CPU, DDRAM and Flash design it still exports almost all possible CPU-Pins on it's connectors to allow a flexible design on base boards.

The StampA5D3x series has an on-board Micro SD-Card slot, thus supporting even large memories needs in its compact design.

5.2. AT91SAMA5D3x Processor Core

The AT91SAMA5D3x runs at 528 MHz with a memory bus frequency of 128 MHz.

Here are some of the most important features of the SAMA5D3x ARM Cortex-A5 core:

- 32 Kbyte Data Cache, 32 Kbyte Instruction Cache
- 2x 32 Bit Memory Bus
- Memory Management Unit (MMU)
- ARM v7-A Thumb2® Instruction Set, ARM Thumb 16-bit and 32-bit Instruction Set supported
- VFPv4 Floating Point Unit
- ARM Jazelle® Technology for Java® Acceleration
- ICE/JTAG Debug Environment

Some of these features - like Jazelle - are currently not supported by the operating system of the product.

5.3. Memory

The AT91SAMA5D3x Microcontroller series is equipped with two 32-Bit external bus interfaces, a DDR2, LPDDR2 and LPDDR interface and a static memory controller (EBI0) and which includes a NAND flash controller (NFC). DDR2/LPDDR2/LPDDR interface voltage is 1.8 V and runs at 132 MHz. Chip select zero (NCS0) of EBI0 ist connected to the optional NOR flash, the NAND flash is connected on chip select three (NCS3). The EBI0 operates at 3.3V.

The external bus interface is not available on the interface connectors of the StampA5D3x.

5.3.1. NAND Flash

The StampA5D3x is equipped with a 256 MB NAND flash with 100000 erase and write cycles. Customer specific adaptations are possible up to 1 GB on-board NAND flash. It is connected to chip select three (NCS3) of the microcontroller.

NAND flash has a different organisation of transistors than the commonly used NOR flash. While it allows a much higher density and thus an increase in storage capacity, there are some differences which need to be kept in mind.

Typically, NAND flash is organized in pages and blocks, similar to hard disks. Pages are 512, 2048 or 4096 bytes in size, typical block sizes are 16, 128, 256 or 512 KB. Reading and programming are performed on a page basis. Programming can only be done sequently in one block.

Additionally, NAND flash requires bad block management, either by the driver software or by a separate controller chip. Most NAND devices are shipped with bad blocks. These are identified and marked according to a specified bad block strategy. Further bad blocks may be detected during runtime. They are detected via an ECC (error correcting code). If a bad block is detected, the data is written to a different, good block, and the bad block table is updated. So the overall memory capacity gradually shrinks as more and more blocks are marked bad.

This error detection is done by software like U-boot and Linux. Additionally, NAND flash is subject to a limited number of write and erase cycles. These are typically 100.000 cycles per block. So it is highly recomended to use wear levelling filesystems.

5.3.2. NOR Flash

Optional the StampA5D3x can be equipped with 64MB NOR flash. Please note that when NOR flash is assembled pins 14 to 40 (PE0 - PE27) are used on the module itself and are not available for other multiplexing (see Appendix D, *StampA5D3X Pin Assignment*).

Typically NOR flash is organized in blocks, similar to hard disks. Typical block sizes are 64, 128, 256 KB. NOR flash can be read and written randomly. This makes it possible to use NOR flash as execute in place (XIP) memory. To erase already written data, the whole block containing the data has to be erased.

NOR flash is subject to limited write and erase cycles. These are typically 100.000 cycles per block. So it is highly recommended to use wear levelling file systems.

5.3.3. LPDDR-SDRAM

The StampA5D3x is equipped with 256MB LPDDR-SDRAM (Low power DDR-SDRAM). Customer specific adaptations allow configurations up to 512MB.

DDR-SDRAM allows random access to any of its memory area and is volatile memory. DDR-SDRAM (Double Data Rate) takes over data at the rising and falling edge of a clock pulse, thus achieving almost twice the bandwidth than a similar connected SDRAM. It has a synchronous interface, that means it waits for a clock signal before responding to control inputs and is therefore synchronized with the CPU bus. The clock is used to drive a final

state machine in the chip, which allows to accept new instructions, before the previous one has finished executing.

5.3.4. SRAM

The StampA5D3x is equipped with 128 KB internal SRAM. The internal SRAM can be accessed in one bus cycle and may be used for time critical sections of code or interrupt handlers.

5.4. Bus Matrix

The bus matrix of AT91SAM-controllers allows many master and slave devices to be connected independently of each other. Each master has a decoder and can be defined specially for each master. This allows concurrent access of masters to their slaves (provided the slave is available).

The bus matrix is thus the bridge between external devices connected to the EBI, the microcontroller's embedded peripherals and the CPU core.

Master 0	Cortex A5
Master 1	DMA Controller 0
Master 2	DMA Controller 0
Master 3	DMA Controller 0
Master 4	DMA Controller 1
Master 5	DMA Controller 1
Master 6	DMA Controller 1
Master 7	Gigabit Ethernet MAC DMA
Master 8	LCD DMA
Master 9	LCD DMA
Master 10	USB Host High Speed EHCI DMA
Master 11	USB HOST OHCI DMA
Master 12	USB Device High Speed DMA
Master 13	Ethernet MAC DMA
Master 14	ISI Controller DMA

Table 5.1. Bus Matrix Masters

Slave 0	Internal SRAM 0
Slave 1	Internal SRAM 1
Slave 2	NFC SRAM
Slave 3	Internal ROM
Slave 4	Soft Modem (SMD)
Slave 5	UDP High Speed Dual RAM
	USB OHCI
	USB EHCI
Slave 6	External Bus Interface

Slave 7	DDR2 Port 0
Slave 8	DDR2 Port 1
Slave 9	DDR2 Port 2
Slave 10	DDR2 Port 3
Slave 11	Peripheral Bridge 0
Slave 12	Peripheral Bridge 1

Table 5.2. Bus Matrix Slaves

5.5. Advanced Interrupt Controller (AIC)

The core features of the Advanced Interrupt Controller are:

- 128 Internal and External Sources
- 8-level Priority Controller
- Level Sensitive or Edge Triggered
- Programmable Polarity for External Sources

Moreover, all PIO lines can be used to generate a PIO interrupt. However, the PIO lines can only generate level change interrupts, that is, positive as well as negative edges will generate an interrupt. The PIO interrupt itself (PIO to AIC line) is usually programmed to be level-sensitive. Otherwise interrupts will be lost if multiple PIO lines source an interrupt simultaneously.

On the StampA5D3x FIQ, IRQ and GPIO interrupts are available. The list of peripheral identifiers, which are used to program the AIC can be found in Table B.1, “Peripheral Identifiers”

5.6. Battery Backup

The following parts of the AT91SAMA5D3x Processor can be backed-up by a battery:

- RC Oscillator
- Slow Clock Oscillator
- Reset Controller
- Shutdown Controller
- RTC
- General Purpose Backup Registers
- Boot Select Control Register

It is recommended to always use a backup power supply (normally a battery) in order to speed up the boot-up time and to avoid reset problems.

5.7. Reset Controller (RSTC)

The embedded microcontroller has an integrated Reset Controller which samples the backup and the core voltage. The presence of a backup voltage (VDDBU) when the card is powered down speeds up the boot time of the microcontroller.

5.8. Peripheral Input/Output Controller (PIO)

The StampA5D3x has a maximum of 150 freely programmable digital I/O ports on its connectors. These pins are also used by other peripheral devices.

The Parallel Input/Output Controller(PIO) manages up to 32 programmable I/O ports. Each I/O port is associated with a bit number in the 32 bit register of the user interface. Each I/O port may be configured for general purpose I/O or assigned to a function of an integrated peripheral device. In doing so multiplexing with multiple integrated devices is possible. That means a pin may be used as GPIO or only as one of the peripheral functions. The PIO Controller also features a synchronous output providing up to 32 bits of data output in a single write operation.

The following characteristics are individually configurable for each PIO pin:

- PIO enable
- Peripheral enable
- Output enable
- Output level
- Write Enable
- Level change interrupt
- Glitch filter: pulses that are lower than a half clock cycle are ignored
- Open-drain outputs
- Pull-up resistor

All configurations as well as the pin status can be read back by using the appropriate status register. Multiple pins of each PIO can also be written simultaneously by using the synchronous output register.

For interrupt handling, the PIO Controllers are considered as user peripherals. This means that the PIO Controller interrupt lines are connected among the interrupt sources 2 to 31. Refer to the PIO Controller peripheral identifier Table B.1, “Peripheral Identifiers” to identify the interrupt sources dedicated to the PIO Controllers. The PIO Controller interrupt can be generated only if the PIO Controller clock is enabled.

A number of the PIO signals might be used internally on the module. Care has to be taken when accessing the PIO registers in order not to change the settings of these internal signals, otherwise a system crash is likely to happen.

5.9. Clock Generation

5.9.1. Processor Clocks

The AT91SAMA5D3x has no PLLB, but provides the 480 MHz USB Clock via a UPLL.

The CPU generates its clock signals based on two crystal oscillators: One slow clock (SLCK) oscillator running at 32.768 KHz and one main clock oscillator running at 18.432 MHz. The slow clock oscillator also serves as the time base for the real time timer. It draws a minimum of current (a few micro-Amps) and can therefore be backeded up by a small lithium battery when the board is powererd down.

From the main clock oscillator, the CPU generates two further clocks by using two PLLs. PLLA provides the processor clock (PCK) and the master clock (MCK). PLLB typically provides the 48 MHz USB clock and is normally used only for this purpose. The clocks of most peripherals are derived from MCK. These include EBI, USART, SPI, TWI, SSC, PIT and TC.

Some peripherals like the programmable clocks and the timer counters (TC) can also run on SLCK. The real time timer (RTT) always runs on SLCK.

Clock	Frequency	Source
PCK (Processor Clock)	528 MHz	PLLA
MCK (Master Clock)	132 MHz	PCK
USB Clock	480 MHz	UPLL
Slow Clock	32.768 KHz	Slow Clock Oscillator

Table 5.3. AT91SAMA5D3x Clocks

5.9.2. Programmable Clocks

The programmable clocks can be individually programmed to derive their input from SLCK, PLLA, PLLB and Main Clock. Each PCK has a divider of 2, 4, 8, 16, 32 or 64.

The StampA5D3x features three programmable clocks PCK0/1/2.

5.10. Power Management Controller (PMC)

5.10.1. Function

The PMC has a Peripheral Clock register which allows to individually enable or disable the clocks of all integrated peripherals by using their "Peripheral Identifier" (see Table B.1, “Peripheral Identifiers”). The System Clock register allows to enable or disable each of the following clocks individually:

- Processor Clock
- DDR Clock
- LCD Clock

- SMD Clock
- USB Host Clock (common for all three channels)
- USB Device Clock
- Programmable Clocks

The PMC status register provides "Clock Ready" or, respectively, "PLL Lock" status bits for each of these clocks. An interrupt is generated when any of these bits changes from 0 to 1. The PMC provides status flags for the

- Main Oscillator
- Master Clock
- PLLA
- PLLB
- Programmable Clocks

The Main Oscillator frequency can be measured by using the PMC Main Clock Frequency register. The SLCK is used as reference for the measurement.

5.10.2. Power Management

Using power management can dramatically reduce the power consumption of an Embedded Device. Via the PMC various clocks can be disabled or their speed can be reduced:

- stopping the PLLs (PLLA and / or PLLB)
- stopping the clocks of the various peripherals
- reducing the clock rates of peripherals, especially by changing MCK.

The PMC supports the following power-saving features: Idle mode and power-down mode. Please note that not every operating system supports these modes.

- **Idle Mode.** In idle mode, the processor clock will be re-enabled by any interrupt. The peripherals, however, are only able to generate an interrupt if they still have a clock, so care has to be taken as to when a peripheral can be powered down.
- **Power-down Mode.** In many cases a system waits for a user action or some other rare event. In such a case, it is possible to change MCK to SLCK. Any external event which changes the state on peripheral pins (not the USB) can then be detected by the PIO controller or the AIC.

  It should also be taken into account that when a PLL is stopped it will take some time to restart it. Changing the PLL frequencies or stopping them can therefore be done only at a moderate rate. If short reaction times are required, this is not a choice.

Additionally, the following measures can reduce power consumption considerably:

- switching off the TFT supply voltage
- putting peripheral chips like Ethernet controller and / or PHY or serial driver devices in power down mode
- putting the SDRAM into self-refresh mode

5.11. Timer Counter (TC)

The StampA5D3x features two blocks of timer counters with three counters each. The second block is not present on all variations of the StampA5D3x series. Compare Table 2.1, “SAMA5D3X Device Differences”.

The TC consists of three independent 16-bit Timer/Counter units. They may be cascaded to form a 32-bit or 48-bit timer/counter. The timers can run on the internal clock sources MCK/2, MCK/8, MCK/32, MCK/128, SLCK or the output of another timer channel. External clocks may be used as well as the counters can generate signals on timer events. They also can be used to generate PWM signals.

5.12. Pulse Width Modulation Controller (PWM)

The PWM controls four channels independently. Each Channel controls two complementary square output waveforms. Characteristics of the output waveforms such as period, duty-cycle, polarity and dead-times are configured through the user interface. Each channel selects and uses one of the clocks provided by the clock generator. The clock generator provides several clocks resulting from the division of the PWM master clock (MCK).

- 4 Independent Channels
- Common clock Generator Providing Thirteen Different Clocks
- 2 2-bit Gray Up/Down Channels for Stepper Motor Control
- Synchronous Channel Mode
- 2 Independent Event Lines to Synchronize ADC Conversions
- Comparision Units
- Write Protected Registers

5.13. Periodic Interval Timer (PIT)

The PIT consists of a 20-bit counter running on MCK / 16. This counter can be preloaded with any value between 1 and 2^{20}. The counter increments until the preloaded value is reached. At this stage it rolls over and generates an interrupt. An additional 12-bit counter counts the interrupts of the 20 bit counter.

The PIT is intended for use as the operating system's scheduler interrupt.

5.14. Watchdog Timer

The watchdog timer is a 12-bit timer running at 256 Hz (Slow Clock / 128). The maximum watchdog timeout period is therefore equal to 16 seconds. If enabled, the watchdog timer asserts a hardware reset at the end of the timeout period. The application program must always reset the watchdog timer before the timeout is reached. If an application program has crashed for some reason, the watchdog timer will reset the system, thereby reproducing a well defined state once again.

The Watchdog Mode Register can be written only once. After a processor reset, the watchdog is already activated and running with the maximum timeout period. Once the watchdog has been reconfigured or deactivated by writing to the Watchdog Mode Register, only a processor reset can change its mode once again.

5.15. Real-time Clock (RTC)

The Real-time clock combines a complete time-of-day clock with alarm, a two-hundred-year Gregorian calendar and a programmable periodic interrupt. The time and calendar values are coded in BCD format.

5.16. DMA Controller (DMAC)

The DMA Controller (DMAC) supports the following transfer schemes:

- Peripheral-to-Memory
- Memory-to-Peripheral
- Peripheral-to-Peripheral
- Memory-to-Memory

The DMAC contains unidirectional and bidirectional channels. The full-duplex peripherals feature unidirectional channels used in pairs (transmit only or receive only). The half-duplex peripherals feature one bidirectional channel. Typically full-duplex peripherals are USARTs, SPI or SSC. The HSMCI is a half duplex device.

The SAMA5 microcontrollers have two DMA controllers connected to the AMBA peripheral bridge. DMAC0 handles transfers between peripherals and memory from peripherals connected on APB0 (AMBA Peripheral Bridge 0).

Instance	T/R Channel	Interface Number
HSMCI0	Receive/Transmit	0
SPI0	Transmit	1
SPI0	Receive	2
USART0	Transmit	3
USART0	Receive	4
USART1	Transmit	5

Instance	T/R Channel	Interface Number
USART1	Receive	6
TWI0	Transmit	7
TWI0	Receive	8
TWI1	Transmit	9
TWI1	Receive	10
UART0	Transmit	11
UART0	Receive	12
SSC0	Transmit	13
SSC0	Receive	14
SMD	Transmit	15
SMD	Receive	16

Table 5.4. DMAC0 Channels Definition

DMAC1 handles transfers between peripherals and memory from peripherals connected on APB1 (AMBA Peripheral Bridge 1).

Instance	T/R Channel	Interface Number
HSMCI1	Receive/Transmit	0
HSMCI0	Receive/Transmit	1
ADC	Receive	2
SSC1	Transmit	3
SSC1	Receive	4
UART1	Transmit	5
UART1	Receive	6
USART2	Transmit	7
USART2	Receive	8
USART3	Transmit	9
USART3	Receive	10
TWI2	Transmit	11
TWI2	Receive	12
DBGU	Transmit	13
DBGU	Receive	14
SPI1	Transmit	15
SPI1	Receive	16
SHA	Transmit	17
AES	Transmit	18
AES	Receive	19
TDES	Transmit	20
TDES	Receive	21

Table 5.5. DMAC1 Channels Definition

Using the DMAC removes processor overhead by reducing its intervention during the transfer. This significantly reduces the number of clock cycles required for a data transfer,

which improves microcontroller performance. The DMAC supports single transfer and chained buffer transfer. In chained buffer transfer mode, the address is automatically incremented, when the countable limit of the current transfer buffer is reached.

To launch a transfer, the peripheral triggers its associated DMA channels by using transmit and receive signals. When the programmed data is transferred, an end of transfer interrupt is generated by the peripheral itself. There are four kinds of interrupts generated by the DMAC:

- Buffer Transfer Completed
- Chained Buffer Transfer Completed
- Access Error
- Descriptor Integrity Check Error

5.17. Debug Unit (DBGU)

The Debug Unit is a simple UART which provides only RX/TX lines. It is used as a simple serial console for Firmware and Operating Systems.

5.18. JTAG Unit

The JTAG unit can be used for hardware diagnostics, hardware initialization, flash memory programming, and debug purposes. The JTAG unit supports two different modes, namely the "ICE Mode", and the "Boundary Scan" mode. It is normally jumpered for "ICE Mode".

JTAG interface devices are available for the unit. However, the use of them is not within the scope of this document.

5.19. Two-wire Interface (TWI)

The StampA5D3x features three two-wire interfaces.

The TWI is also known under the expression "I^2C-Bus", which is a trademark of Philips and may therefore not be used by other manufacturers. However, interoperability is guaranteed. The TWI supports both master or slave mode.

The TWI uses only two lines, namely serial data (SDA) and serial clock (SCL). According to the standard, the TWI clock rate is limited to 400 kHz in fast mode and 100 kHz in normal mode, but configurable baud rate generator permits the output data rate to be adapted to a wide range of core clock frequencies.

5.20. Multimedia Card Interface (MCI)

The StampA5D3x features a onboard Micro-SD-Card slot, which is connected to the HMCI1 interface of the microcontroller. The HMCI0 interface is provided for external additional use.

The MultiMedia Card Interface (MCI) supports the MultiMedia Card (MMC) Specification V3.11, the SDIO Specification V1.1 and the SD Memory Card Specification V1.0.

The MCI includes a command register, response registers, data registers, timeout counters and error detection logic that automatically handle the transmission of commands and, when required, the reception of the associated responses and data with a limited processor overhead. The MCI supports stream, block and multi-block data read and write, and is compatible with the Peripheral DMA Controller (PDC) channels, minimizing processor intervention for large buffer transfers.

The MCI operates at a rate of up to Master Clock divided by 2 and supports the interfacing of 2 slot(s). Each slot may be used to interface with a MultiMediaCard bus (up to 30 Cards) or with a SD Memory Card. Only one slot can be selected at a time (slots are multiplexed). A bit field in the SD Card Register performs this selection.

The SD Memory Card communication is based on a 9-pin interface (clock, command, four data and three power lines) and the MultiMedia Card on a 7-pin interface (clock, command, one data, three power lines and one reserved for future use). The SD Memory Card interface also supports MultiMedia Card operations. The main differences between SD and MultiMedia Cards are the initialization process and the bus topology.

5.21. USB Host Port (UHP)

The StampA5D3x integrates three USB host ports supporting speeds up to 480 MBit/s. USB Host Port B and C are connected directly to the transceiver, USB Host Port A is multiplexed with the USB device port. Only one of them can be used at a time.

The controller is fully compliant with the Enhanced HCI(EHCI) specification. It supports both High-speed 480 Mbps and Full-speed 12 Mbps devices.

The USB Host Port (UHP) interfaces the USB with the host application. It handles Open HCI protocol (Open Host Controller Interface) as well as USB v2.0 Full-speed and Low-speed protocols.

The USB Host Port integrates a root hub and transceivers on downstream ports. It provides several high-speed half-duplex serial communication ports. Up to 127 USB devices (printer, camera, mouse, keyboard, disk, etc.) and an USB hub can be connected to the USB host in the USB "tiered star" topology.

5.22. USB Device Port (UDP)

The StampA5D3x integrates one USB device port supporting speeds up to 480 MBit/s. It is multiplexed with the USB Host Port A. Only one of them can be used at a time.

The controller is fully compliant with the Enhanced HCI(EHCI) specification. It supports both High-speed 480 Mbps and Full-speed 12 Mbps devices.

The USB Device Port (UDP) is compliant with the Universal Serial Bus (USB) V2.0 full-speed device specification. The USB device port enables the product to act as a device to other host controllers.

The USB device port can also be implemented to power on the board. One I/O line may be used by the application to check that VBUS is still available from the host. Self-powered devices may use this entry to be notified that the host has been powered off. In this case, the pullup on DP must be disabled in order to prevent feeding current to the host. The application should disconnect the transceiver, then remove the pullup.

5.23. Ethernet MAC (EMAC)

The EMAC module implements a 10/100 MBit/s Ethernet MAC compatible with the IEEE 802.3 standard using an address checker, statistics and control registers, receive and transmit blocks, and a DMA interface.

The address checker recognizes four specific 48-bit addresses and contains a 64-bit hash register for matching multicast and unicast addresses. It can recognize the broadcast address of all ones, copy all frames, and act on an external address match signal.

An individual 48-bit MAC address (ETHERNET hardware address) is allocated to each product. This number is stored in flash memory. It is recommended not to change the MAC address in order to comply with IEEE Ethernet standards.

To completely implement ethernet an additional physical layer interface is needed (PHY). A sample implementation is found on the Starterkit Board. The EMAC is not present on all variations of the StampA5D3x series. Compare Table 2.1, “SAMA5D3X Device Differences”.

5.24. Gigabit Ethernet MAC (GMAC)

The GMAC module implements a 10/100/1000 MBit/s Ethernet Gigabit MAC compatible with the IEEE 802.3 standard using an address checker, statistics and control registers, receive and transmit blocks, and a DMA interface.

The address checker recognizes four specific 48-bit addresses and contains a 64-bit hash register for matching multicast and unicast addresses. It can recognize the broadcast address of all ones, copy all frames, and act on an external address match signal.

An individual 48-bit MAC address (ETHERNET hardware address) is allocated to each product. This number is stored in flash memory. It is recommended not to change the MAC address in order to comply with IEEE Ethernet standards.

To completely implement ethernet an additional physical layer interface is needed (PHY). Only RGMII is supported on on the StampA5D3x series The GMAC is not present on all variations of the StampA5D3x series. Compare Table 2.1, “SAMA5D3X Device Differences”.

5.25. Controller Area Network (CAN)

The CAN controller provides all features required to implement the serial communication protocol. It is fully compliant with CAN 2.0 Part A and Part B specifications. Part A or B specification is independently programmable for each message.

It supports bit rates up to 1 Mbit/s and handles data, remote, error and overload frames.

The StampA5D3x integrates two CAN controllers, CAN0 and CAN1. The CAN controller is not present on all variations of the StampA5D3x series. Compare Table 2.1, “SAMA5D3X Device Differences”.

5.26. Software Modem Device (SMD)

The SMD is a block for communication via a modem's Digital Isolation Barrier (DIB) with a complementary Line Side Device (LSD). Power and clock are supplied by the SMD and consumed by the LSD. The data flow is bidirectional. The data transfer is based on pulse width modulation for transmission from the SMD to the LSD, and for receiving from the LSD.

It has two bidirectional channels, a data and a control channel. The data channel is used to transfer digitized signal samples at a constant rate of 16 bits at 16 kHz, whereas the control channel is used to communicate with control regiters of the LSD at a maximum rate of 8 bits at 16 kHz.

5.27. Universal Sychronous Asynchronous Receiver and Transmitter (USART)

The StampA5D3x has up to four independent USARTs and two UARTs, not including the debug unit. The UARTS are not present on all variations of the StampA5D3x series. Compare Table 2.1, “SAMA5D3X Device Differences”.

The Universal Synchronous Asynchronous Receiver Transceiver (USART) provides one full duplex universal synchronous asynchronous serial link. Data frame format is widely programmable (data length, parity, number of stop bits) to support a maximum of standards. The receiver implements parity error, framing error and overrun error detection. The receiver time-out enables handling variable-length frames and the transmitter timeguard facilitates communications with slow remote devices. Multidrop communications are also supported through address bit handling in reception and transmission.

The USART supports the connection to the Peripheral DMA Controller, which enables data transfers to the transmitter and from the receiver. The PDC provides chained buffer management without any intervention of the processor.

Six different modes are implemented within the USARTs:

- Normal (standard RS232 mode)
- RS485
- Hardware Handshaking
- ISO7816 Protocol: T=0 or T=1
- IrDA

RS485. In RS485 operating mode the RTS pin is automatically driven high during transmit operations. If RTS is connected to the "enable" line of the RS485 driver, the driver will thus be enabled only during transmit operations.

Hardware Handshaking. The hardware handshaking feature enables an out-of-band flow control by automatic management of the pins RTS and CTS. The receive DMA channel must be active for this mode. The RTS signal is driven high if the receiver is disabled or if the DMA indicates a buffer full condition. As the RTS signal is connected to the CTS line of the connected device, its transmitter is thus prevented from sending any more characters.

ISO7816. The USARTs have an ISO7816-compatible mode which permits interfacing with smart cards and Security Access Modules (SAM). Both T=0 and T=1 protocols of the ISO7816 specification are supported.

IrDA. The USART features an infrared (IrDA) mode supplying half-duplex point-to-point wireless communication. It includes the modulator and demodulator which allows a glueless connection to the infrared transceivers. The modulator and demodulator are compliant with the IrDA specification version 1.1 and support data transfer speeds ranging from 2.4 kb/s to 115.2 kb/s.

Signals of the Serial Interfaces. All UARTs/USARTs have one receiver and one transmitter data line (full duplex). Not all USARTs are implemented with full modem control lines. Furthermore the available lines depend largely on the used multiplexing. Most modem control lines can be implemented with standard digital ports.

Hardware Interrupts. There are several interrupt sources for each USART:

- Receive: RX Ready, (DMA) Buffer Full, End of Receive Buffer
- Transmit: TX Ready, (DMA) Buffer Empty, End of Transmit Buffer, Shift Register Empty
- Errors: overrun, parity, framing, and timeout errors
- Handshake: the status of CTS has changed
- Break: the receiver has detected a break condition on RXD
- NACK: non acknowledge (ISO7816 mode only)
- Iteration: the maximum number of repetitions has been reached (ISO7816 mode only)

Please refer to the chapter about the DMA unit (PDC) for a description of the "Buffer Full" and "End of Receive / Transmit Buffer" events.

5.28. Synchronous Peripheral Interface (SPI)

The StampA5D3x features two SPI ports, with four respectively one chipselect available.

The Serial Peripheral Interface (SPI) circuit is a synchronous serial data link that provides communication with external devices in Master or Slave Mode. It also enables communication between processors if an external processor is connected to the system.

The Serial Peripheral Interface is essentially a shift register that serially transmits data bits to other SPIs. During a data transfer, one SPI system acts as the "master" which controls the data flow, while the other devices act as "slaves" which have data shifted into and out by the master.

A slave device is selected when the master asserts its NSS signal. If multiple slave devices exist, the master generates a separate slave select signal for each slave (NPCS). The SPI system consists of two data lines and two control lines:

- Master Out Slave In (MOSI): This data line supplies the output data from the master shifted into the input(s) of the slave(s).
- Master In Slave Out (MISO): This data line supplies the output data from a slave to the input of the master. There may be no more than one slave transmitting data during any particular transfer.
- Serial Clock (SPCK): This control line is driven by the master and regulates the flow of the data bits. The master may transmit data at a variety of baud rates; the SPCK line cycles once for each bit that is transmitted. The SPI baudrate is Master Clock (MCK) divided by a value between 1 and 255
- Slave Select (NSS): This control line allows slaves to be turned on and off by hardware.

Each SPI Controller has a dedicated receive and transmit DMA channel.

5.29. Synchronous Serial Controller (SSC)

The StampA5D3x has two SSC interfaces available, depending on the multiplexing of the pins.

The SSC supports many serial synchronous communication protocols generally used in audio and telecom applications such as I2S, Short Frame Sync, Long Frame Sync, etc.

The SSC has separated receive and transmit channels. Each channel has a data, a clock and a frame synchronization signal (RD, RK, RF, resp. TD, TK, TF). Both a receive and a transmit DMA channel are assigned to each SSC.

5.30. Image Sensor Interface (ISI)

The Image Sensor Interface (ISI) supports direct connection to the ITU-R BT. 601/656 8-bit mode compliant sensors and up to 12-bit grayscale sensors. It receives the image data stream from the image sensor on the 12-bit data bus. This module receives up to 12 bits for data, the horizontal and vertical synchronizations and the pixel clock. The reduced pin count alternative for synchronization is supported for sensors that embed SAV (start of active video) and EAV (end of active video) delimiters in the data stream.

The Image Sensor Interface interrupt line is generally connected to the Advanced Interrupt Controller and can trigger an interrupt at the beginning of each frame and at the end of a DMA frame transfer. If the SAV/EAV synchronization is used, an interrupt can be triggered on each delimiter event.

For 8-bit color sensors, the data stream received can be in several possible formats: YCbCr 4:2:2, RGB 8:8:8, RGB 5:6:5 and may be processed before the storage in memory. The data stream may be sent on both preview path and codec path if the bit CODEC_ON in the ISI_CR1 is one. To optimize the bandwidth, the codec path should be enabled only when a capture is required.

In grayscale mode, the input data stream is stored in memory without any processing. The 12-bit data, which represent the grayscale level for the pixel, is stored in memory one or two pixels per word, depending on the GS_MODE bit in the ISI_CR2 register. The codec datapath is not available when grayscale image is selected.

5.31. LCD controller

The LCD controller supports single scan active TFT LCD modules with a resolution of up to 2048x2048 with a color depth of up 24 bits per pixel. As the video memory is shared, a maximum resolution of 1280x720 pixels is recommended to maintain a reasonable memory bandwidth for other applications.

The LCD controller relies on a relatively simple frame buffer concept, which means that all graphics and character functions have to be implemented in software: character sets and graphic primitives are not integrated in the controller.

5.31.1. LCDC Initialisation and LCD Power Sequencing

LCD cells (pixels) should not be subjected to DC power for prolonged periods of time, as chemical decomposition might take place. The LCD controller therefore provides for a strict AC control of the LCD pixels. To do so, the LCD controller has to be initialized appropriately. Switching on the LCD supply voltage therefore has to take place after the LCDC initialization or shortly before.

Accordingly, the LCDC should not be powered down without deactivating the LCD supply voltage. The same is true if the LCDC is stopped indirectly by stopping the respective clock source, namely the PLLA.

The LCD backlight supply is not involved in these considerations. It may switched on or off at any time independently of the state of the LCDC.

5.31.2. LCDC Frame Buffer

The LCDC Frame Buffer typically resides in the external RAM.

The LCDC video memory is organized as a frame buffer in a straight forward way. It supports color depths of 1, 2, 4, 8, 16, or 24 bit per pixel. The video data is stored in a packed form with no unused bits in the video memory.

The color resolutions of 1, 2, 4, and 8 bpp (bits per pixel) use a palette table which is made up of 16-bit entries. The value of each pixel in the frame buffer serves as an index into the palette table. The value of the respective palette table entry is output to the display by the LCDC, see Table 5.6, “LCDC palette entry”.

Bit[14..10]	Bit[9..5]	Bit[4..0]
Blue[7..3]	Green[7..3]	Red[7..3]

Table 5.6. LCDC palette entry

The bits 2..0 of each color channel are not used in the palettized configuration — they are set to 0.

The same scheme as above is used in the 16-bit color resolution configuration, although in this case the frame buffer entry is output directly to the display instead of indexing a palette table.

In the 24-bit color resolution configuration, each frame buffer entry consists of one byte for each color, see Table 5.7, “LCDC 24 bit memory organization”.

Bit[23..16]	Bit[15..8]	Bit[7..0]
Blue[7..0]	Green[7..0]	Red[7..0]

Table 5.7. LCDC 24 bit memory organization

If the LCD Module has lower color resolution (fewer bits per color component), only the most significant bits of each component are used.

The Linux frame buffer driver offers a function which returns the information about the frame buffer structure including the assignment of each frame buffer bit to a color channel bit. It is recommended that graphics software uses this function in order to achieve a correct color representation.

5.32. Touch Screen ADC Controller (ADC)

The StampA5D3x has a 12-bit Analog-to-Digital Converter, which includes a 4-wire or 5-wire resistive touchscreen controller. It integrates a 12-to-1 analog multiplexer, making analog-to-digital conversions of 12 analog lines possible. The conversions extend from 0V to the voltage carried on pin ADVREF and has configurable timings.

6. Design Considerations

6.1. Ethernet Controller (EMAC)

The emac needs an aditional PHY design. The emac supports both, MII and RMII interface.

Please take care of the specific layout requirements of the Ethernet port when designing a base board. The two signals of the transmitter pair (ETX+ and ETX-) should be routed in parallel (constant distance, e.g. 0.5mm) with no vias on their way to the RJ45-jack. The same is true for the receiver pair (ERX+ and ERX-). No other signals should be crossing or get next to these lines. If a ground plane is used on the base board, it should be omitted in the vicinity of the Ethernet signals.

A 1nF / 2kV capacitor should be connected between board ground and chassis ground (which is usually connected to the shield of the RJ45-jack).

6.2. USB Host Controller (UHP)

External Parts. A few external parts are required for the proper operation of the UHP:

- No pull-down resistors are needed.
- No series resistors are needed.
- Small capacitors (e.g. 15pF) to ground on each line (optional).
- ESD protection devices are recommended for applications which are subject to external contact. The restrictions with regard to capacitive loading have to be applied when selecting a protection device.
- A circuit to generate the 5V VBUS supply voltage.

V_{BUS} considerations for USB Host. A USB host port has to provide a supply voltage V_{BUS} of 5V +- 5% which has to be able to source a maximum of 500mA, or 100mA in case of battery operation. Please refer to the appropriate rules in the USB specification. A low ESR capacitor of at least 120µF has to be provided on V_{BUS} in order to avoid excessive voltage drops during current spikes.

V_{BUS} has to have an over-current protection. The over-current drawn temporarily on V_{BUS} must not exceed 5A. Polymeric PTCs or solid state switches are recommended by the specification. Suitable PPTCs are "MultiFuse" (Bourns), "PolyFuse" (Wickmann/Littelfuse), "PolySwitch" (Raychem/Tyco).

It is required that the over-current condition can be detected by software, so that V_{BUS} can be switched off or be reduced in power in such a case.

Layout considerations. If external resistors are needed, they should be placed in the vicinity of the module's connector. The two traces of any of the differential pairs (USB-Host A+ and USB-Host A- , as well as USB-Host B+ and USB-Host B-) should not encircle large areas on the base board, in order to reduce signal distortion and noise. The are preferably routed closely in parallel to the USB connector.

USB High-Speed. If designing USB High-Speed a wave impedance of 90 Ω on the traces should be respected. The traces shoud be routed as short as possible and in parallel with as low parallel capacitance as possible.

6.3. USB Device Controller (UDP)

External Parts. A few external parts are required for the proper operation of the UDP:

- No pull-down resistors are needed.
- No series resistors are needed.
- A voltage divider on the 5V USB supply voltage VBUS converting this voltage to 3.3V (1.8V), e.g. 27 kΩ / 47 kΩ, for the VBUS monitoring input (USB_CNX).
- ESD protection devices are recommended for applications which are subject to external contact. The restrictions with regard to capacitive loading have to be applied when selecting a protection device.

The USB specification demands a switchable pull-up resistor of 1.5 kΩ on USB-Device+ which identifies the UDP as a full speed device to the attached host controller. On this module, this resistor is integrated on the chip. It can be switched on or off using the "USB Pad Pull-up Control Register", which is part of the "Bus Matrix User Interface" (not the "USB Device Port User Interface", as one might expect). This pull-up resistor is required to be switchable in order not to source current to an attached but powered down host. This would otherwise constitute an irregular condition on the host. The software has to take care of this fact.

The capacitors are intended to improve the signal quality (edge rate control) depending on the specific design. They are not mandatory. The total capacitance to ground of each USB pin, the PCB trace to the series resistor, and the capacitor must not exceed 75pF.

Operation with V_{BUS} as a Supply. Special care has to be taken if the module is powered by the VBUS supply. Please refer to the appropriate rules in the USB specification with regard to inrush current limiting and power switching. As the module draws more than 100mA in normal mode, it is a "high-power" device according to the specification (<100mA = "low-power", 100..500mA = "high-power"). It therefore requires staged switching which means that at power-up it should draw not more than 100mA on VBUS. The capacitive load of a USB device on VBUS should be not higher than 10µF.

Layout considerations. The external resistors should be placed in the vicinity of the module's connector. The traces of the differential pair (USB-Device+ and USB-Device-) should not encircle large areas on the base board, in order to reduce signal distortion and noise. The are preferably routed closely in parallel to the USB connector.

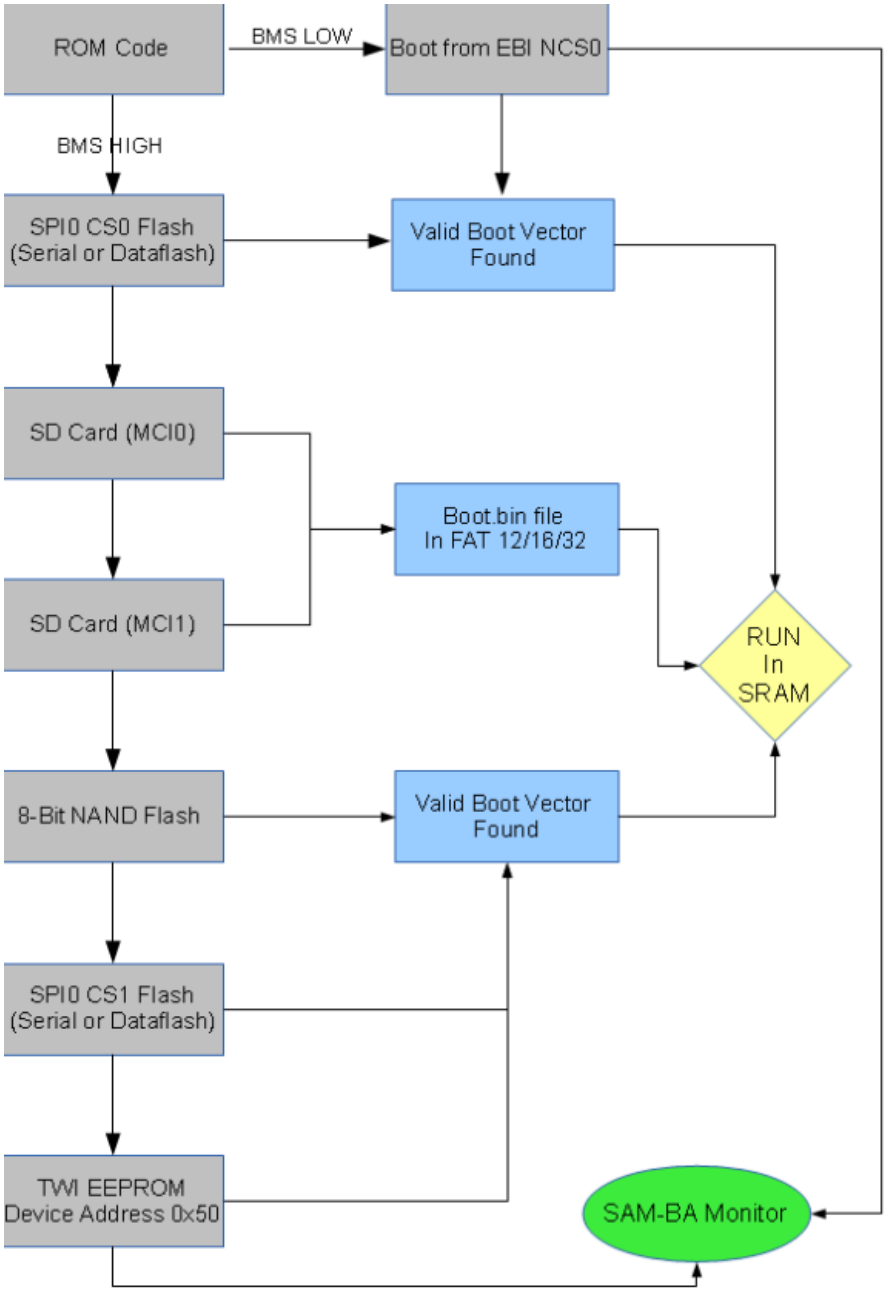
6.4. Booting Strategies

6.4.1. Boot Sequence

On power-up the AT91SAMA5 microcontroller always boots the first level bootloader from internal ROM memory at address 0x0. It can boot in standard boot mode, which will be

described in this chapter, or in secure boot mode. How the secure boot mode can be enabled and how the chip operates in this mode is provided in an application by Atmel®, which is only available under NDA. Please contact taskit support, if you want to employ the secure bootloader.

The ROM code first samples the BMS signal, if it is low, it will boot from NOR flash connected to NCS0 of the external bus. If it is high it tries to retrieve valid code from external memories. The sequence is shown in the following diagram



The standard boot sequence can be altered by writing to the boot sequence controller (BSC) at address 0xFFFF FE54. This has the effect of speeding up the boot process or to avoid having relevant pins driven during the boot process. The boot configuration register is battery-backed and thus the state is preserved during reboots, if a battery is connected. Otherwise it is reset to the default value (0X0).

Boot Value	SPI0 NPCS0	SD Card MCI0	SD Card MCI1	NAND Flash	SPI0 NPCS1	TWI EEPROM	SAM-BA
0	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1	Yes	No	Yes	Yes	Yes	Yes	Yes
2	Yes	No	No	Yes	Yes	Yes	Yes
3	Yes	No	No	No	Yes	Yes	Yes
4	Yes	No	No	No	Yes	Yes	Yes
5-7	No	No	No	No	No	No	Yes

Table 6.1. SAMA5D3X Boot Sequence

Please note, that boot from SD Card (MCI1) is not working according to the errata of the Microcontroller.

6.4.2. SAM-BA Monitor

If no valid code is found along the configured sequence the SAM-BA monitor is launched. The SAM-BA Monitor initializes the DBGU and USB-Device. It then checks if an USB device enumeration occurs or if characters are received on the DBGU. Once the communication interface is identified, it runs an infinite loop, waiting for commands.

The SAM-BA monitor allows programming of flash or similar. For this purpose Atmel provides a tool running on desktop PCs. If you need to use the SAM-BA monitor and have valid code on one of the booting devices, these have to be disabled first (e.g. disable chipselect of serial or nand flash or remove SD/MMC-Card).

6.4.3. Design Constraints

The boot sequence affects the design of the pins, which are initialized during the boot sequence. When using pins in a different multiplexing, which are also assigned to a boot device, it has to be kept in mind that these pins could be muxed for the relevant peripheral during boot process and accordingly driven by the microprocessor. Programming the boot sequence controller may help to avoid unwanted side effects.

Before performing the jump to the application in the internal SRAM, all PIOs and peripherals used in the boot program are set to their reset state

Boot Device	Pin	Pio Line	Pin on Stamp
SD Card MCI0	CK	PD9	Bus 71
	CDA	PD0	Bus 76
	DA0	PD1	Bus 75
	DA1	PD2	Bus 74
	DA2	PD3	Bus 73
	DA3	PD4	Bus 72
SPI Flash SPI0	MOSI	PD11	IO 94
	MISO	PD10	IO 95
	SPCK	PD12	IO 93
	NPCS0	PD13	IO 92

Boot Device	Pin	Pio Line	Pin on Stamp
	NPCS1	PD14	IO 91
TWI EEPROM TWI0	TWD0	PA30	IO 38
	TWCK0	PA31	IO 37
DBGU	DRXD	PB30	Bus 43
	DTXD	PB31	Bus 42

Table 6.2. Pins Driven by Boot on Stamp Interface

Appendix A. Peripheral Color Codes

This table matches the color used to identify various peripherals in tables.

Power Supply/Ground
USART
Debug UART
TWI (I^2C-Bus)
SD-Card/MMC
SPI
USB Host
USB Device
Reserved
Synhcronous Serial Controller (SSC)
JTAG
Control
Ethernet
Genral Purpose I/O Port
Programmable Clock Output
Analog-to-digital Converter
Timer Counter
Image Sensor Interface
LCD/TFT Controller Interface
Embedded Trace Macrocell
Static Memory Controller
Compact Flash Interface
Pulse Width Modulator
Touch Controller
Can Controller
AC97 Sound Interface
Encryption Device
Soft Modem
True Random Generator

Appendix B. Peripheral Identifiers

ID	Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC	System Controller Interrupt	
2	DBGU	Debug Unit Interrupt	
3	PIT	Periodic Interval Timer Interrupt	
4	WDT	Watchdog Timer Interrupt	
5	HSMC	Multi-bi ECC Interrupt	
6	PIOA	Parallel I/O Controller A	
7	PIOB	Parallel I/O Controller B	
8	PIOC	Parallel I/O Controller C	
9	PIOD	Parallel I/O Controller D	
10	PIOE	Parallel I/O Controller E	
11	SMD	SMD Soft Modem	
12	US0	USART 0	
13	US1	USART 1	
14	US2	USART 2	
15	US3	USART 3	
16	UR0	UART 0	
17	UR1	UART 1	
18	TWI0	Two-Wire Interface 0	
19	TWI1	Two-Wire Interface 1	
20	TWI2	Two-Wire Interface 2	
21	HSMCI0	High Speed Multi Media Card Interface 0	
22	HSMCI1	High Speed Multi Media Card Interface 0	
23	HSMCI2	High Speed Multi Media Card Interface 0	
24	SPI0	Serial Peripheral Interface	
25	SPI1	Serial Peripheral Interface	
26	TC0	Timer Counter 0 (0,1,2)	
27	TC1	Timer Counter 1 (3,4,5)	
28	PWM	Pulse Width Modulation Controller	
29	ADC	Touch Screen ADC Controller	
30	DMAC0	DMA Controller 0	
31	DMAC1	DMA Controller 1	
32	UHPHS	USB Host High Speed	
33	UDPHS	USB Device High Speed	
34	GMAC	Gigabit Ethernet MAC	
35	EMAC	Ethernet MAC	
36	LCDC	LCD Controller	
37	ISI	Image Sensor Interface	
38	SSC0	Synchronous Serial Controller 0	

ID	Mnemonic	Peripheral Name	External Interrupt
39	SSC1	Synchronous Serial Controller 1	
40	CAN0	Can Controller 0	
41	CAN1	Can Controller 1	
42	SHA	Secure Hash Algorithm	
43	AES	Advanced Encryption Standard	
44	TDES	Triple Data Encryption Standard	
45	TRNG	True Random Generator	
46	ARM	Performance Monitor Unit	
47	AIC	Advanced Interrupt Controller	IRQ
48	FUSE	Fuse Controller	
49	MPDDRC	MPDDR Controller	
50-63	Reserved		

Table B.1. Peripheral Identifiers

Appendix C. Address Map (Physical Address Space)

After the execution of the remap command the 4 GB physical address space is separated as shown in the following table. Accessing these addresses directly is only possible if the MMU (memory management unit) is deactivated. As soon as the MMU is activated the visible address space is changed completely. If absolute memory addresses should be accessed within an application, the corresponding address space has first to be mapped to the virtual address space using mmap or ioremap under Linux.

Address (Hex)	Mnemonic	Function
00 0000	Boot Memory	NCS0 or Internal ROM or internal SRAM (depending on BMS and REMAP)
10 0000	ROM	Internal ROM
20 0000	NFC SRAM	Nand Flash Controller SRAM
30 0000	SRAM 0	Internal SRAM 0 64 kByte
31 0000	SRAM 1	Internal SRAM 1 64 kByte
40 0000	SMD	Static Memory Controller
50 0000	UDPHS	USB Device Port (DMA)
60 0000	USB OHCI	USB OHCI Controller
70 0000	USB EHCI	USB EHCI Controller
80 0000	AXI	AXI Matrix
90 0000	DAP	Bridge Controller
1000 0000	EBI NCS0	Chip Select 0
2000 0000	DDRCS	DDRAM Chip Select
4000 0000	EBI NCS1	Chip Select 1
5000 0000	EBI NCS2	Chip Select 2
6000 0000	EBI NCS3	Chip Select 3
7000 0000	NFC	NAND Flash Controller Command Register
F000 0000	HSMCI0	High Speed Multimedia Card / SD-Card Interface 0
F000 4000	SPI0	Serial Peripheral Interface 0
F000 8000	SSC0	Serial Synchronous Controller 0(I^2S)
F000 C000	CAN0	CAN Interface 0
F001 0000	TC0, TC1, TC2	3 Timer Counter, 16-Bit
F001 4000	TWI0	Two Wire Interface 0(I^2C)
F001 8000	TWI1	Two Wire Interface 1(I^2C)
F001 C000	USART0	Synchronous or Asynchronous Serial Port 0
F002 0000	USART1	Synchronous or Asynchronous Serial Port 1
F002 4000	UART0	Asynchronous Serial Port 0
F002 8000	GMAC	Gigabit Ethernet Controller
F002 C000	PWM	Pulse Width Modulator
F003 0000	LCD	LCD Controller
F003 4000	ISI	Image Sensor Interface

Address (Hex)	Mnemonic	Function
F003 8000	SFR	Special Functions Register
F800 0000	HSMCI1	High Speed Multimedia Card / SD-Card Interface 1
F800 4000	HSMCI2	High Speed Multimedia Card / SD-Card Interface 2
F800 8000	SPI1	Serial Peripheral Interface 1
F800 C000	SSC1	Serial Synchronous Controller 1(I^2S)
F801 0000	CAN1	CAN Interface 1
F801 4000	TC3, TC4, TC5	3 Timer Counter, 16-Bit
F801 8000	TSADC	Touch Controller ADC Interface
F801 C000	TWI2	Two Wire Interface 2(I^2C)
F802 0000	USART2	Synchronous or Asynchronous Serial Port 2
F802 4000	USART3	Synchronous or Asynchronous Serial Port 3
F802 8000	UART1	Asynchronous Serial Port 1
F802 C000	EMAC	Ethernet Controller
F803 0000	UDPHS	High Speed USB Device
F803 4000	SHA	Secure Hash Algorithm
F803 8000	AES	Advanced Encryption Standard
F803 C000	TDES	Triple Data Encryption Standar
F804 0000	TRNG	True Random Number Generator
FFFF C000	HSMC	Static Memory Controller
FFFF E400	FUSE	Fuse Controller
FFFF E600	DMAC0	DMA Controller 0
FFFF E800	DMAC1	DMA Controller 1
FFFF EA00	MPDDRC	DDRAM Controller
FFFF EC00	MATRIX	Bus Matrix User Interface
FFFF EE00	DBGU	Debug Unit, including UART
FFFF F000	AIC	Advanced Interrupt Controller
FFFF F200	PIOA	32 Bit Parallel I/O Controller A
FFFF F400	PIOB	32 Bit Parallel I/O Controller B
FFFF F600	PIOC	32 Bit Parallel I/O Controller C
FFFF F800	PIOD	32 Bit Parallel I/O Controller D
FFFF FA00	PIOE	32 Bit Parallel I/O Controller E
FFFF FC00	PMC	Power Management Controller
FFFF FE00	RSTC	Reset Controller, Battery Powered
FFFF FE10	SHDC	Shutdown Controller, Battery Powered
FFFF FE30	PIT	Periodic Interval Timer 32 Bit
FFFF FE40	WDT	Watchdog Timer
FFFF FE50	SCKCR	Serial Clock Register
FFFF FE54	BSC	Boot Sequence Configuration Register
FFFF FE60	GPBR	General Purpose Backup Registers
FFFF FEB0	RTCC	Real-time Clock, Battery Powered

Table C.1. Physical Address Space

Appendix D. StampA5D3X Pin Assignment

Pin	GPIO	Periph. A	Periph. B	Periph. C		Periph. C	Periph. B	Periph. A	GPIO	Pin
1	VCC					GND				2
3	VCC					GND				4
5	VCC					GND				6
7	VCC					GND				8
9	PE31	IRQ	PWM L1					NWAIT	PE30	10
11	PE29	NWR1/ NBS1	TCLK2			LCD DAT23	TIOB2	NCS2	PE28	12
13	PE27	NCS1	TIOA2	LCD DAT22			TXD2	**NCS0**	PE26	14
15	PE25	**A25**	RXD2				RTS2	**A24**	PE24	16
17	PE23	**A23**	CTS2				SCK2	**A20**	PE20	18
19	GND						TXD3	**A19**	PE19	20
21	PE18	**A18**	RXD3				RTS3	**A17**	PE17	22
23	PE16	**A16**	CTS3				SCK3	**A15**	PE15	24
25	PE14	**A14**						**A13**	PE13	26
27	PE12	**A12**						**A11**	PE11	28
29	PE10	**A10**				GND				30
31	PE9	**A9**						**A8**	PE8	32
33	PE7	**A7**						**A6**	PE6	34
35	PE5	**A5**						**A4**	PE4	36
37	PE3	**A3**						**A2**	PE2	38
39	PE1	**A1**						**A0/NBS0**	PE0	40
41	GND							DTXD	PB31	42
43	PB30	DRXD						TXD1	PB29	44
45	PB28	RXD1					G12SCK0	RTS1	PB27	46
47	PB26	CTS1	GRX7				GRX6	SCK1	PB25	48
49	PB18	G12SK						GMDIO	PB17	50
51	GND							GMDC	PB16	52
53	PB15	GCOL	CANTX1				CANRX1	GCRS	PB14	54
55	PB13	GRXER	PWM L3				PWM H3	GRXDV	PB12	56
57	PB11	GRXK	RD1				RF1	GTXER	PB10	58
59	PB9	GTXEN	PWM L2			GND				60
61	PB8	GTXCK	PWM H2				RK1	GRX3	PB7	62
63	PB6	GRX2	TD1				PWM L1	GRX1	PB5	64
65	PB4	GRX0	PWM H1				TF1	GTX3	PB3	66
67	PB2	GTX2	TK1				PWM L0	GTX1	PB1	68
69	PB0	GTX0	PWM H0			GND				70
71	PD9	MCI0 CK						MCI0 DA3	PD4	72
73	PD3	MCI0 DA2						MCI0 DA1	PD2	74
75	PD1	MCI0 DA0						MCI0 CDA	PD0	76

Pin	GPIO	Periph. A	Periph. B	Periph. C		Periph. C	Periph. B	Periph. A	GPIO	Pin
77	GND					VBATT				78
79	BMS								NRST	80
81	WKUP								SHDN	82
83	GND								DIBP	84
85	HHSDPC								DIBN	86
87	HHSDMC					TCK				88
89	GND					TDO				90
91	HHSDPB					TMS				92
93	HHSDMB					TDI				94
95	GND					JTAGSEL				96
97	HHSDPA	DHSDP				NTRST				98
99	HHSDMA	DHSDM				GND				100

Table D.1. Pin Assignment BUS Interface X2

Pin	GPIO	Periph. A	Periph. B	Periph. C		Periph. C	Periph. B	Periph. A	GPIO	Pin
1	GND						PWMFI1	FIQ	PC31	2
3	PC30	UTXD0		ISI PCK		ISI D8	PWMFI2	URXD0	PC29	4
5	PC28	SPI1 NPCS3	PWMFI0	ISI D9		ISI D10	TWCK1	SPI1 NPCS2	PC27	6
7	PC26	SPI1 NPCS1	TWD1	ISI D11				SPI1 NPCS0	PC25	8
9	PC24	SPI1 SPCK						SPI1 MOSI	PC23	10
11	PC22	SPI1 MISO				GND				12
13	PC21	RD0						RF0	PC20	14
15	PC19	RK0						TD0	PC18	16
17	PC17	TF0						TK0	PC16	18
19	PC15	MCI2 CK	PCK2	LCD DAT21		LCD DAT16	TCLK1	MCI2 DA3	PC14	20
21	PC13	MCI2 DA2	TIOB1	LCD DAT17		LCD DAT18	TIOA1	MCI2 DA1	PC12	22
23	PC11	MCI2 DA0		LCD DAT19		LCD DAT20		MCI2 CDA	PC10	24
25	GND							EMDIO	PC9	26
27	PC8	EMDC	TCLK5				TIOB5	EREFCK	PC7	28
29	PC6	ERXER	TIOA5				TCLK4	ECRSDV	PC5	30
31	PC4	ETXEN	TIOB4				TIOA4	ERX1	PC3	32
33	PC2	ERX0	TCLK3				TIOB3	ETX1	PC1	34
35	PC0	ETX0	TIOA3			GND				36
37	PA31	**TWCK0**	UTXD1	ISI HSYNC		ISI VSYNC	URXD1	**TWD0**	PA30	38
39	PA29	LCD DEN						LCD PCK	PA28	40
41	PA27	LCD HSYNC						LCD VSYNC	PA26	42

Pin	GPIO	Periph. A	Periph. B	Periph. C		Periph. C	Periph. B	Periph. A	GPIO	Pin
43	PA25	LCD DISP						LCD PWM	PA24	44
45	PA23	LCD DAT23	PWM L1	ISI D7		ISI D6	PWM H1	LCD DAT22	PA22	46
47	GND					ISI D5	PWM L0	LCD DAT21	PA21	48
49	PA20	LCD DAT20	PWM H0	ISI D4		ISI D3	TWCK2	LCD DAT19	PA19	50
51	PA18	LCD DAT18	TWD2	ISI D2		ISI D1		LCD DAT17	PA17	52
53	PA16	LCD DAT16		ISI D0				LCD DAT15	PA15	54
55	PA14	LCD DAT14						LCD DAT13	PA13	56
57	PA12	LCD DAT12						LCD DAT11	PA11	58
59	GND							LCD DAT10	PA10	60
61	PA9	LCD DAT9						LCD DAT8	PA8	62
63	PA7	LCD DAT7						LCD DAT6	PA6	64
65	PA5	LCD DAT5						LCD DAT4	PA4	66
67	PA3	LCD DAT3						LCD DAT2	PA2	68
69	PA1	LCD DAT1						LCD DAT0	PA0	70
71	GND					ADVREF				72
73	PD31	AD11	PCK1				PCK0	AD10	PD30	74
75	PD29	AD9						AD8	PD28	76
77	PD27	AD7						AD6	PD26	78
79	PD25	AD5						AD4	PD24	80
81	PD23	AD3						AD2	PD22	82
83	PD21	AD1						AD0	PD20	84
85	PD19	ADTRG				GND				86
87	PD18	TXD0						RXD0	PD17	88
89	PD16	RTS0	SPI0 NPCS3	PWM FI3		CAN TX0	SPI0 NPCS2	CTS0	PD15	90
91	PD14	SCK0	SPI0 NPCS1	CAN RX0				**SPI0 NPCS0**	PD13	92
93	PD12	**SPI0 SPCK**						**SPI0 MOSI**	PD11	94
95	PD10	**SPI0 MISO**				PWM L3		MCI0 DA7	PD8	96
97	PD7	MCI0 DA6	TCLK0	PWM H3		PWM L2	TIOB0	MCI0 DA5	PD6	98
99	PD5	MCI0 DA4	TIOA0	PWM H2		GND				100

Table D.2. Pin Assignment IO Interface X1

Appendix E. StampA5D3x Electrical Characteristics

Ambient temperature 25℃, unless otherwise indicated

Symbol	Description	Parameter	Min.	Typ.	Max	Unit
V_{CC}	Operating Voltage		3.0	3.3	3.6	V
V_{MEM}	Memory Bus Voltage		1.7	1.8	1.95	V
V_{RES}	Reset Treshhold			2.93		V
T_{RES}	Duration of Reset Pulse		100	220	330	ms
V_{IH}	High-Level Input Voltage	3.3V	2.0		V_{CC} + 0.3	V
V_{IL}	Low-Level Input Voltage	3.3V	-0.3		0.8	V
V_{VDDANA}	Analog DC Supply Voltage		3.0	3.3	3.6	V
R_{PULL}	Pull-up Resistance		45	70	130	kΩ
	Pull-down Resistance					
P	Normal Operation			353		mW
	Full Load	max.		550		mW
	Power-Down			5		mW
V_{BATT}	Battery Voltage		2.0	3.0	V_{CC}	V
I_{BATT}	Battery Current	Ambient temp. = 25℃		5		µA
		Ambient temp. = 70℃			17	µA
		Ambient temp. = 85℃			22	µA

Table E.1. Electrical Characteristics

Appendix F. StampA5D3x Clock Characteristics

Symbol	Description	Dependency	Tolerance	Typical Value	Unit
MAINCK	Main Oscillator Frequency			12.000	MHz
SLCK	Slow Clock			32.768	KHz
PLLACK	PLLA Clock	MAINCK		528.000	MHz
PCK	Processor Clock	PLLACK		528.000	MHz
MCK	Master Clock	PCK		132.000	MHz
DDRCK	DDRAM Clock	MCK		132.000	MHz
BCK	Baudrate Clock	MCK	1.5%	10.37(max)	MHz
UTMI PLL	USB Clock	MAINCK	0.25%	480.000	MHz

Table F.1. Clock Characteristics

Appendix G. StampA5D3x Environmental Ratings

Symbol	Description	Parameter	Operating		Storage		Unit
			Min.	Max.	Min.	Max.	
T_A	Ambient temperature		-30	85	-45	85	℃
	Relative Humidity	no condensation		90		90	%RH
	Absolute Humidity		<= Humidity@T_A = 60℃, 90%RH				
	Corrosive Gas		not admissible				

Table G.1. Environmental Ratings

Appendix H. StampA5D3x Dimensions

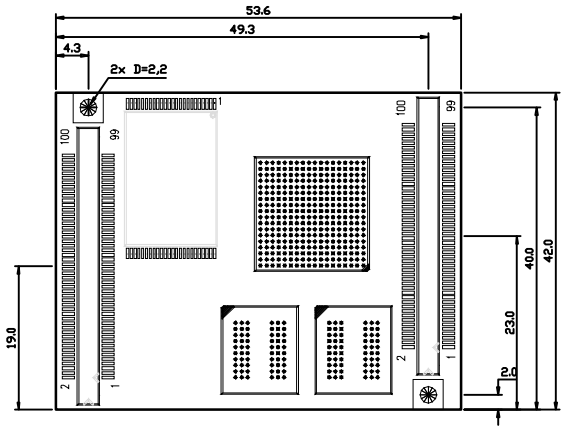


Figure H.1. StampA5D3x Dimensions

Appendix I. PortuxA5/Starterkit Schematics

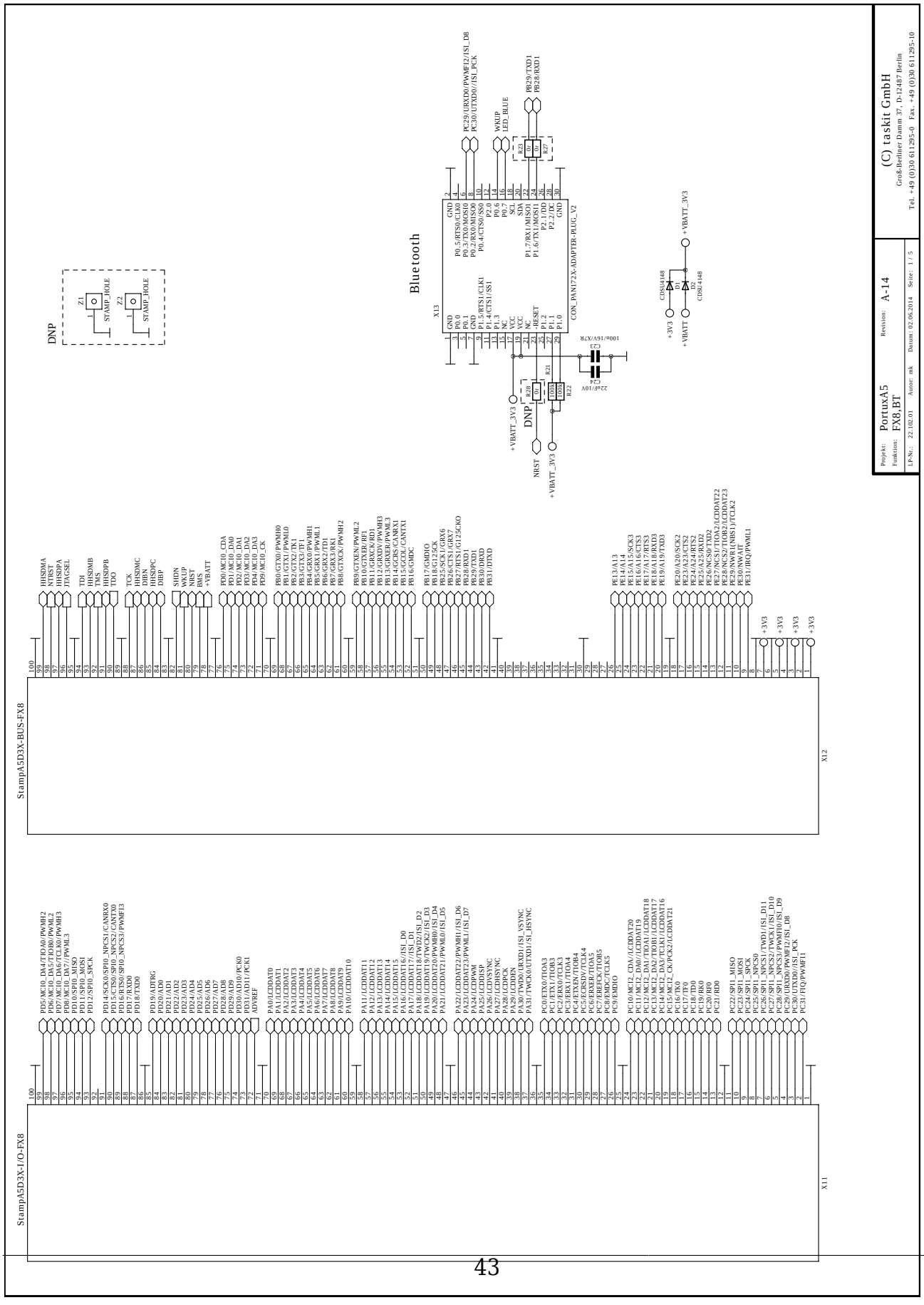


Figure I.1. PortuxA5 FX8,BT

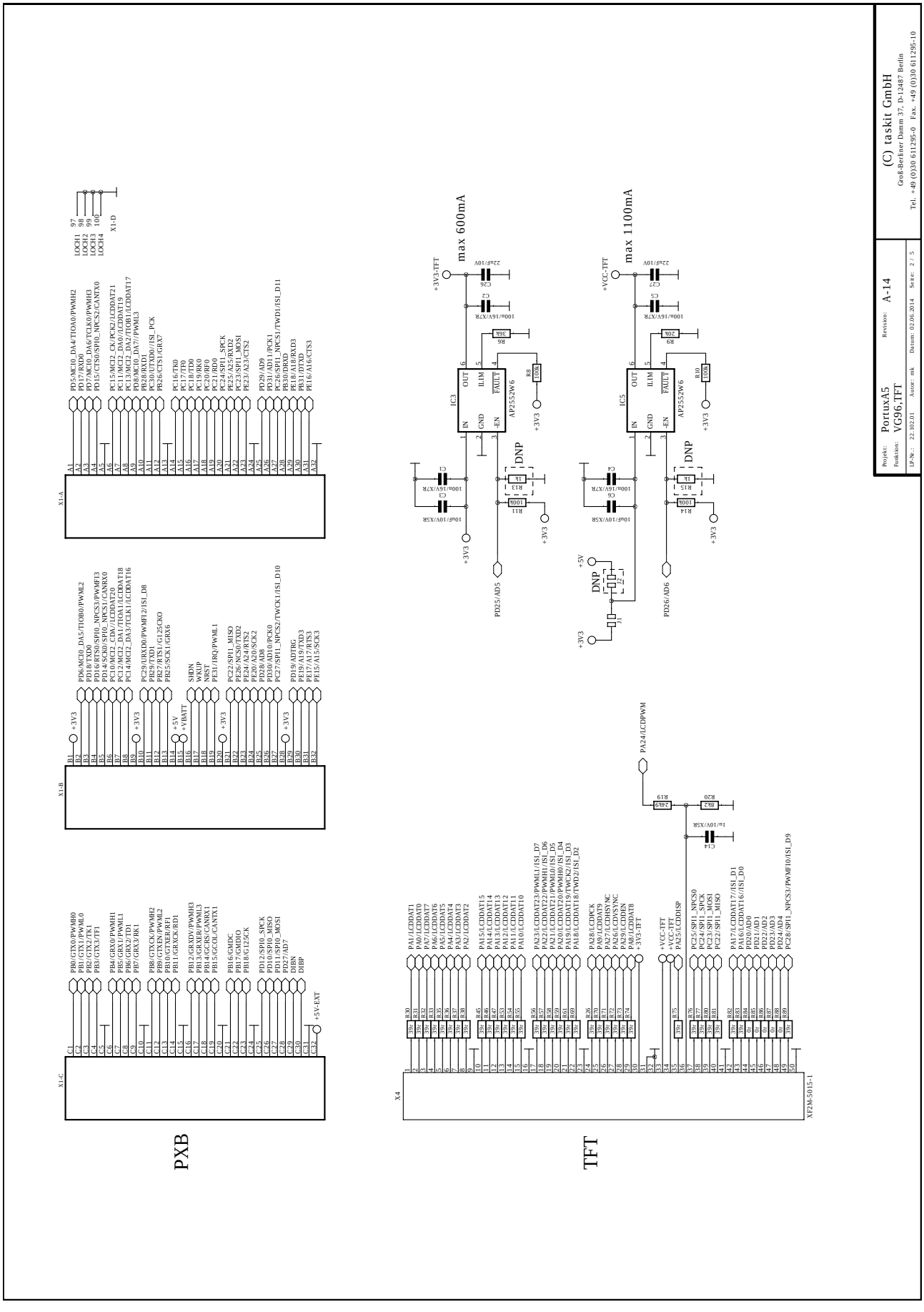


Figure I.2. PortuxA5 VG96,TFT

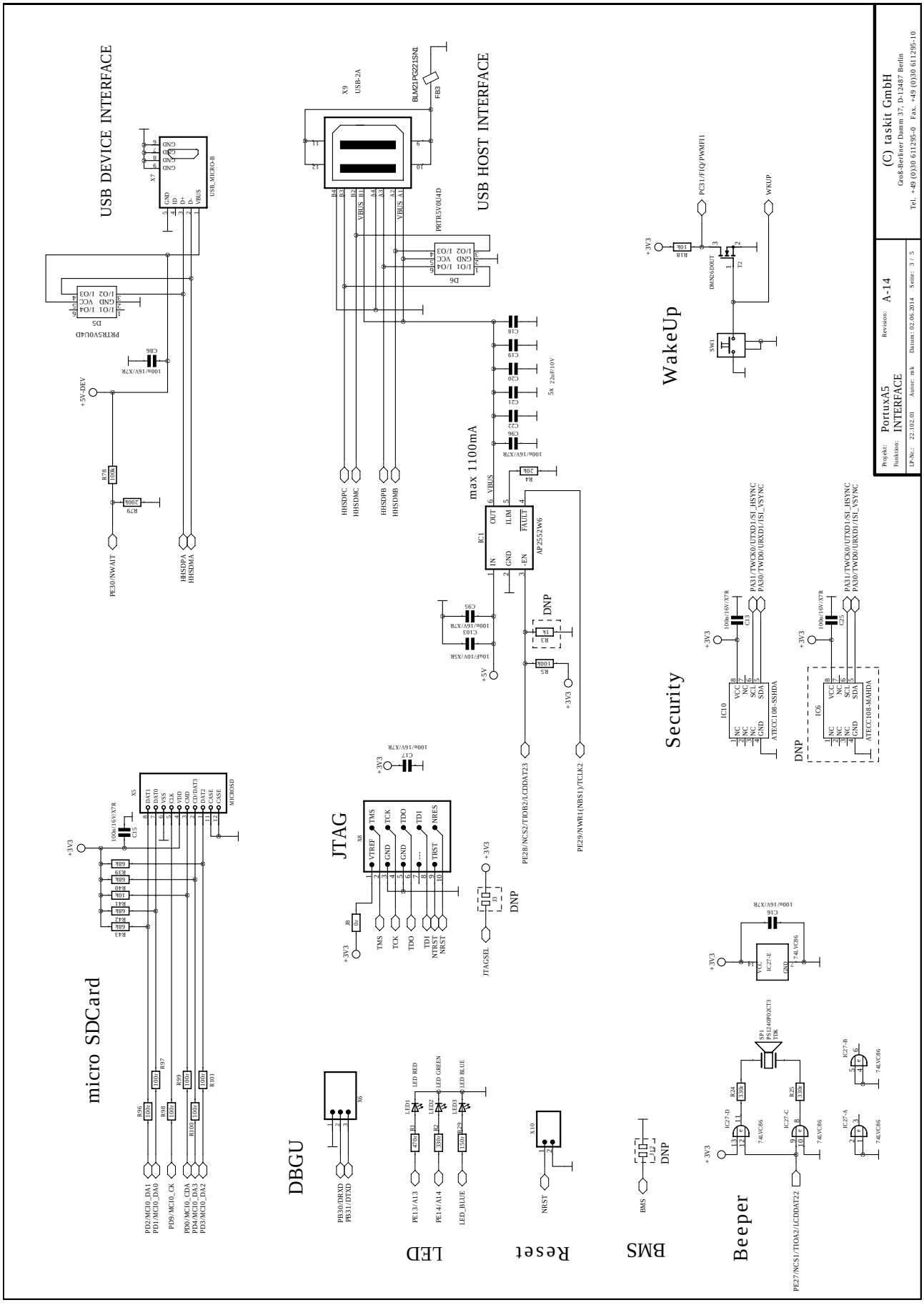


Figure I.3. PortuxA5 Interface

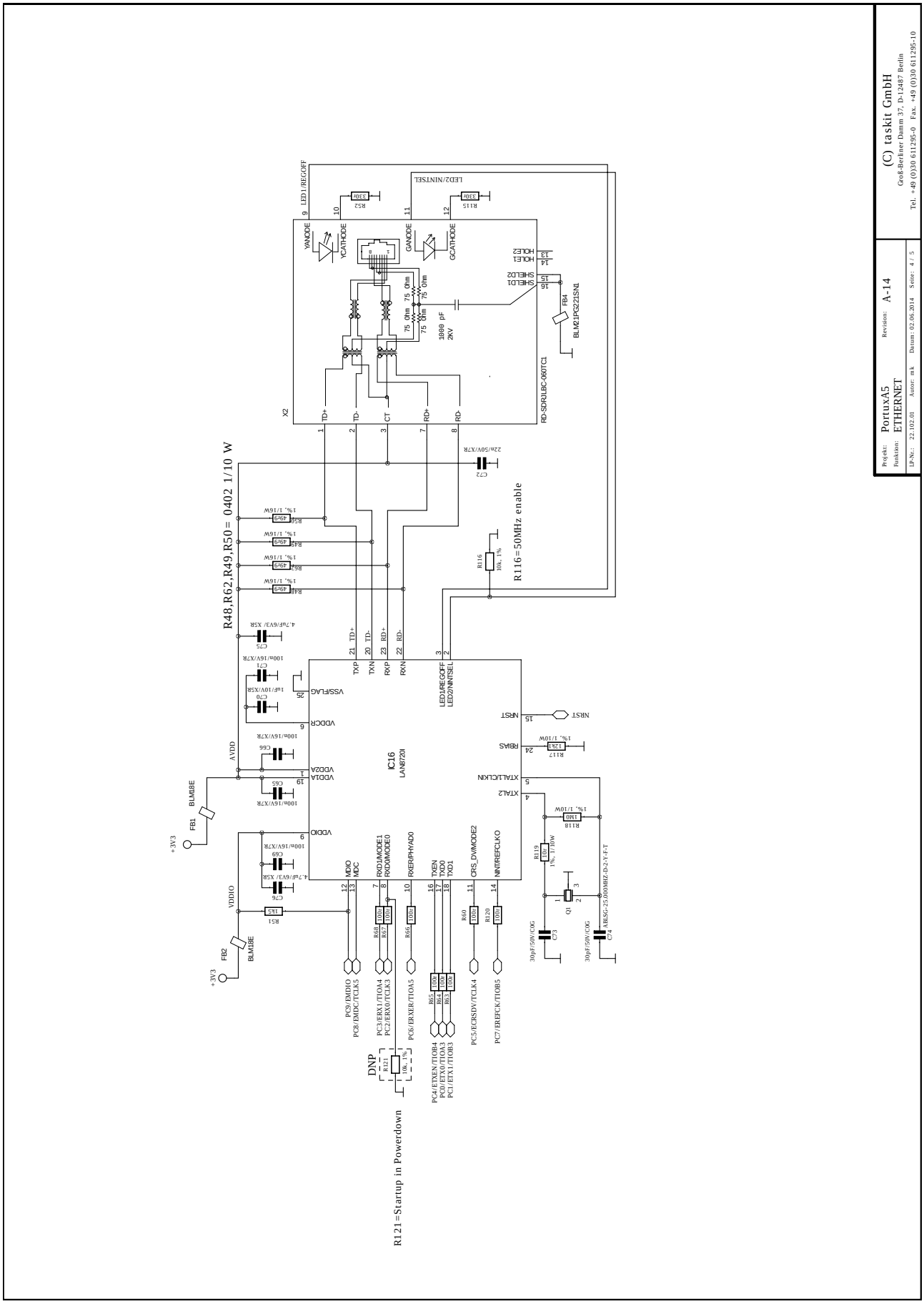


Figure I.4. PortuxA5 Ethernet

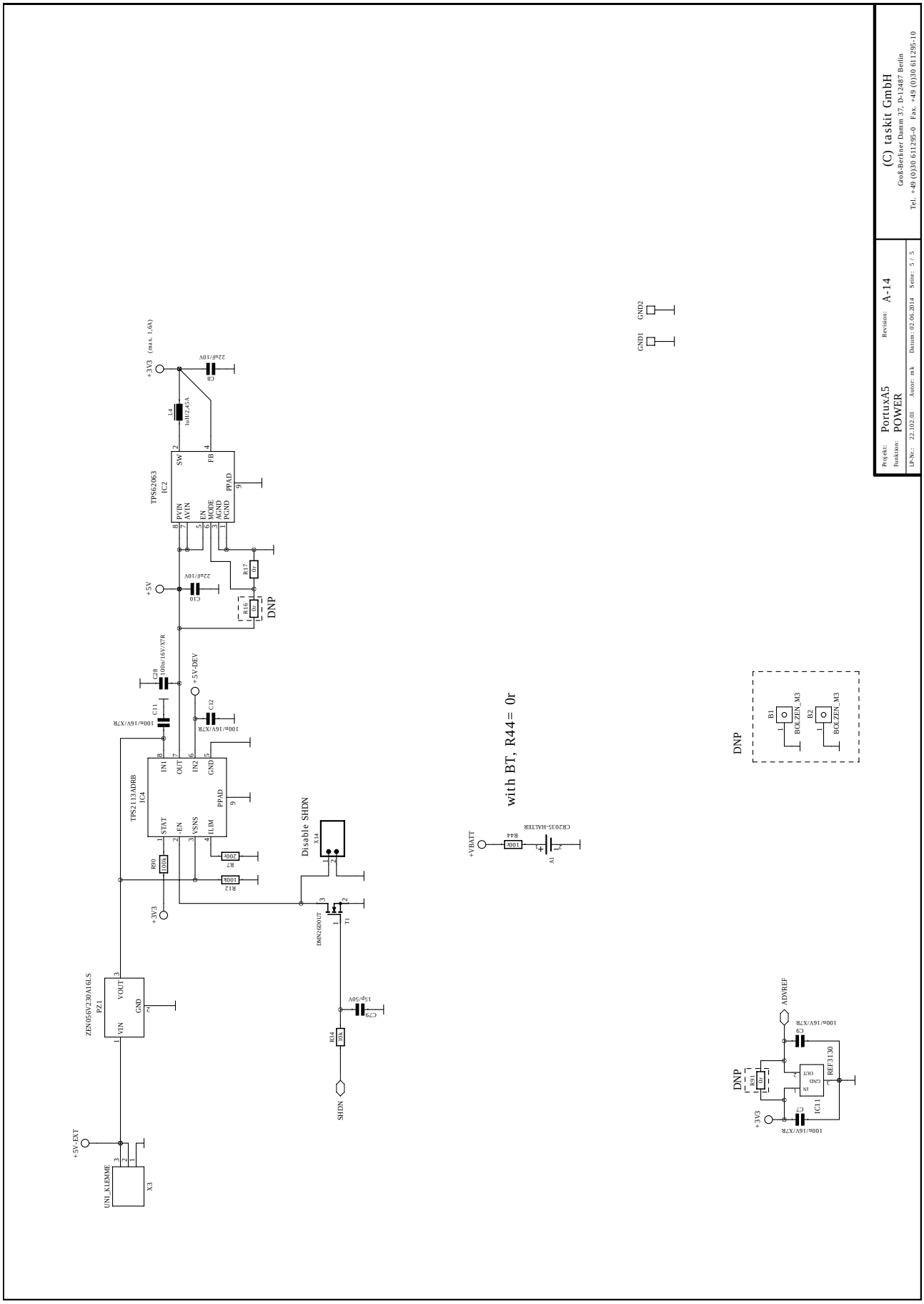


Figure I.5. PortuxA5 Power