

TSL2591

Datasheet - Apr. 2013 - ams163.5

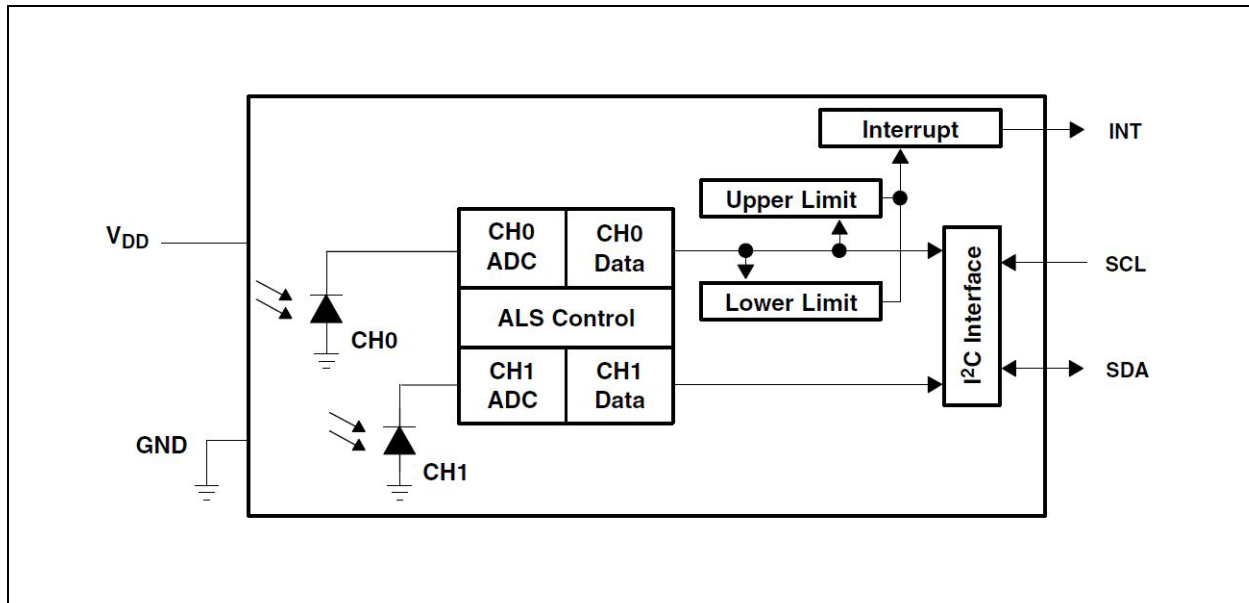
General Description

The TSL2591 is a very-high sensitivity light-to-digital converter that transforms light intensity into a digital signal output capable of direct I²C interface. The device combines one broadband photodiode (visible plus infrared) and one infrared-responding photodiode on a single CMOS integrated circuit. Two integrating ADCs convert the photodiode currents into a digital output that represents the irradiance measured on each channel. This digital output can be input to a microprocessor where illuminance (ambient light level) in lux is derived using an empirical formula to approximate the human eye response. The TSL2591 supports a traditional level style interrupt that remains asserted until the firmware clears it.

Figure TSL2591 – 1:
Key Benefits and Features

| Benefits | Features |
|---|---|
| Approximates Human Eye Response | Dual Diode |
| Flexible Operation | Programmable Analog Gain and Integration Time |
| Suited for Operation Behind Dark Glass | 600M:1 Dynamic Range |
| Low Operating Overhead | <ul style="list-style-type: none"> • Two Internal Interrupt Sources • Programmable Upper and Lower Thresholds • One Interrupt Includes Programmable Persistence Filter |
| Low Power 3.0 μ A Sleep State | User Selectable Sleep Mode |
| I ² C Fast Mode Compatible Interface | <ul style="list-style-type: none"> • Data Rates up to 400 kbit/s • Input Voltage Levels Compatible with 3.0V Bus |

Figure TSL2591 – 2:
Block Diagram



Detailed Description

The TSL2591 contains two integrating analog-to-digital converters (ADC) that integrate currents from two photodiodes. Integration of both channels occurs simultaneously. Upon completion of the conversion cycle, the conversion result is transferred to the Channel 0 and Channel 1 data registers, respectively. The transfers are double-buffered to ensure that the integrity of the data is maintained. After the transfer, the device automatically begins the next integration cycle.

Communication with the device is accomplished through a standard, two-wire I²C serial bus. Consequently, the TSL2591 can be easily connected to a microcontroller or embedded controller. No external circuitry is required for signal conditioning. Because the output of the device is digital, the output is effectively immune to noise when compared to an analog signal.

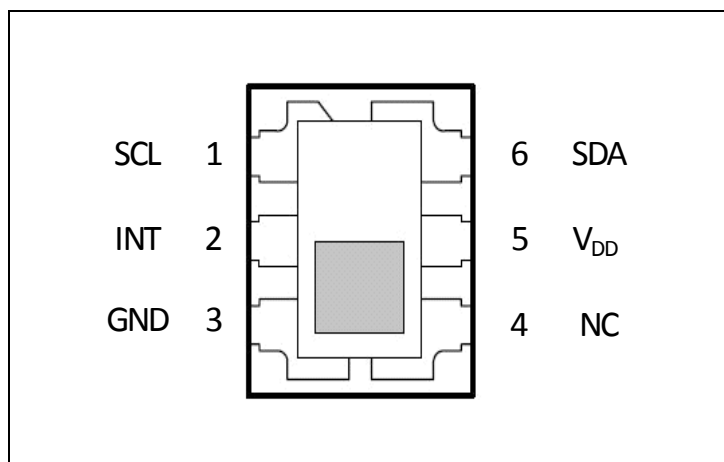
The TSL2591 also supports an interrupt feature that simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity value. The primary purpose of the interrupt function is to detect a meaningful change in light intensity. The concept of a meaningful change can be defined by the user both in terms of light intensity and time, or persistence, of that change in intensity. The device has the ability to define two sets of thresholds, both above and below the current light level. An interrupt is generated when the value of a conversion exceeds either of these limits. One set of thresholds can be configured to trigger an interrupt only when the ambient light exceeds them for a configurable amount of time (persistence) while the other set can be configured to trigger an immediate interrupt.

Pin Assignment

The TSL2591 pin assignments are described below.

**Figure TSL2591 – 3:
Pin Diagram**

Package FN Dual Flat No-Lead (Top View): Package drawing is not to scale.



**Figure TSL2591 – 4:
Pin Description**

| Pin Number | Pin Name | Description |
|------------|-----------------|--|
| 1 | SCL | I ² C serial clock input terminal |
| 2 | INT | Interrupt — open drain output (active low). |
| 3 | GND | Power supply ground. All voltages are referenced to GND. |
| 4 | NC | No connect — do not connect. |
| 5 | V _{DD} | Supply voltage |
| 6 | SDA | I ² C serial data I/O terminal |

Ordering Information

Figure TSL2591 – 5:
Ordering Information

| Ordering Code | Address | Interface | Delivery form |
|---------------|---------|---|---------------|
| TSL25911FN | 0x29 | I ² C V _{bus} = V _{DD} Interface | ODFN-6 |
| TSL25913FN* | 0x29 | I ² C V _{bus} = 1.8V | ODFN-6 |

*Contact factory for availability.

Notes:

1. All products are RoHS compliant and ams green.
2. Buy our products or get free samples online at www.ams.com/ICdirect
3. Technical Support is available at www.ams.com/Technical-Support
4. For further information and requests, email us at sales@ams.com
5. (or) find your local distributor at www.ams.com/distributor
6. Please contact ams for alternate address device availability.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure TSL2591 – 6:
Absolute Maximum Ratings

| Parameter | Min | Max | Units | Comments |
|---|------|------|-------|--------------------------------------|
| Supply voltage, V _{DD} | | 3.8 | V | All voltages are with respect to GND |
| Input terminal voltage | -0.5 | 3.8 | V | |
| Output terminal voltage | -0.5 | 3.8 | V | |
| Output terminal current | -1 | 20 | mA | |
| Storage temperature range, T _{stg} | -40 | 85 | °C | |
| ESD tolerance, human body model | | 2000 | V | |

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure TSL2591 – 7:
Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Units |
|----------|--------------------------------|-----|-----|-----|-------|
| V_{DD} | Supply voltage | 2.7 | 3 | 3.6 | V |
| T_A | Operating free-air temperature | -30 | | 70 | °C |

Figure TSL2591 – 8:
Operating Characteristics, $V_{DD}=3V$, $T_A=25^\circ C$ (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------|-------------------------------------|--|--------------|------------|--------------|---------|
| I_{DD} | Supply Current | Active Sleep state - no I ² C activity | | 275 2.3 | 325 4 | μA |
| V_{OL} | INT, SDA output low voltage | 3mA sink current 6mA sink current | 0 0 | | 0.4 0.6 | V |
| I_{LEAK} | Leakage current, SDA, SCL, INT pins | | -5 | | 5 | μA |
| V_{IH} | SCL, SDA input high voltage | | $0.7 V_{DD}$ | | | V |
| V_{IL} | SCL, SDA input low voltage | | | | $0.3 V_{DD}$ | V |

Figure TSL2591 – 9:
ALS Characteristics, $V_{DD}=3V$, $T_A=25^\circ C$, $AGAIN = Max$, $AEN=1$, (unless otherwise noted) (Notes 1, 2, 3),

| Parameter | Conditions | Channel | Min | Typ | Max | Units |
|---|---|------------|--------|------------------------|----------|-----------------------------|
| Dark ADC count value | $E_e = 0$, ATIME=000b (100ms) | CH0 CH1 | 0 0 | | 25 25 | counts |
| ADC integration time step size | ATIME = 000b (100ms) | | 95 | 101 | 108 | ms |
| ADC number of integration steps (Note 4) | | | 1 | | 6 | steps |
| ADC counts per step | ATIME = 000b (100ms) | | 0 | | 37888 | counts |
| ADC count value | ATIME = 101b (600ms) | | 0 | | 65535 | counts |
| ADC count value | White light (Note 2) $E_e = 4.98 \mu W/cm^2$ ATIME = 000b (100 ms) | CH0 CH1 | 25500 | 30000 4996 | 34500 | counts |
| | $\lambda_p = 850 \text{ nm}$ (Note 3) $E_e = 5.62 \mu W/cm^2$, ATIME = 000b (100 ms) | CH0 CH1 | 25500 | 30000 19522 | 34500 | counts |
| ADC count value ratio: CH1/CH0 | White light (Note 2) | | 0.116 | 0.166 | 0.216 | |
| | $\lambda_p = 850 \text{ nm}$ (Note 3) | | 0.456 | 0.652 | 0.848 | |
| R_e Irradiance responsivity | White light (Note 2) ATIME = 000b (100 ms) | CH0 CH1 | | 6024 1003 | | counts/ ($\mu W/cm^2$) |
| | $\lambda_p = 850 \text{ nm}$ (Note 3) ATIME = 000b (100 ms) | CH0 CH1 | | 5338 3474 | | |
| Noise (Note 4) | White light (Note 2) $E_e = 4.98 \mu W/cm^2$ ATIME = 000b (100 ms) | CH0 | | 1 | 2 | 1 standard deviation |
| Gain scaling, relative to 1× gain setting | AGAIN = Low AGAIN = Med AGAIN = High AGAIN = Max | | | 1 25 428 9876 | | × |

Notes:

- Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Visible white LEDs and infrared 850 nm LEDs are used for final product testing for compatibility with high-volume production
- The white LED irradiance is supplied by a white light-emitting diode with a nominal color temperature of 4000 K.
- The 850 nm irradiance is supplied by a GaAs light-emitting diode with the following typical characteristics: peak wavelength $\lambda_p = 850 \text{ nm}$ and spectral halfwidth $\Delta\lambda_{1/2} = 42 \text{ nm}$.
- Parameter ensured by design and is not 100% tested.

Timing Characteristics

The timing characteristics of TSL2591 are given below.

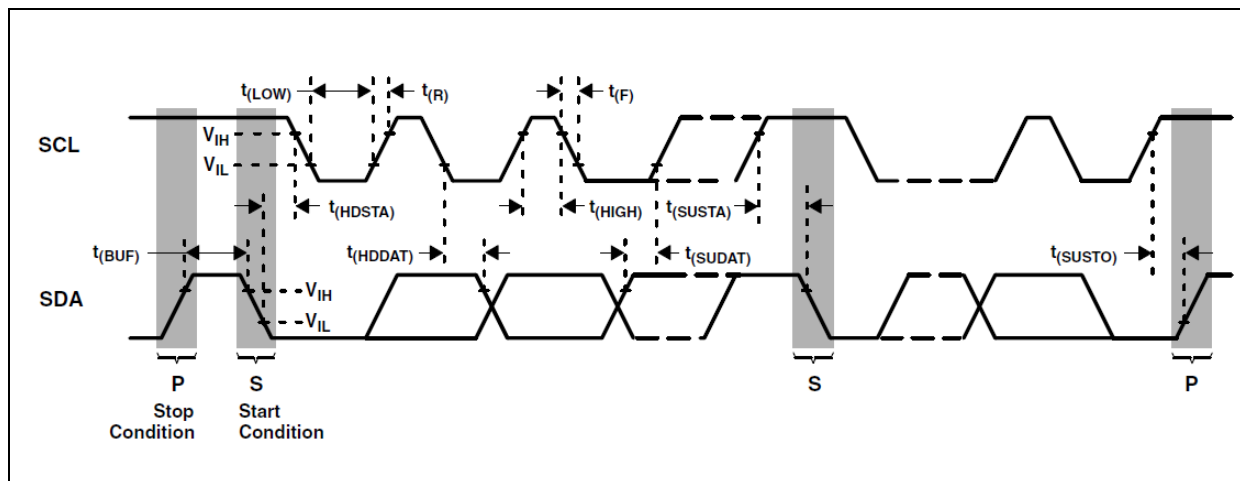
Figure TSL2591 – 10:
AC Electrical Characteristics, $V_{DD} = 3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| Parameter† | Description | Min | Typ | Max | Units |
|---------------|--|-----|-----|-----|---------------|
| $f_{(SCL)}$ | Clock frequency (I ² C only) | 0 | | 400 | kHz |
| $t_{(BUF)}$ | Bus free time between start and stop condition | 1.3 | | | μs |
| $t_{(HDSTA)}$ | Hold time after (repeated) start condition. After this period, the first clock is generated. | 0.6 | | | μs |
| $t_{(SUSTA)}$ | Repeated start condition setup time | 0.6 | | | μs |
| $t_{(SUSTO)}$ | Stop condition setup time | 0.6 | | | μs |
| $t_{(HDDAT)}$ | Data hold time | 0 | | | μs |
| $t_{(SUDAT)}$ | Data setup time | 100 | | | ns |
| $t_{(LOW)}$ | SCL clock low period | 1.3 | | | μs |
| $t_{(HIGH)}$ | SCL clock high period | 0.6 | | | μs |
| t_F | Clock/data fall time | | | 300 | ns |
| t_R | Clock/data rise time | | | 300 | ns |
| C_i | Input pin capacitance | | | 10 | pF |

† Specified by design and characterization; not production tested.

Timing Diagrams

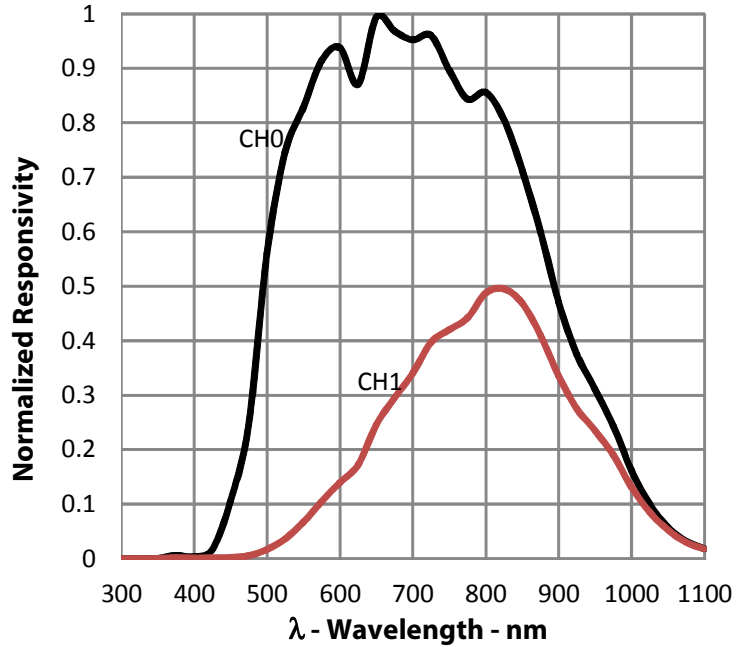
Figure TSL2591 – 11:
Parameter Measurement Information



Typical Operating Characteristics

Spectral Responsivity: Two channel response allows for tunable illuminance (lux) calculation regardless of transmissivity of glass.

**Figure TSL2591 – 12:
Spectral Responsivity**



**Figure TSL2591 – 13:
White Normalized Responsivity vs. Angular Displacement**

White LED Angular Response: Near cosine angular response for broadband white light sources.

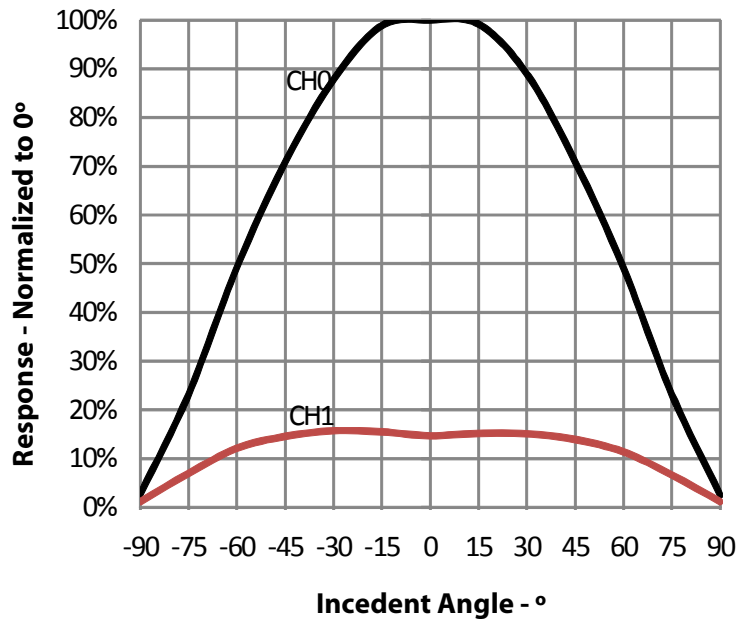


Figure TSL2591 – 14:
Normalized I_{DD} vs. V_{DD} and Temperature

I_{DD} vs. V_{DD} vs. Temp: Effect of supply voltage and temperature on active current.

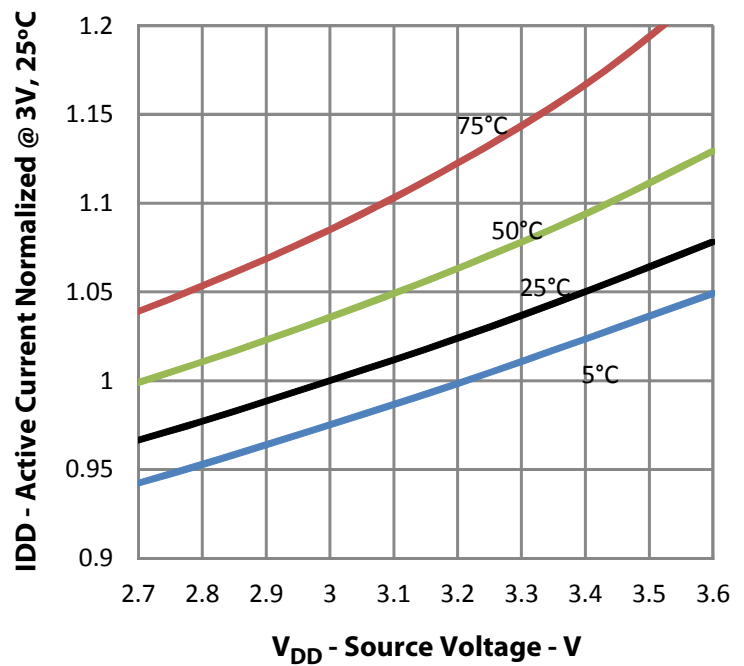
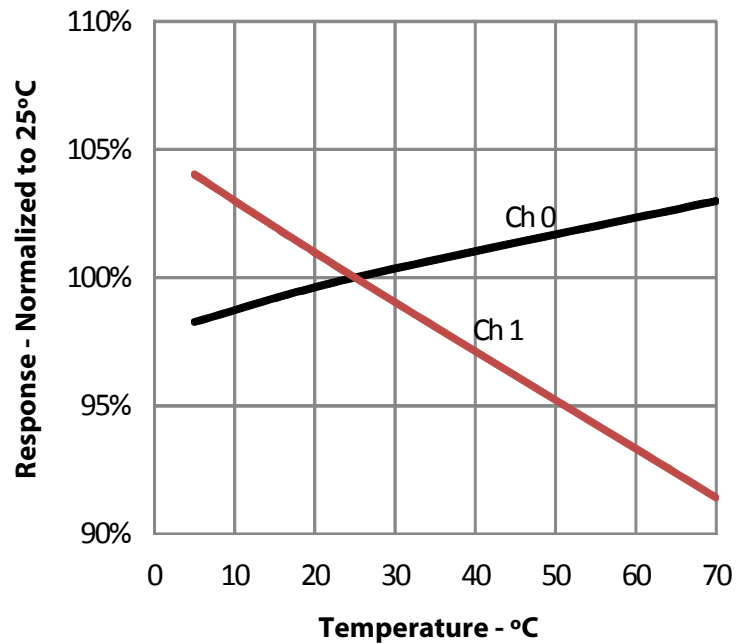


Figure TSL2591 – 15:
Response to White LED vs. Temperature

White LED Response v Temp: Effect of temperature on the device response for a broadband white light source.



Register Description

The device is controlled and monitored by registers accessed through the I²C serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Figure TSL2591 - 16.

**Figure TSL2591 – 16:
Register Description**

| Address | Register Name | R/W | Register Function | Reset Value |
|---------|---------------|-----|---|-------------|
| -- | COMMAND | W | Specifies Register Address | 0x00 |
| 0x00 | ENABLE | R/W | Enables states and interrupts | 0x00 |
| 0x01 | CONFIG | R/W | ALS gain and integration time configuration | 0x00 |
| 0x04 | AILTL | R/W | ALS interrupt low threshold low byte | 0x00 |
| 0x05 | AILTH | R/W | ALS interrupt low threshold high byte | 0x00 |
| 0x06 | AIHTL | R/W | ALS interrupt high threshold low byte | 0x00 |
| 0x07 | AIHTH | R/W | ALS interrupt high threshold high byte | 0x00 |
| 0x08 | NPAILTL | R/W | No Persist ALS interrupt low threshold low byte | 0x00 |
| 0x09 | NPAILTH | R/W | No Persist ALS interrupt low threshold high byte | 0x00 |
| 0x0A | NPAIHTL | R/W | No Persist ALS interrupt high threshold low byte | 0x00 |
| 0x0B | NPAIHTH | R/W | No Persist ALS interrupt high threshold high byte | 0x00 |
| 0x0C | PERSIST | R/W | Interrupt persistence filter | 0x00 |
| 0x11 | PID | R | Package ID | -- |
| 0x12 | ID | R | Device ID | ID |
| 0x13 | STATUS | R | Device status | 0x00 |
| 0x14 | CODATAL | R | CH0 ADC low data byte | 0x00 |
| 0x15 | CODATAH | R | CH0 ADC high data byte | 0x00 |
| 0x16 | C1DATAL | R | CH1 ADC low data byte | 0x00 |
| 0x17 | C1DATAH | R | CH1 ADC high data byte | 0x00 |

Note: JGS-Stopped here.

Command Register

The COMMAND register specifies the address of the target register for future read and write operations, as well as issues special function commands.

| | | | | | | | |
|-----|-------------|---|---------|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMD | TRANSACTION | | ADDR/SF | | | | |

| Fields | Bits | Description | |
|-------------|--|--|---|
| CMD | 7 | Select Command Register. Must write as 1 when addressing COMMAND register. | |
| TRANSACTION | 6:5 | Select type of transaction to follow in subsequent data transfers | |
| | | FIELD VALUE | DESCRIPTION |
| | | 00 | Reserved - Do not use |
| | | 01 | Normal Operation |
| | | 10 | Reserved – Do not use |
| 11 | Special Function – See description below | | |
| ADDR/SF | 4:0 | Address field/special function field. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-data register for subsequent read and write transactions. The field values listed below apply only to special function commands. | |
| | | FIELD VALUE | DESCRIPTION |
| | | 00100 | Interrupt set – forces an interrupt |
| | | 00110 | Clears ALS interrupt |
| | | 00111 | Clears ALS and no persist ALS interrupt |
| | | 01010 | Clears no persist ALS interrupt |
| | | other | Reserved – Do not write |
| | | The interrupt set special function command sets the interrupt bits in the status register (0x13). For the interrupt to be visible on the INT pin, one of the interrupt enable bits in the enable register (0x00) must be asserted. The interrupt set special function must be cleared with an interrupt clear special function. The ALS interrupt clear special functions clear any pending interrupt(s) and are self-clearing. | |

Enable Register (0x00)

The ENABLE register is used to power the device on/off, enable functions and interrupts.

| | | | | | | | |
|-------|-----|----------|------|----------|---|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NPIEN | SAI | Reserved | AIEN | Reserved | | AEN | PON |

| Fields | Bits | Description |
|----------|------|--|
| NPIEN | 7 | No Persist Interrupt Enable. When asserted NP Threshold conditions will generate an interrupt, bypassing the persist filter. |
| SAI | 6 | Sleep after interrupt. When asserted, the device will power down at the end of an ALS cycle if an interrupt has been generated. |
| Reserved | 5 | Reserved. Write as 0. |
| AIEN | 4 | ALS Interrupt Enable. When asserted permits ALS interrupts to be generated, subject to the persist filter. |
| Reserved | 3:2 | Reserved. Write as 0. |
| AEN | 1 | ALS Enable. This field activates ALS function. Writing a one activates the ALS. Writing a zero disables the ALS. |
| PON | 0 | Power ON. This field activates the internal oscillator to permit the timers and ADC channels to operate. Writing a one activates the oscillator. Writing a zero disables the oscillator. |

Control Register (0x01)

The CONTROL register is used to configure the ALS gain and integration time. In addition, a system reset is provided. Upon power up, the CONTROL register resets to 0x00.

| | | | | | | | |
|--------|----------|-------|----------|-------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SRESET | Reserved | AGAIN | Reserved | ATIME | | | |

| Fields | Bits | Description | | |
|----------|------|---|------------------|-----------|
| SRESET | 7 | System reset. When asserted, the device will reset equivalent to a power-on reset. SRESET is self-clearing. | | |
| Reserved | 6 | Reserved. Write as 0. | | |
| AGAIN | 5:4 | ALS gain sets the gain of the internal integration amplifiers for both photodiode channels. | | |
| | | FIELD VALUE | DESCRIPTION | |
| | | 00 | Low gain mode | |
| | | 01 | Medium gain mode | |
| | | 10 | High gain mode | |
| Reserved | 3 | Reserved. Write as 0. | | |
| | | ALS time sets the internal ADC integration time for both photodiode channels. | | |
| | | FIELD VALUE | INTEGRATION TIME | MAX COUNT |
| ATIME | 2:0 | 000 | 100 ms | 37888 |
| | | 001 | 200 ms | 65535 |
| | | 010 | 300 ms | 65535 |
| | | 011 | 400 ms | 65535 |
| | | 100 | 500 ms | 65535 |
| | | 101 | 600 ms | 65535 |

ALS Interrupt Threshold Register (0x04 – 0x0B)

The ALS interrupt threshold registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If C0DATA crosses below the low threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

If the C0DATA exceeds the persist thresholds (registers: 0x04 – 0x07) for the number of persist cycles configured in the PERSIST register an interrupt will be triggered. If the C0DATA exceeds the no-persist thresholds (registers: 0x08 – 0x0B) an interrupt will be triggered immediately following the end of the current integration.

Note that while the interrupt is observable in the STATUS register (0x13), it is visible only on the INT pin when AIEN or NPIEN are enabled in the ENABLE register (0x00).

Upon power up, the interrupt threshold registers default to 0x00.

| Register | Address | Bits | Description |
|----------|---------|------|--|
| AILTL | 0x04 | 7:0 | ALS low threshold lower byte |
| AILTH | 0x05 | 7:0 | ALS low threshold upper byte |
| AIHTL | 0x06 | 7:0 | ALS high threshold lower byte |
| AIHTH | 0x07 | 7:0 | ALS high threshold upper byte |
| NPAILTL | 0x08 | 7:0 | No Persist ALS low threshold lower byte |
| NPAILTH | 0x09 | 7:0 | No Persist ALS low threshold upper byte |
| NPAIHTL | 0x0A | 7:0 | No Persist ALS high threshold lower byte |
| NPAIHTH | 0x0B | 7:0 | No Persist ALS high threshold upper byte |

PERSIST Register (0x0C)

The Interrupt persistence filter sets the number of consecutive out-of-range ALS cycles necessary to generate an interrupt. Out-of-range is determined by comparing C0DATA (0x14 and 0x15) to the interrupt threshold registers (0x04 - 0x07). Note that the no-persist ALS interrupt is not affected by the interrupt persistence filter. Upon power up, the interrupt persistence filter register resets to 0x00.

| | | | | | | | |
|----------|---|---|---|-------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | APERS | | | |

| Field | Bits | Description | |
|----------|------------------------------------|----------------------------------|--|
| Reserved | 7:4 | Reserved. Write as 0. | |
| APERS | 3:0 | ALS interrupt persistence filter | |
| | | FIELD VALUE | PERSISTENCE |
| | | 0000 | Every ALS cycle generates an interrupt |
| | | 0001 | Any value outside of threshold range |
| | | 0010 | 2 consecutive values out of range |
| | | 0011 | 3 consecutive values out of range |
| | | 0100 | 5 consecutive values out of range |
| | | 0101 | 10 consecutive values out of range |
| | | 0110 | 15 consecutive values out of range |
| | | 0111 | 20 consecutive values out of range |
| | | 1000 | 25 consecutive values out of range |
| | | 1001 | 30 consecutive values out of range |
| | | 1010 | 35 consecutive values out of range |
| | | 1011 | 40 consecutive values out of range |
| | | 1100 | 45 consecutive values out of range |
| | | 1101 | 50 consecutive values out of range |
| | | 1110 | 55 consecutive values out of range |
| 1111 | 60 consecutive values out of range | | |

PID Register (0x11)

The PID register provides an identification of the devices package. This register is a read-only register whose value never changes.

| | | | | | | | |
|----------|---|-----------|---|----------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | PACKAGEID | | Reserved | | | |

| Field | Bits | Description |
|----------|------|-----------------------------|
| Reserved | 7:6 | Reserved. |
| PID | 5:4 | Package Identification = 00 |
| Reserved | 3:0 | Reserved. |

ID Register (I0x12)

The ID register provides the device identification. This register is a read-only register whose value never changes.

| | | | | | | | |
|----|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID | | | | | | | |

| Field | Bits | Description |
|-------|------|------------------------------|
| ID | 7:0 | Device Identification = 0x50 |

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

| | | | | | | | |
|----------|---|--------|------|----------|---|--------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | NPINTR | AINT | Reserved | | AVALID | |

| Field | Bits | Description |
|----------|------|--|
| Reserved | 7:6 | Reserved. Write at zero. |
| NPINTR | 5 | No-persist Interrupt. Indicates that the device has encountered a no-persist interrupt condition. |
| AINT | 4 | ALS Interrupt. Indicates that the device is asserting an ALS interrupt. |
| Reserved | 3:1 | Reserved. |
| AVALID | 0 | ALS Valid. Indicates that the ADC channels have completed an integration cycle since the AEN bit was asserted. |

ALS Data Register (0x14 - 0x17)

ALS data is stored as two 16-bit values; one for each channel. When the lower byte of either channel is read, the upper byte of the same channel is latched into a shadow register. The shadow register ensures that both bytes are the result of the same ALS integration cycle, even if additional integration cycles occur between the lower byte and upper byte register readings.

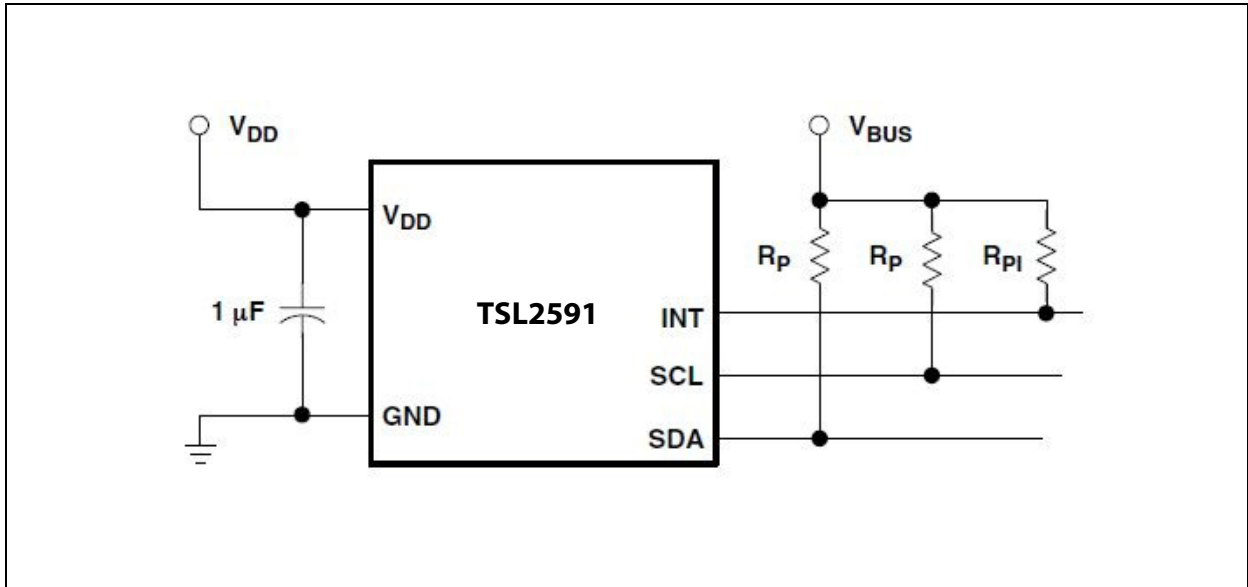
Each channel independently operates the upper byte shadow register. So to minimize the potential for skew between CH0 and CH1 data, it is recommended to read all four ADC bytes in sequence. The simplest way to accomplish this is to perform a four-byte I²C read operation using the auto-increment protocol, which is set in the Command register TRANSACTION field.

| Register | Address | Bits | Description |
|----------|---------|------|------------------------|
| C0DATA_L | 0x14 | 7:0 | ALS CH0 data low byte |
| C0DATA_H | 0x15 | 7:0 | ALS CH0 data high byte |
| C1DATA_L | 0x16 | 7:0 | ALS CH1 data low byte |
| C1DATA_H | 0x17 | 7:0 | ALS CH1 data high byte |

Application Information

Figure TSL2591 - 17 shows a typical hardware application circuit. A 1- μF low-ESR decoupling capacitor should be placed as close as possible to the V_{DD} pin. V_{BUS} in this figure refers to the I²C bus voltage, which is equal to V_{DD} .

Figure TSL2591 – 17:
Typical Application Hardware Circuit

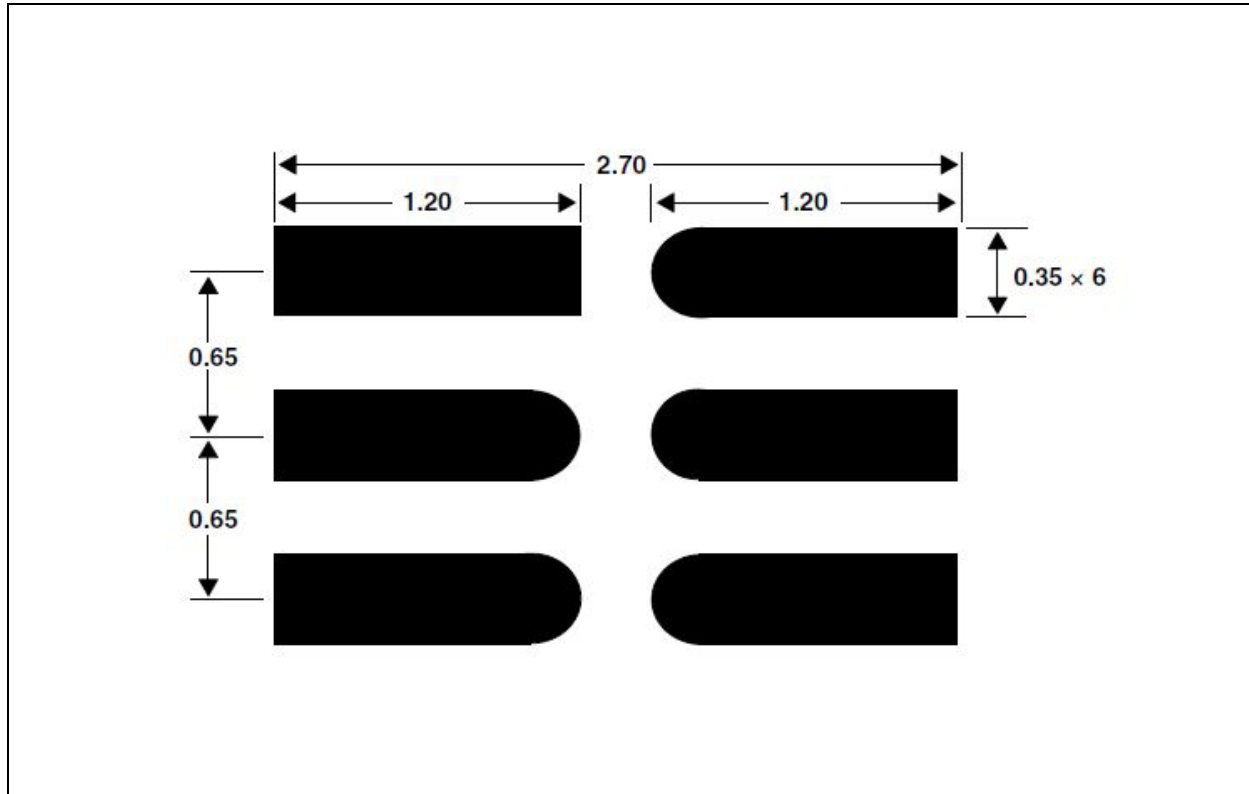


The I²C signals and the Interrupt are open-drain outputs and require pull-up resistors. The pull-up resistor (R_{P}) value is a function of the I²C bus speed, the I²C bus voltage, and the capacitive load. The ams EVM running at 400 kbps, uses 1.5-k Ω resistors. A 10-k Ω pull-up resistor (R_{PI}) can be used for the interrupt line.

PCB Pad Layout

Suggested land pattern based on the IPC-7351B Generic Requirements for Surface Mount Design and Land Pattern Standard (2010) for the small outline no-lead (SON) package is shown in Figure TSL2591 - 18.

Figure TSL2591 – 18:
Suggested FN Package PCB Layout (Top View)

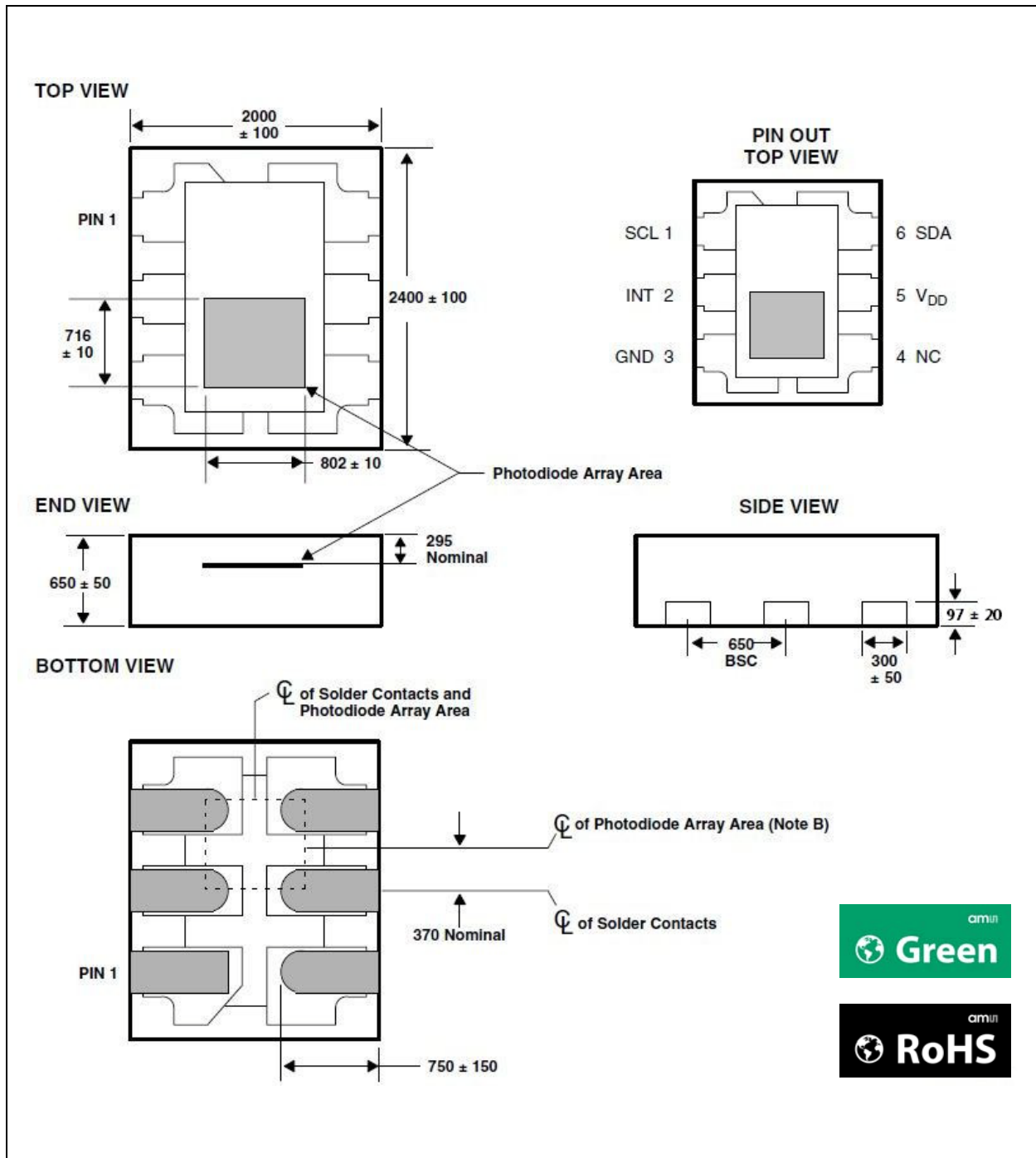


Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

Package Drawings and Markings

Figure TSL2591 – 19:
FN Package – Dual Flat No-Lead Packaging Configuration

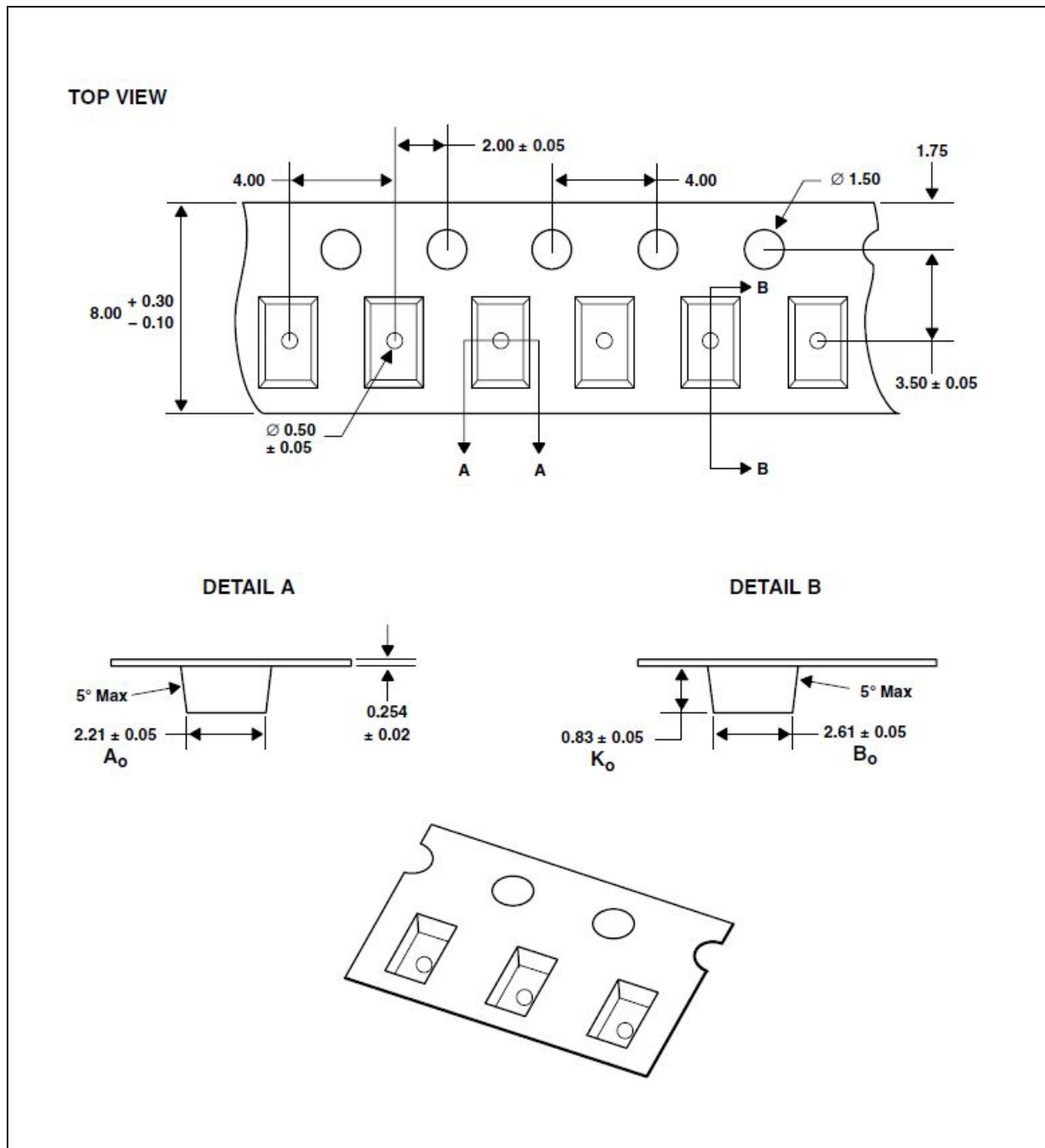


Notes:

1. All linear dimensions are in micrometers.
2. The die is centered within the package within a tolerance of ±75 μm.
3. Package top surface is molded with an electrically non-conductive clear plastic compound having an index of refraction of 1.55.
4. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.

Mechanical Data

Figure TSL2591 – 20:
FN Package Carrier Tape and Reel Information



Notes:

1. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A₀, B₀ and K₀ are defined in ANSI EIA Standard 481-B 2001.
4. Each reel is 178 millimeters in diameter and contains 3500 parts.
5. ams packaging tape and reel conform to the requirements of EIA Standard 481 - B.
6. In accordance with EIA Standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Soldering Information

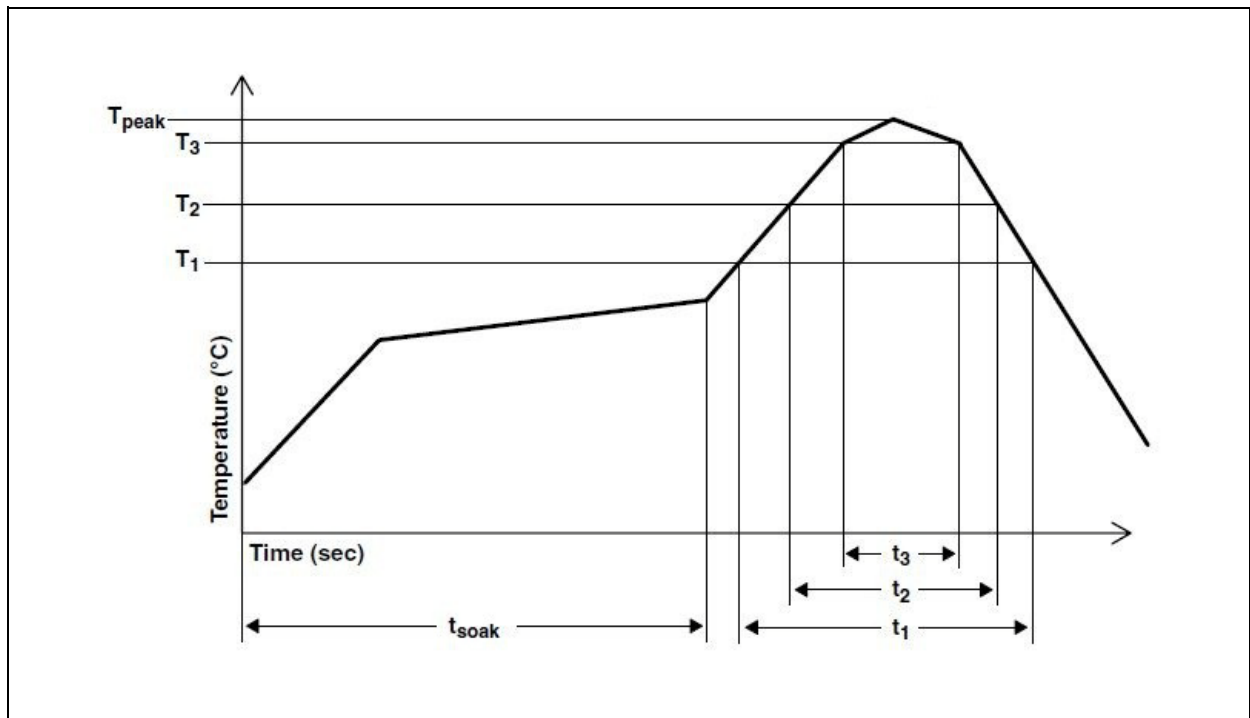
The package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

**Figure TSL2591 – 21:
Solder Reflow Profile**

| Parameter | Reference | Device |
|--|-------------------|----------------|
| Average temperature gradient in preheating | | 2.5 °C/sec |
| Soak time | t_{soak} | 2 to 3 minutes |
| Time above 217 °C (T1) | t_1 | Max 60 sec |
| Time above 230 °C (T2) | t_2 | Max 50 sec |
| Time above $T_{\text{peak}} - 10$ °C (T3) | t_3 | Max 10 sec |
| Peak temperature in reflow | T_{peak} | 260 °C |
| Temperature gradient in cooling | | Max -5 °C/sec |

**Figure TSL2591 – 22:
Solder Reflow Profile Graph**



Note: Not to scale – for reference only.

Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping.

Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: < 40°C
- Relative Humidity: < 90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The FN package has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: < 30°C
- Relative Humidity: < 60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

RoHS Compliant and ams Green Statement

The term RoHS compliant means that ams products fully comply with current RoHS directive. Our semiconductor products do not contain any chemicals for all 6 substance categories, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes. ams Green means RoHS compliant and no Sb/Br). ams defines Green that additionally to RoHS compliance our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

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