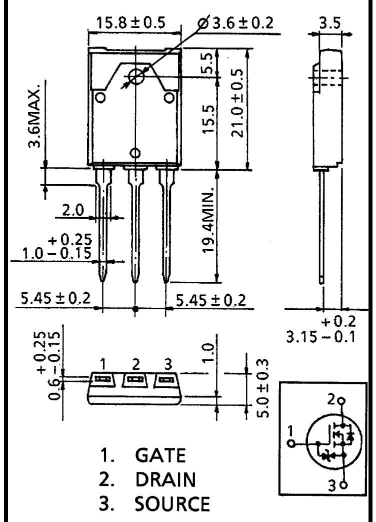
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π−MOSV)

2SK2917

Chopper Regulator, DC−DC Converter and Motor Drive Applications

Unit: mm



JEDEC	―
JEITA	―
TOSHIBA	2-16F1B

Weight: 5.8 g (typ.)

- Low drain–source ON resistance : $R_{DS\ (ON)}$ = 0.21 Ω (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 17 S (typ.)
- Low leakage current : I_{DSS} = 100 μA (max) (V_{DS} = 500 V)
- Enhancement mode : V_{th} = 2.0~4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain–source voltage		V_{DSS}	500	V
Drain–gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	500	V
Gate–source voltage		V_{GSS}	±30	V
Drain current	DC (Note 1)	I_D	18	A
	Pulse (Note 1)	I_{DP}	72	
Drain power dissipation (Ta = 25°C)		P_D	90	W
Single pulse avalanche energy (Note 2)		E_{AS}	915	mJ
Avalanche current		I_{AR}	18	A
Repetitive avalanche energy (Note 3)		E_{AR}	9	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch–c)}$	1.39	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch–a)}$	41.6	°C / W

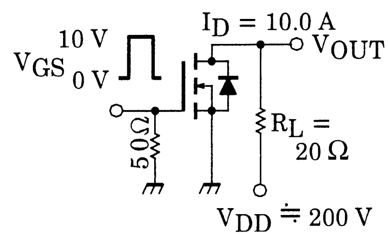
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 4.8 mH, R_G = 25 Ω, I_{AR} = 18 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device.
Please handle with caution.

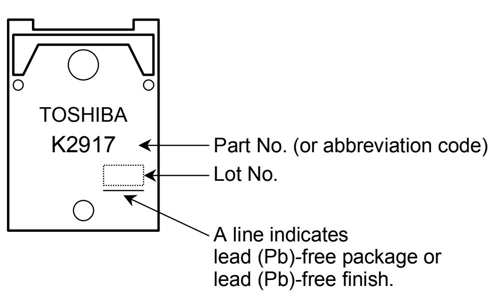
Electrical Characteristics (Ta = 25°C)

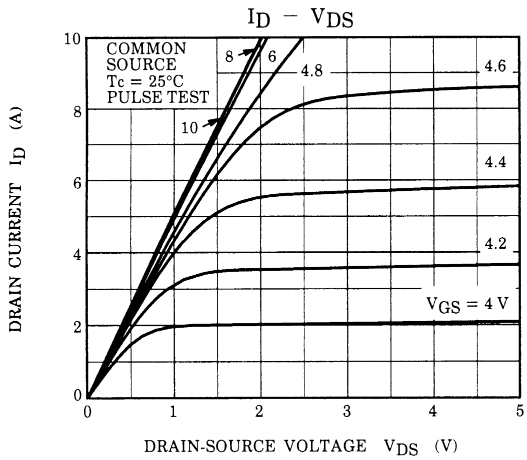
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±25 V, V_{DS} = 0 V	—	—	±10	μA
Gate−source breakdown voltage		$V_{(BR)\ GSS}$	I_G = ±10 μA, V_{DS} = 0 V	±30	—	—	V
Drain cut−off current		I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	—	—	100	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	500	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.0	—	4.0	V
Drain–source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 10 A	—	0.21	0.27	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 10 A	10	17	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	3720	—	pF
Reverse transfer capacitance		C_{rss}		—	340	—	
Output capacitance		C_{oss}		—	1165	—	
Switching time	Rise time	t_r		—	30	—	ns
	Turn−on time	t_{on}		—	70	—	
	Fall time	t_f		—	50	—	
	Turn−off time	t_{off}	Duty ≦ 1%, t_w = 10 μs	—	290	—	
Total gate charge (gate−source plus gate−drain)		Q_g	V_{DD} ≈ 400 V, V_{GS} = 10 V, I_D = 18 A	—	80	—	nC
Gate−source charge		Q_{gs}		—	48	—	
Gate−drain (“miller”) Charge		Q_{gd}		—	32	—	

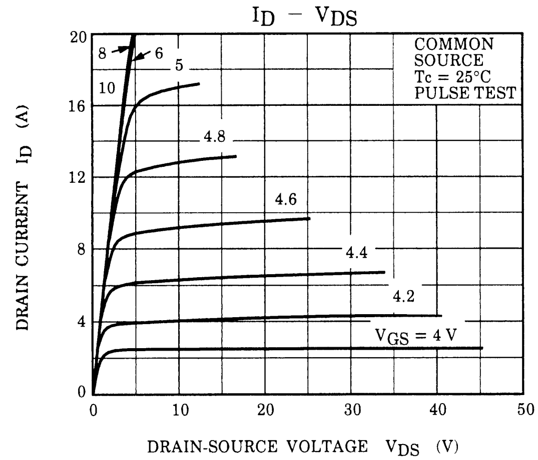
Source−Drain Ratings and Characteristics (Ta = 25°C)

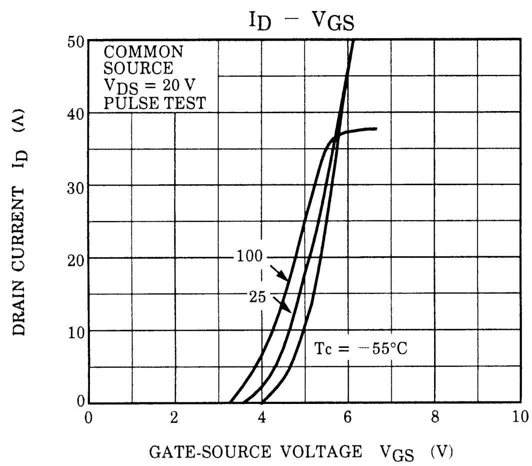
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	18	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	72	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 18 A, V_{GS} = 0 V	—	—	−2.0	V
Reverse recovery time	t_{rr}	I_{DR} = 18 A, V_{GS} = 0 V dI_{DR} / dt = 100 A / μs	—	540	—	ns
Reverse recovery charge	Q_{rr}		—	5.4	—	μC

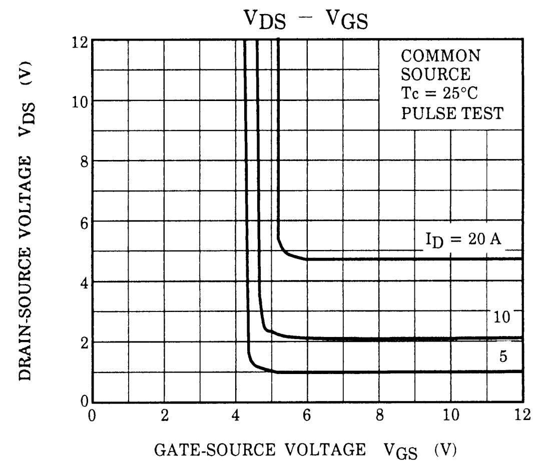
Marking

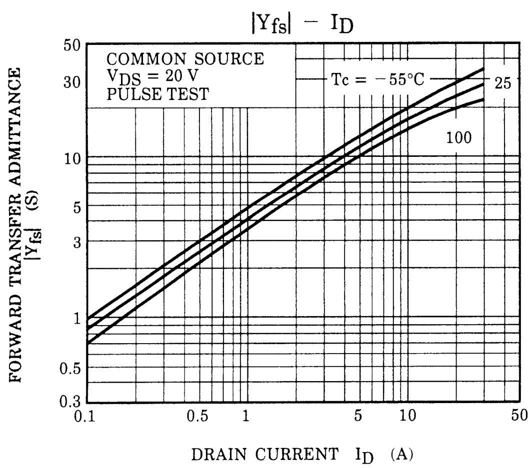


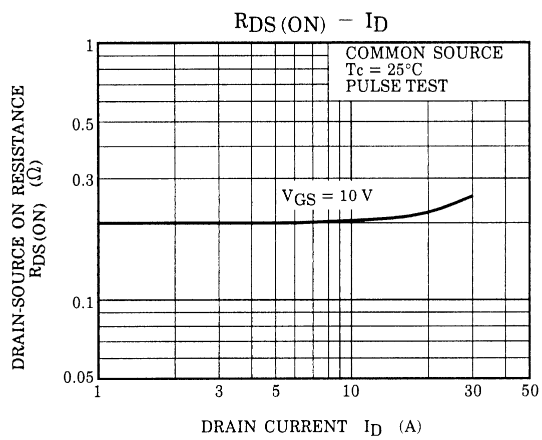

ID – VDS
COMMON SOURCE
Tc = 25°C
PULSE TEST
8
6
4.8
4.6
10
4.4
4.2
VGS = 4 V
DRAIN CURRENT ID (A)
DRAIN-SOURCE VOLTAGE VDS (V)
0
1
2
3
4
5
2
4
6
8
10


ID – VDS
COMMON SOURCE
Tc = 25°C
PULSE TEST
8
6
5
10
4.8
4.6
4.4
4.2
VGS = 4 V
DRAIN CURRENT ID (A)
DRAIN-SOURCE VOLTAGE VDS (V)
0
10
20
30
40
50
4
8
12
16
20

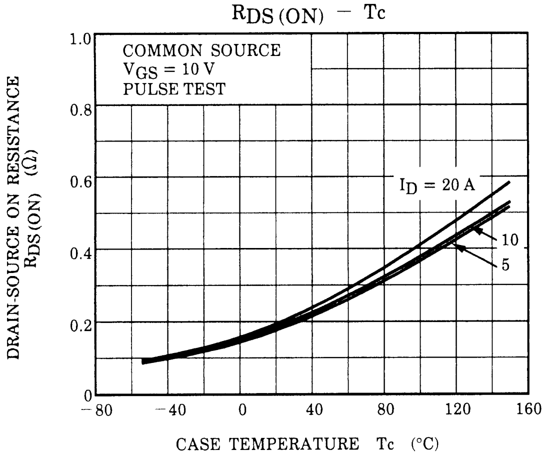

ID – VGS
COMMON SOURCE
VDS = 20 V
PULSE TEST
100
25
Tc = −55°C
DRAIN CURRENT ID (A)
GATE-SOURCE VOLTAGE VGS (V)
0
2
4
6
8
10
20
30
40
50


VDS – VGS
COMMON SOURCE
Tc = 25°C
PULSE TEST
ID = 20 A
10
5
DRAIN-SOURCE VOLTAGE VDS (V)
GATE-SOURCE VOLTAGE VGS (V)
0
2
4
6
8
10
12

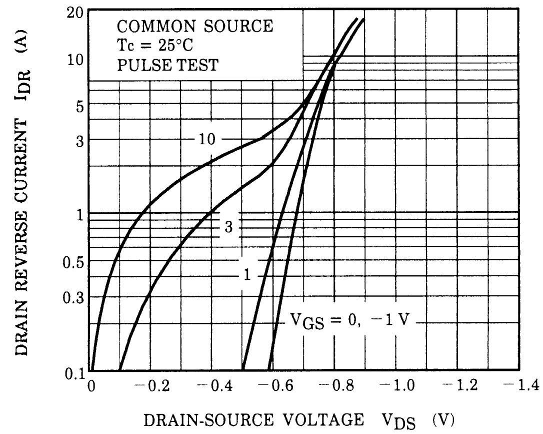

|Yfs| – ID
COMMON SOURCE
VDS = 20 V
PULSE TEST
Tc = −55°C
25
100
FORWARD TRANSFER ADMITTANCE |Yfs| (S)
DRAIN CURRENT ID (A)
0.1
0.5
1
5
10
50
0.3
3
30


RDS (ON) – ID
COMMON SOURCE
Tc = 25°C
PULSE TEST
VGS = 10 V
DRAIN-SOURCE ON RESISTANCE RDS (ON) (Ω)
DRAIN CURRENT ID (A)
0.05
0.1
0.3
0.5
1
3
5
10
30
50

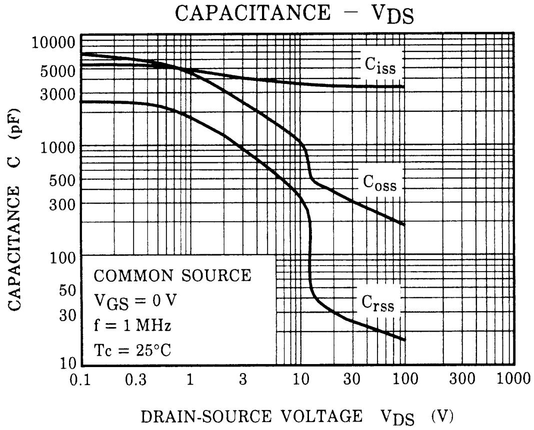
$R_{DS(ON)}$ – Tc



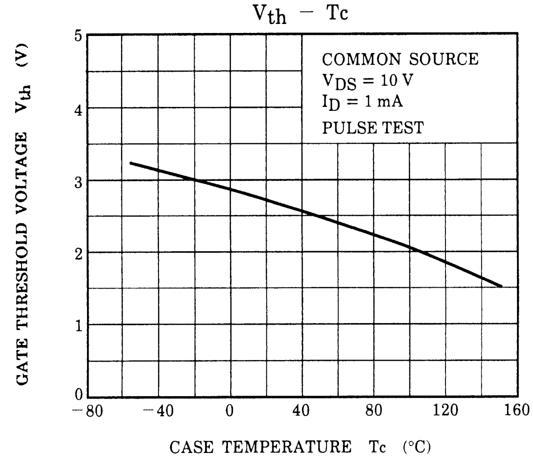
I_{DR} – V_{DS}



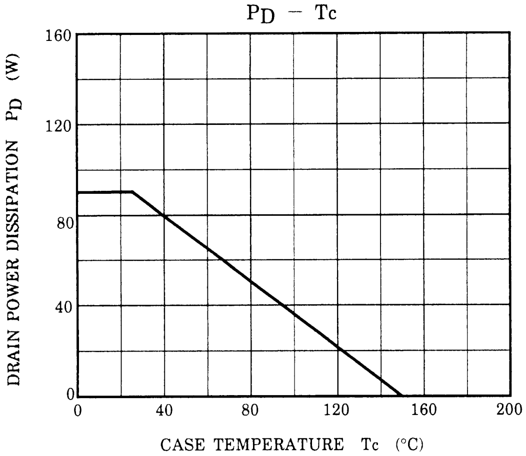
CAPACITANCE – V_{DS}



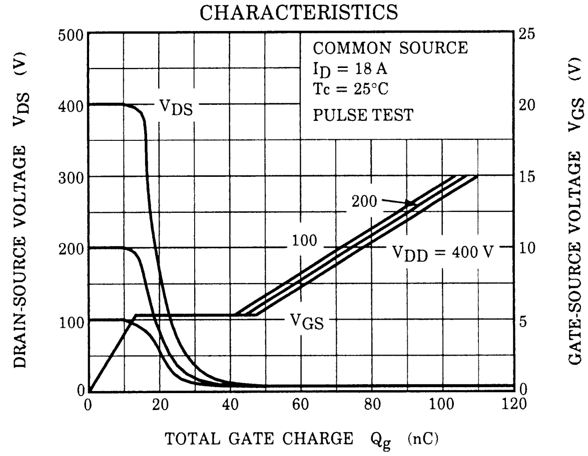
V_{th} – Tc

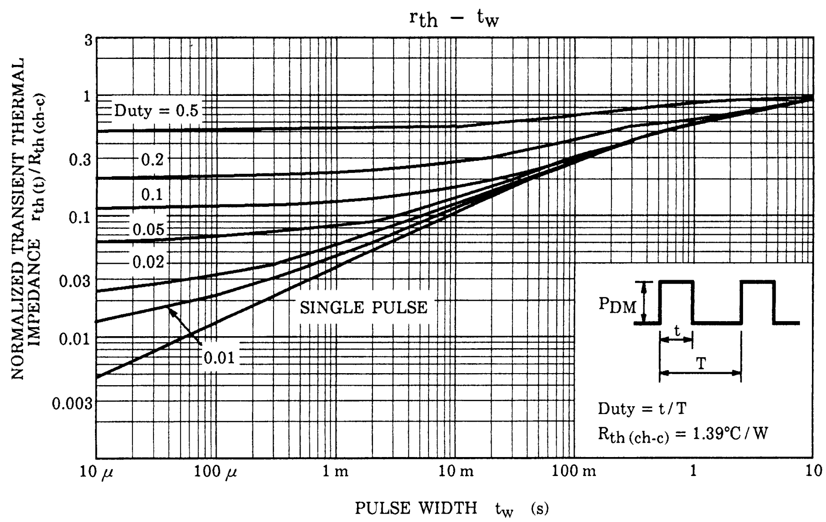


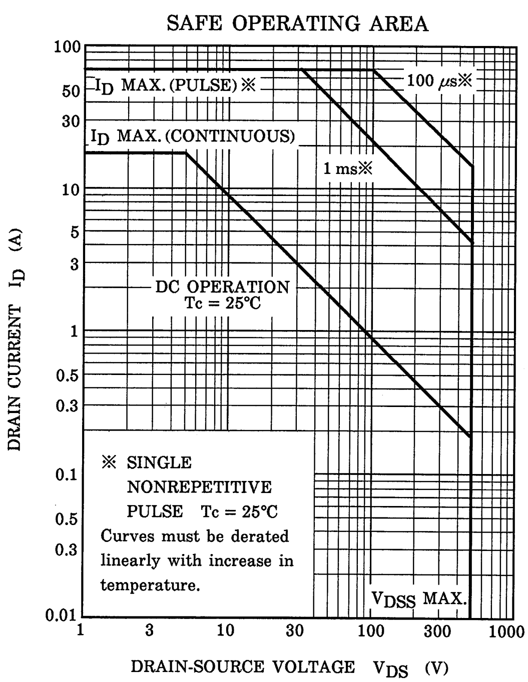
P_D – Tc

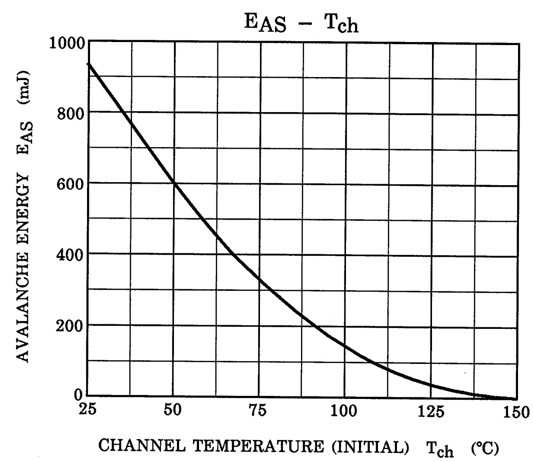


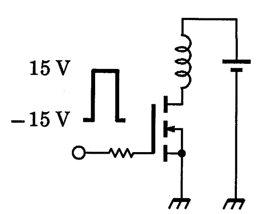
DYNAMIC INPUT / OUTPUT CHARACTERISTICS



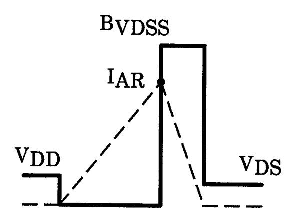








TEST CIRCUIT



WAVE FORM

$R_G = 25\ \Omega$
$V_{DD} = 90\ V$, $L = 4.8\ mH$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

RESTRICTIONS ON PRODUCT USE