



## Evaluating the 3 kV RMS **ADM2561E** and the 5.7 kV RMS **ADM2861E**, 500 kbps Signal and Power Isolated, Half-Duplex RS-485 Transceivers with $\pm 15$ kV IEC ESD

### FEATURES

- Simplified evaluation of the **ADM2561E** and **ADM2861E**
  - 500 kbps half-duplex, isolated RS-485 transceiver
- 2-layer PCB compliant to EN 55032/CISPR 32 Class B radiated emissions
- Footprint for 10.15 mm  $\times$  10.05 mm, 28-lead SOIC\_W\_FP package with 8.3 mm creepage and clearance
- On-board **ADP7104** LDO regulator with jumper options for simplified evaluation in 5 V or 3.3 V configuration
- Flexible, low voltage  $V_{IO}$  supply rail for interfacing with I/O nodes as low as 1.7 V
- ESD protection on RS-485 A, B, Y, and Z pins
  - $\geq \pm 12$  kV IEC61000-4-2 contact discharge
  - $\geq \pm 15$  kV IEC61000-4-2 air discharge
- SMA connector for Tx/D input signal
- Optional on-board **LTC6900** oscillator for providing Tx/D signal
- Screw terminal blocks for connecting power, digital signals, and RS-485 signals
- Jumper selectable enable and disable for digital input signals
- Resistors and footprints for loopback test and termination
- Test points for measuring all signals

### EVALUATION KIT CONTENTS

EVAL-ADM2561EEBZ or EVAL-ADM2861EEBZ

### EQUIPMENT NEEDED

- Oscilloscope
- Signal generator
- 3.0 V to 5.5 V supply
- 1.62 V to 5.5 V supply

### DOCUMENTS NEEDED

- ADM2561E** data sheet
- ADM2861E** data sheet

### GENERAL DESCRIPTION

The EVAL-ADM2561EEBZ and the EVAL-ADM2861EEBZ allow the simplified, efficient evaluation of the 3 kV rms **ADM2561E** and the 5.7 kV rms **ADM2861E** signal and power, isolated half-duplex RS-485 transceivers, respectively. The **ADM2561E** and the **ADM2861E** transceivers are available in a small footprint, 10.15 mm  $\times$  10.05 mm, 28-lead, small outline, wide body, with fine pitch (SOIC\_W\_FP) package. The evaluation boards differ only by the isolated RS-485 device populated on U3.

The **ADM2561E** and the **ADM2861E** feature an integrated, isolated, dc-to-dc converter that provides power to the isolated side of the device with no additional ICs required.

An on-board **ADP7104** low dropout (LDO) regulator accepts an input voltage of 3.3 V to 20 V and regulates the voltage to a selectable 3.3 V or 5 V supply for the  $V_{CC}$  pin of the **ADM2561E** and the **ADM2861E**. The LDO regulator can be bypassed to power the  $V_{CC}$  pin of the **ADM2561E** and the **ADM2861E** directly.

A screw terminal block on the evaluation boards allows connection to the flexible  $V_{IO}$  logic supply pin of the **ADM2561E/ADM2861E**. This connection allows the **ADM2561E/ADM2861E** to operate with a digital input/output (I/O) voltage from 1.7 V to 5.5 V, which enables communication with nodes using either a 1.8 V or 2.5 V power supply. The  $V_{IO}$  pin can also be supplied from the **ADP7104** regulated supply.

Digital and RS-485 bus signals are easily accessible via the screw terminal blocks on each evaluation board. Each digital input is configured via the on-board jumper options.

Alternative methods can provide the transmit data input (Tx/D) signal to the **ADM2561E** or the **ADM2861E**. An **LTC6900** oscillator is included on each evaluation board and can be optionally configured to provide a clock signal for the Tx/D digital input within a 1 kHz to 250 kHz range. For optimal signal integrity, use the on-board Subminiature Version A (SMA) connector to connect an external data signal.

For full details on the **ADM2561E** or the **ADM2861E**, see the **ADM2561E** or the **ADM2861E** data sheet, which must be consulted in conjunction with this user guide when using the EVAL-ADM2561EEBZ and the EVAL-ADM2861EEBZ.

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## REVISION HISTORY

### 6/2020—Rev. 0 to Rev. A

Added EVAL-ADM2861E.....	Universal
Changes to Features Section and General Description Section.....	1
Moved General Description.....	1
Moved Evaluation Board Photographs.....	3
Inserted Figure 2; Renumbered Sequentially.....	3
Changes to Radiated Emissions Section and Figure 3.....	6
Changes to Figure 5.....	7
Changes to Figure 7.....	9
Changes to Table 4.....	11

### 5/2020—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

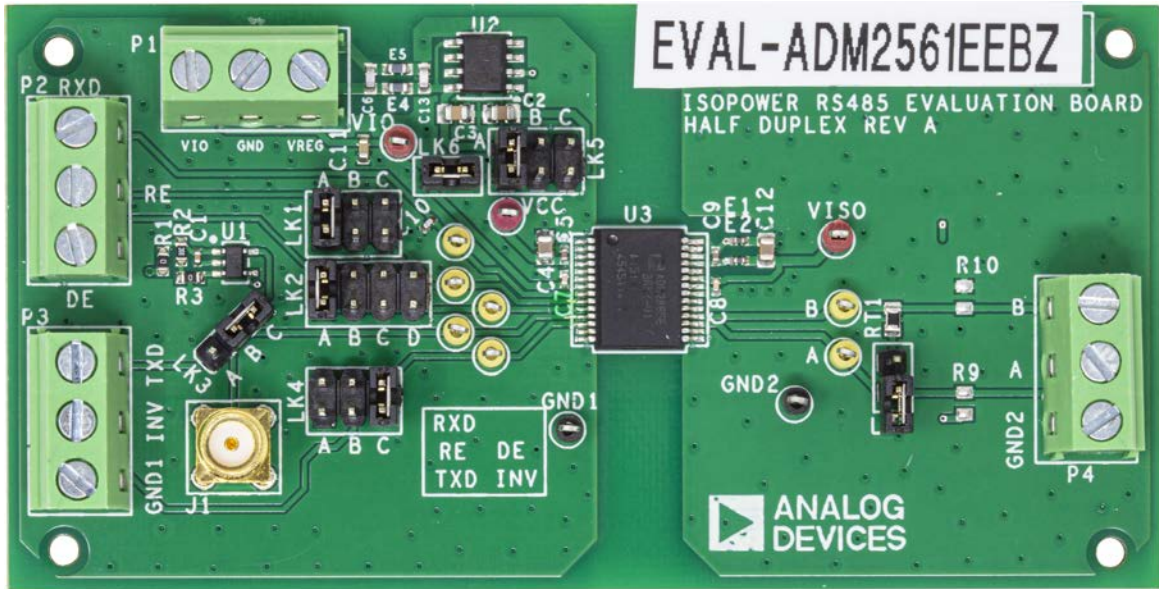


Figure 1. EVAL-ADM2561EEBZ

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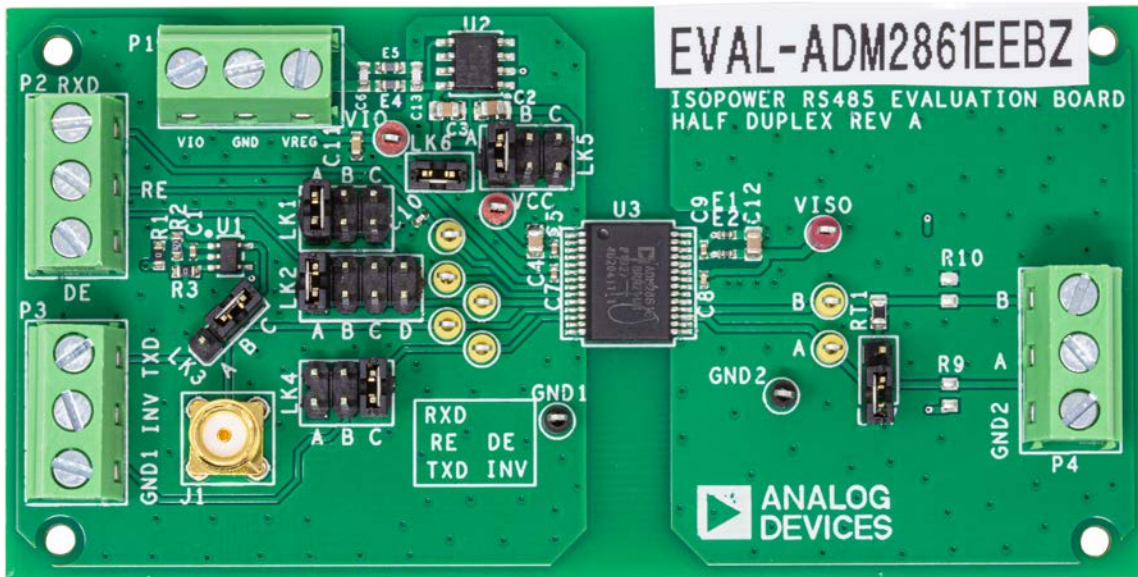


Figure 2. EVAL-ADM2861EEBZ

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## EVALUATION BOARD HARDWARE

### SETTING UP THE EVALUATION BOARD

The EVAL-ADM2561EEBZ and the EVAL-ADM2861EEBZ are powered via the VREG connection on the P1 screw terminal connector. The voltage connected to the VREG terminal on the P1 screw terminal connector can either be regulated or connected directly to the  $V_{CC}$  pin of the [ADM2561E/ADM2861E](#). Insert the LK5 jumper into Position A to power the  $V_{CC}$  pin of the [ADM2561E/ADM2861E](#) directly from the VREG terminal.

The on-board [ADP7104](#) voltage regulator accepts a voltage from 5.5 V to 20 V on the VREG terminal, and can supply either a 3.3 V or a 5 V regulated supply to the  $V_{CC}$  pin of the [ADM2561E/ADM2861E](#). The regulated voltage is selected via the LK5 jumper. Insert the LK5 jumper into Position B to operate the device with a regulated, 3.3 V  $V_{CC}$  supply. Insert the LK5 jumper into Position C to operate the device with a regulated 5 V  $V_{CC}$  supply. The  $V_{CC}$  pin is fitted with a 10  $\mu$ F decoupling capacitor (C4) and a 0.1  $\mu$ F decoupling capacitor (C5).

The  $V_{IO}$  supply pin of the [ADM2561E/ADM2861E](#) can be powered from the VREG terminal block by inserting Jumper LK6 to operate the  $V_{IO}$  and  $V_{CC}$  supply pins at the same voltage.

Alternatively, the  $V_{IO}$  supply pin can be powered from a separate VIO terminal block by removing Jumper LK6. In this configuration, the VIO input of the P1 screw terminal connector can be connected to a separate, low voltage logic supply between 1.7 V and 5.5 V. A 0.1  $\mu$ F decoupling capacitor, C7, is fitted at the connector between  $V_{IO}$  and  $GND_1$ . A footprint for a second 10  $\mu$ F capacitor, C11, can be used to provide additional decoupling capacitance to the  $V_{IO}$  pin.

The  $V_{SEL}$  pin of the [ADM2561E/ADM2861E](#) selects the isolated supply voltage for the RS-485 transceiver. To configure the device to output a 3.3 V isolated supply voltage, connect the [ADM2561E/ADM2861E](#)  $V_{SEL}$  pin to the  $GND_{ISO}$  pins. To configure the device to output a 5 V isolated supply voltage, connect the [ADM2561E/ADM2861E](#)  $V_{SEL}$  pin to the  $V_{ISOOUT}$  pin. The R6 and R7 resistors can be inserted or removed as needed to make these connections. Avoid inserting the R6 and R7 resistors together because this connection shorts the  $V_{ISOOUT}$  power pin to the  $GND_{ISO}$  ground pin.

See Table 1 and Table 2 for details on the jumper and power supply connections. The corresponding labeled test points allow power supply monitoring of the EVAL-ADM2561EEBZ or the EVAL-ADM2861EEBZ with the probe reference connected to ground.

**Table 1. Jumper Configurations**

Link	Jumper Connection	Description
LK1	A	Connects the <a href="#">ADM2561E/ADM2861E</a> $\overline{RE}$ input pin to the $V_{IO}$ pin. This setting disables the receiver.
	B	Connects the <a href="#">ADM2561E/ADM2861E</a> $\overline{RE}$ input pin to the $\overline{RE}$ terminal on the P2 screw terminal connector.
	C	Connects the <a href="#">ADM2561E/ADM2861E</a> $\overline{RE}$ input pin to the $GND_1$ pins. This setting enables the receiver.
LK2	A	Connects the <a href="#">ADM2561E/ADM2861E</a> DE input pin to the $V_{IO}$ pin. This setting enables the driver.
	B	Connects the <a href="#">ADM2561E/ADM2861E</a> DE input pin to the DE terminal on the P2 screw terminal connector.
	C	Connects the <a href="#">ADM2561E/ADM2861E</a> DE input pin to the $GND_1$ pins. This setting disables the driver.
	D	Connects the <a href="#">ADM2561E/ADM2861E</a> DE input pin to the $\overline{RE}$ input signal. Therefore, the input for both $\overline{RE}$ and DE is set by the LK1 jumper. This setting ensures that when the driver is enabled, the receiver is disabled, or when the driver is disabled, the receiver is enabled.
LK3	A and B	Connects the <a href="#">ADM2561E/ADM2861E</a> TxD input pin and J1 SMA connector to the TXD terminal on the P3 screw terminal connector.
	B and C	Connects the <a href="#">ADM2561E/ADM2861E</a> TxD input pin and J1 SMA connector to the <a href="#">LTC6900</a> oscillator output. The oscillator frequency can be configured between 1 kHz and 250 kHz by setting the R2 and R3 resistors. Only use this option when the $V_{IO}$ supply input is between 2.7 V to 5.5 V.
	Not inserted	Connects the <a href="#">ADM2561E/ADM2861E</a> TxD input pin to the J1 SMA connector.
LK4	A	Connects the <a href="#">ADM2561E/ADM2861E</a> INV input pin to the $V_{IO}$ pin. This setting enables the cable inversion feature.
	B	Connects the <a href="#">ADM2561E/ADM2861E</a> INV input pin to the INV terminal on the P3 screw terminal connector.
	C	Connects the <a href="#">ADM2561E/ADM2861E</a> INV input pin to the $GND_1$ pins. This setting is used for normal driver operation.



Link	Jumper Connection	Description
LK5	A	Connects the ADM2561E/ADM2861E V <sub>CC</sub> pin to the VREG terminal on the P1 screw terminal connector. This option bypasses the ADP7104 regulator and allows an external power supply to connect directly to the ADM2561E/ADM2861E V <sub>CC</sub> pin.
	B	Powers the ADM2561E/ADM2861E V <sub>CC</sub> pin with a regulated 3.3 V power supply from the ADP7104. The ADP7104 must be supplied with at least 4 V through the VREG terminal on the P1 screw terminal connector.
	C	Powers the ADM2561E/ADM2861E V <sub>CC</sub> pin with a regulated 5 V power supply from the ADP7104. The ADP7104 must be supplied with at least 6 V through the VREG terminal on the P1 screw terminal connector.
LK6	Inserted	Connects the ADM2561E/ADM2861E V <sub>CC</sub> pin to the V <sub>IO</sub> pin.
	Not inserted	Disconnects the ADM2561E/ADM2861E V <sub>CC</sub> pin from the V <sub>IO</sub> pin. The V <sub>IO</sub> pin is powered from the VIO terminal on the P1 screw terminal connector.
LK7	Inserted	Connects the 120 Ω RT1 termination resistor between the ADM2561E/ADM2861E Pin A and Pin B.
	Not inserted	Disconnects the 120 Ω RT1 termination resistor between the ADM2561E/ADM2861E Pin A and Pin B.

Table 2. Power Supply Configurations

Jumper LK5	V <sub>SEL</sub> Pin	VREG Input Voltage Range	V <sub>CC</sub> Supply	V <sub>ISO</sub> Supply
A	Low	Not used	Power V <sub>CC</sub> directly from the VREG terminal on the P1 screw terminal connector with a supply voltage between 3 V and 5.5 V	3.3 V isolated output
	High	Not used	Power V <sub>CC</sub> directly from the VREG terminal on the P1 screw terminal connector with a supply voltage between 4.5 V and 5.5 V	5 V isolated output
B	Low	4 V to 20 V	Regulator provides 3.3 V supply to V <sub>CC</sub>	3.3 V isolated output
	High	Invalid condition, 5 V isolated output is not supported with V <sub>CC</sub> < 4.5 V		
C	Low	6 V to 20 V	Regulator provides 5 V supply to V <sub>CC</sub>	3.3 V isolated output
	High	6 V to 20 V	Regulator provides 5 V supply to V <sub>CC</sub>	5 V isolated output

### INPUT AND OUTPUT CONNECTIONS

Digital input and output signals are connected via the P2 and P3 screw terminal connectors to allow wire connections from the EVAL-ADM2561EEBZ or the EVAL-ADM2861EEBZ to a signal generator. The evaluation board includes screw terminals for transmit data input (TXD), receiver data output (RXD), receiver enable (RE), driver enable (DE), and the cable inversion (INV) signal. Alternatively, jumper connections can connect these signals to the V<sub>IO</sub> or GND<sub>1</sub> pins of the ADM2561E/ADM2861E (see Table 1).

Connections to the RS-485 bus are made via the P4 screw terminal connector. The EVAL-ADM2561EEBZ or the EVAL-ADM2861EEBZ has two bus input and output signals: Signal A for the noninverting input signal or the noninverting output signal, and Signal B for the inverting input signal or the inverting output signal. The bus cables also include a common ground connection and can be connected to the P4 screw terminal connector of the evaluation board. Test points are available on the evaluation board and are appropriately labeled for all digital and bus input and output signals.

### RADIATED EMISSIONS

The EVAL-ADM2561EEBZ or the EVAL-ADM2861EEBZ is a 2-layer printed circuit board (PCB) that meets the EN 55032 Class B radiated emissions requirements under full load while operating at the maximum data rate. Advances in the isolated dc-to-dc converter eliminate the need for complex mitigation techniques, such as edge guarding and embedded stitching capacitance. Two 0402, surface-mount ferrite beads suppress high frequency noise and minimize the amount of noise radiated by the ADM2561E/ADM2861E device. The recommended ferrite beads have a high impedance in the 100 MHz to 1 GHz frequency range (see Table 3). The EVAL-ADM2561EEBZ or the EVAL-ADM2861EEBZ is populated with BLM15HD182SN1 ferrite beads on E1 and E2.

Table 3. Recommended Surface-Mount Ferrite Beads

Manufacturer	Device Number
Murata Electronics	BLM15HD182SN1
Taiyo Yuden	BKH1005LM182-T

To maximize the margin to the EN 55032 Class B specification, adhere to the following guidelines:

- Ensure that the decoupling capacitors are placed as close to the corresponding ADM2561E/ADM2861E pins as possible.
- Place a 10  $\mu\text{F}$  capacitor (C4) and a 0.1  $\mu\text{F}$  capacitor (C5) between the ADM2561E/ADM2861E  $V_{CC}$  pin and  $\text{GND}_1$  pin.
- Place a 0.1  $\mu\text{F}$  capacitor (C7) between the ADM2561E/ADM2861E  $V_{IO}$  pin and  $\text{GND}_1$  pin.
- Connect the ADM2561E/ADM2861E Pin 24, Pin 26, and Pin 28 together to form a single  $\text{GND}_{\text{ISO}}$  net. Connect this net to the  $\text{GND}_2$  net through the E1 ferrite bead.
- Place a 0.1  $\mu\text{F}$  capacitor (C9) between the ADM2561E/ADM2861E  $V_{\text{ISOOUT}}$  supply pin and  $\text{GND}_{\text{ISO}}$  net.
- Connect the ADM2561E/ADM2861E  $V_{\text{ISOOUT}}$  pin to the  $V_{\text{ISOIN}}$  pin through the E2 ferrite bead.
- Place a 10  $\mu\text{F}$  capacitor (C12) and a 0.01  $\mu\text{F}$  capacitor (C8) between the ADM2561E/ADM2861E  $V_{\text{ISOIN}}$  supply pin and  $\text{GND}_2$  pin (Pin 22).
- Remove any metal planes or floods from the area around or under the  $\text{GND}_{\text{ISO}}$  and  $V_{\text{ISOOUT}}$  net.

The EVAL-ADM2561EEBZ or the EVAL-ADM2861EEBZ is designed according to these guidelines and meets EN 55032 Class B requirements with margin. See Figure 3, Figure 8, and Figure 9 for further details on the recommended PCB layout.

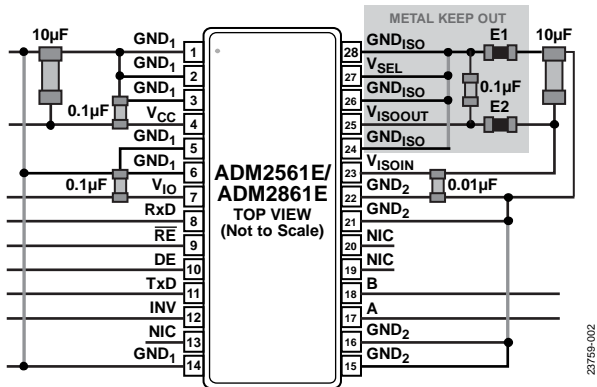


Figure 3. Layout Guidelines to Achieve EN 55032 Class B Requirements

### EN 55032 RADIATED EMISSIONS TEST RESULTS

The EVAL-ADM2561EEBZ or the EVAL-ADM2861EEBZ meets the EN 55032 Class B and CISPR 32 requirements for radiated emissions with margin. The testing was performed in worst case conditions under a full 54  $\Omega$  load with both the transmitter and the receiver switching at 500 kbps. Figure 4 shows the results obtained in a 10 meter, semianechoic chamber, which are below the Class B limit.

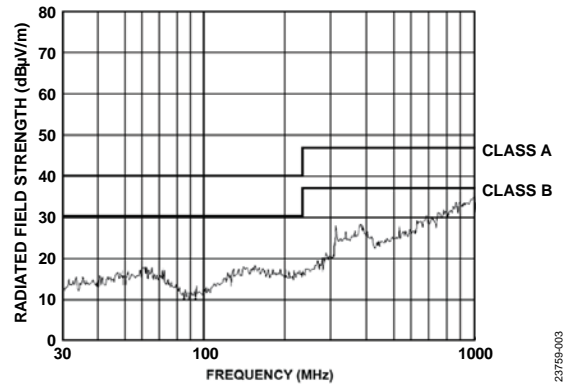


Figure 4. CISPR 32/EN 55032 Radiated Emissions Results

### OTHER BOARD COMPONENTS

The EVAL-ADM2561EEBZ or the EVAL-ADM2861EEBZ has footprints for the RT1 termination resistor. A 120  $\Omega$  termination resistor is fitted to the evaluation board, but this resistor can be removed or replaced with a resistor of a different value as needed. Insert the LK7 jumper to add a 120  $\Omega$  load to the RS-485 driver.

### Biasing Resistors for Bus Idle Fail-Safe

The ADM2561E/ADM2861E has a built in receiver fail-safe for the bus idle condition, but there are footprints on the evaluation board for fitting the R9 pull-up resistor to the VISO supply on the ADM2561E/ADM2861E Pin A, as well as the R10 pull-down resistor to the  $\text{GND}_2$  supply on Pin B. These resistors can be fitted if the user is connecting to other devices that require external biasing resistors on the bus. The exact value required for a 200 mV minimum differential voltage in bus idle condition depends on the minimum supply voltage and the termination scheme. For 5 V transceiver operation, 1140  $\Omega$  is recommended. For 3.3 V transceiver operation, 900  $\Omega$  is recommended.

See the AN-960 Application Note for more information about the bus idle fail-safe.

**On-Board LTC6900 Oscillator**

An LTC6900 oscillator is provided on the evaluation board to allow efficient evaluation of the device without the need for an external signal source.

To use the LTC6900 oscillator for evaluation, insert the LK3 jumper between Position B and Position C. This setting connects the oscillator output (LTC6900) to the ADM2561E/ADM2861E TxD input pin.

The R2 and R3 resistors configure the switching frequency of the clock oscillator within the 10 kHz to 250 kHz range. Use the following equation to calculate the frequency:

$$f_{osc} = 10 \text{ MHz} \left( \frac{20 \text{ k}\Omega}{10(R2 + R3)} \right), 80 \text{ k}\Omega \leq (R2 + R3) \leq 2 \text{ M}\Omega$$

where  $f_{osc}$  is the output frequency of the LTC6900 oscillator.

The LTC6900 oscillator is powered from the V<sub>IO</sub> supply and must only be used when the V<sub>IO</sub> supply voltage is between 2.7 V and 5.5 V. The LTC6900 oscillator can be removed from the V<sub>IO</sub> supply by removing the R1 0 Ω resistor.

**ADP7104 LDO Regulator**

The EVAL-ADM2561EEBZ or the EVAL-ADM2861EEBZ features an on-board ADP7104 LDO regulator that allows flexible power supply configurations during evaluation.

To use the on-board LDO regulator, insert the LK5 jumper into Position B or Position C. This setting connects the regulator output to the V<sub>CC</sub> pin of the ADM2561E/ADM2861E. In this configuration, power must be supplied to the VREG input on the P1 screw terminal connector.

The ADP7104 LDO regulator can be configured to provide regulated 3.3 V or 5 V power to the V<sub>CC</sub> pin of the ADM2561E via the LK5 jumper. When using the ADP7104 regulator, insert the LK5 jumper at Position C to provide regulated 5 V power to the V<sub>CC</sub> pin of the ADM2561E/ADM2861E. Insert the LK5 jumper at Position B to provide 3.3 V power to the V<sub>CC</sub> pin of the ADM2561E/ADM2861E. When LK5 is inserted at Position B, 5 V transceiver operation is not supported.

Insert the LK5 jumper into Position A to bypass the regulator and power the ADM2561E/ADM2861E directly from the VREG input on the P1 screw terminal connector. In this configuration, the VREG input on the P1 screw terminal connector supports a voltage range of 3 V to 5.5 V.

Table 2 lists the supported power supply configurations and the associated jumper configurations.

**RS-485 TRANSCEIVER LOOPBACK TEST**

A loopback test can be set up with the EVAL-ADM2561EEBZ or the EVAL-ADM2861EEBZ. The ADM2561E/ADM2861E is half-duplex and is already configured to easily perform a loopback test. The details of this test are shown in Table 2 and in Figure 5. A signal generator is connected to the TxD pin, which allows verification of the bus signals and the receiver output. To enable both the driver and receiver for the test, set the jumper position for LK1 to Position C, LK2 to Position A, and LK4 to Position C on the evaluation board. See Table 2 for the jumper configurations for different power supply configurations. Insert the LK7 jumper to conduct the test with a 120 Ω load present on the RS-485 outputs.

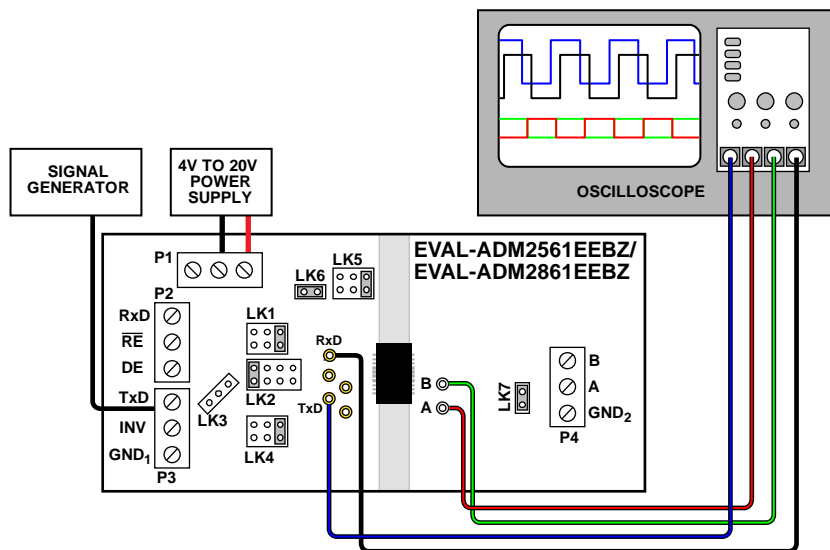


Figure 5. Half-Duplex RS-485 Loopback Test

## IEC 61000-4-2 ELECTROSTATIC DISCHARGE (ESD) PROTECTION

The EVAL-ADM2561EEBZ or the EVAL-ADM2861EEBZ is tested to achieve protection against IEC 61000-4-2 ESD to  $\geq \pm 12$  kV (contact) and  $\geq \pm 15$  kV (air) on Pin A and Pin B of the [ADM2561E/ADM2861E](#).

The IEC 61000-4-2 ESD standard describes testing using two coupling methods known as contact discharge and air discharge. Contact discharge implies a direct contact between the discharge gun and the equipment under test (EUT).

During air discharge testing, the charged electrode of the discharge gun is moved toward the EUT until a discharge occurs as an arc across the air gap. The discharge gun does not make direct contact with the EUT.

During testing, Pin A and Pin B of the [ADM2561E/ADM2861E](#) are subjected to at least 10 positive and 10 negative single discharges with a 1 sec interval between each pulse. The highest specified IEC 61000-4-2 ESD test is Level 4, which

defines a contact discharge voltage of  $\pm 8$  kV and an air discharge voltage of  $\geq \pm 15$  kV.

Figure 6 shows the ESD waveform for an 8 kV contact discharge current waveform as described in the [ADM2561E/ADM2861E](#) data sheet, which has a peak current ( $I_{PEAK}$ ) of 30 A. Important IEC 61000-4-2 waveform parameters include rise times of  $< 1$  ns and pulse widths of  $\sim 60$  ns.

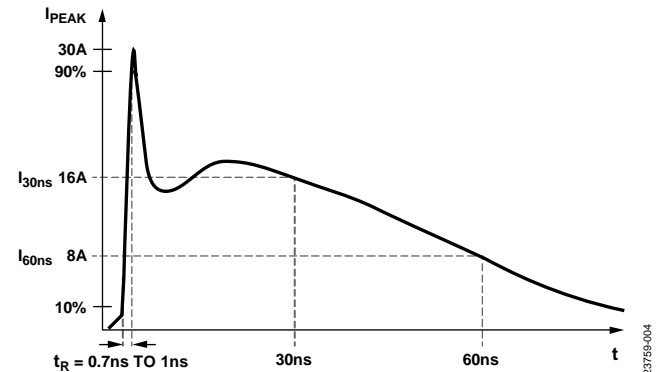


Figure 6. IEC 61000-4-2 ESD Waveform (8 kV)



EVALUATION BOARD SCHEMATICS AND ARTWORK

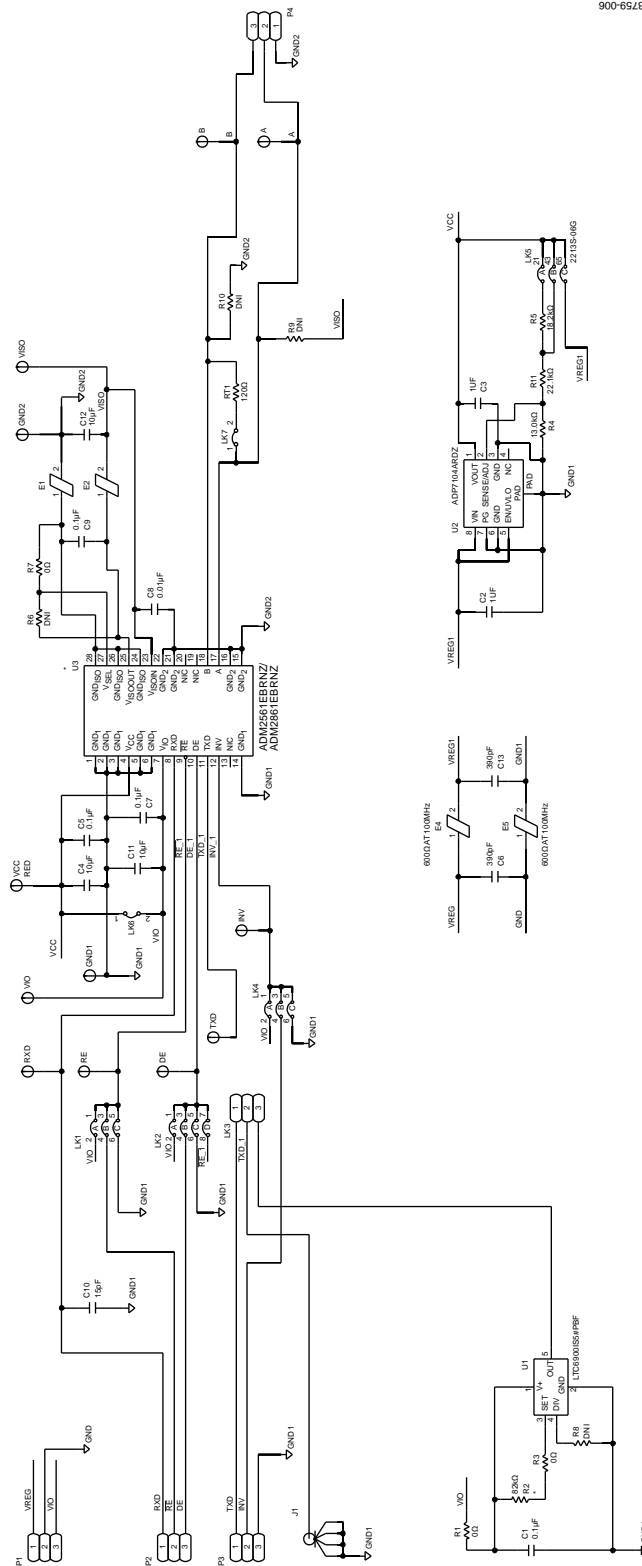


Figure 7. EVAL-ADM2561EEBZ/EVAL-ADM2861EEBZ Schematic

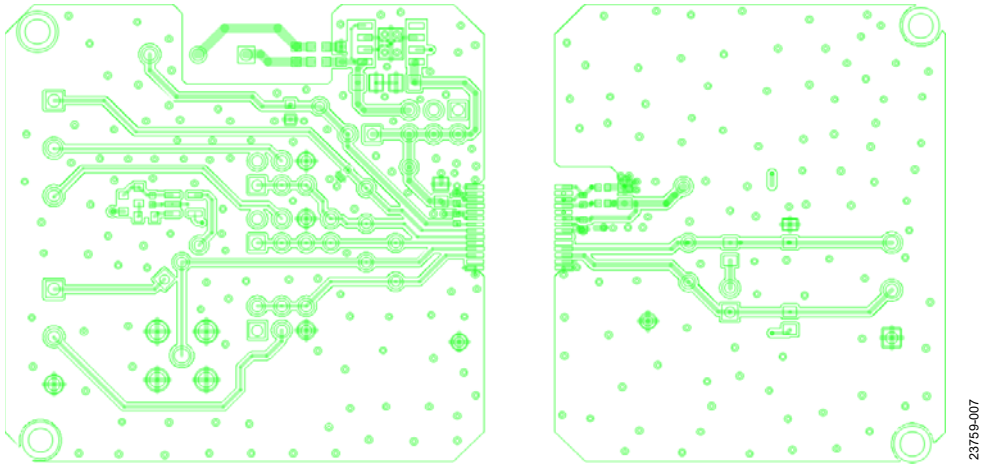


Figure 8. EVAL-ADM2561EEBZ/EVAL-ADM2861EEBZ Component Side, Layer 1

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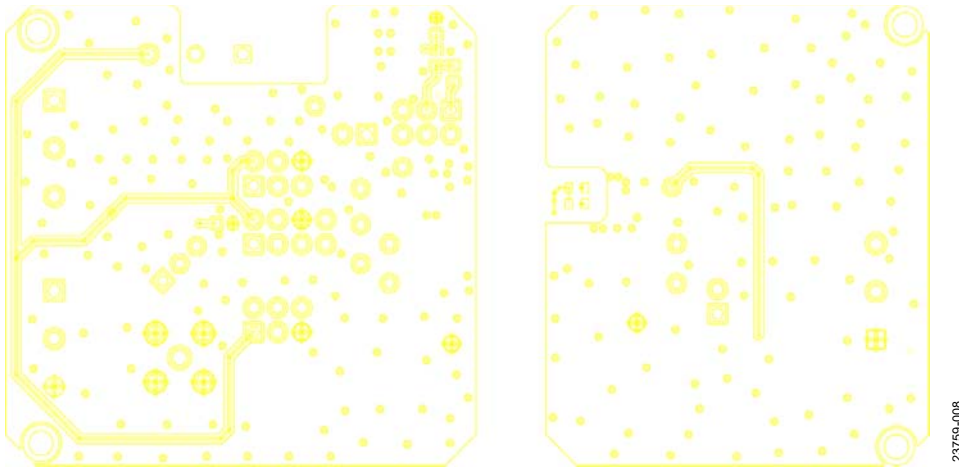


Figure 9. EVAL-ADM2561EEBZ/EVAL-ADM2861EEBZ, Layer 2

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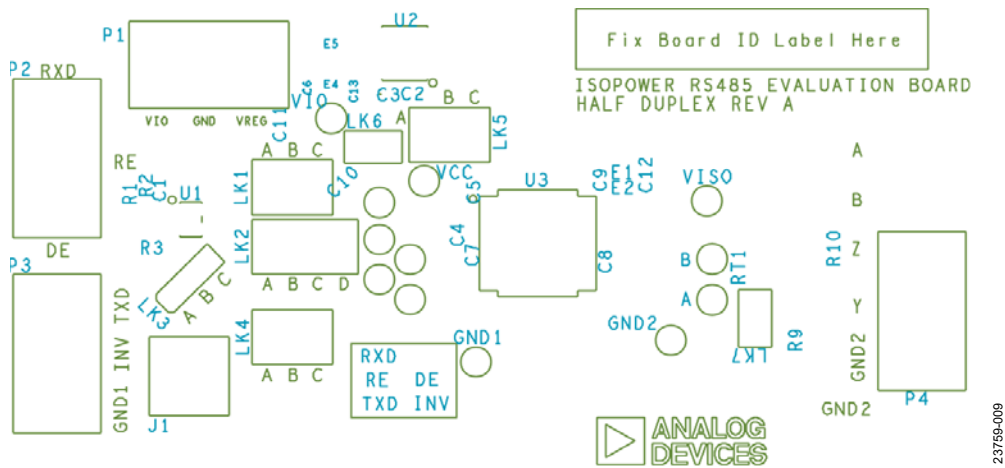


Figure 10. EVAL-ADM2561EEBZ/EVAL-ADM2861EEBZ, Silkscreen

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## ORDERING INFORMATION

## BILL OF MATERIALS

Table 4. EVAL-ADM2561EEBZ/EVAL-ADM2861EEBZ Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Part Number
7	A, B, DE, INV, RE, RXD, TXD	Test points, yellow	Keystone Electronics	36-5004-ND
4	C1, C5, C7, C9	Capacitors, 0.1 $\mu$ F, 0402	Kemet	C0402C104K4RACTU
2	C2, C3	Capacitors, 1 $\mu$ F, 0805	Murata	GCM21BR71E105KA56L
2	C4, C12	Capacitors, 10 $\mu$ F, 0805	TDK	C2012X5R1E106K085AC
2	C6, C13	Capacitors, 390 pF, 0603	AVX Corporation	0603YC391KAT2A
1	C8	Capacitor, 0.01 $\mu$ F, 0402	Murata	GCM155R71H103KA55D
1	C10	Capacitor, 15 pF, 0402	Murata	GCM1555C1H150FA16D
1	C11	Capacitor, 10 $\mu$ F, 0603	TDK	C1608X5R1A106M080AC
2	E1, E2	Ferrite beads, 0402	Murata	BLM15HD182SN1
2	E4, E5	Ferrite beads, 0603, 600 $\Omega$ at 100 MHz	Murata	BLM18HE601SN1D
2	GND1, GND2	Test points, black	Components Corporation	TP-105-01-00
1	J1	Coaxial, straight SMA connector	TE Connectivity	5-1814832-1
3	LK1, LK4, LK5	6-pin (3 $\times$ 2), 0.1 inch header and shorting blocks	Multicomp	2213S-06G
1	LK2	8-pin (4 $\times$ 2), 0.1 inch header and shorting block	Multicomp	2213S-08G
1	LK3	3-pin (3 $\times$ 1), 0.1 inch header and shorting block	Molex	22-28-4033
2	LK6, LK7	2-pin (1 $\times$ 2), 0.1 inch header and shorting blocks	Harwin	M20-9990246
4	P1 to P4	Three-way screw terminal connectors	Würth Elektronik	691131710003
3	R1, R3, R7, R8	Resistors, 0 $\Omega$ , 0603	Vishay	CRCW0603000ZRT1
1	R2	Resistor, 20 k $\Omega$ , 0603	Panasonic	ERJ-3EKF2002V
1	R4	Resistor, 13 k $\Omega$ , 0603	Panasonic	ERJ-3EKF1302V
1	R5	Resistor, 18.2 k $\Omega$ , 0603	Panasonic	ERJ-3EKF1822V
1	R6	Resistor, do not install (DNI), 0 $\Omega$ , 0603	Not applicable	Not applicable
1	R11	Resistor, 22.1 k $\Omega$ , 0603	Panasonic	ERJ-3EKF2212V
2	R9, R10	Resistors, DNI, 0805	Not applicable	Not applicable
1	RT1	Resistor, 120 $\Omega$ , 0805	Panasonic	ERJ-P6WF1200V
1	U1	Low power, 1 kHz to 20 MHz oscillator	Analog Devices, Inc.	<a href="#">LTC6900IS5#PBF</a>
1	U2	Low noise, CMOS LDO	Analog Devices	<a href="#">ADP7104ARDZ-R7</a>
1	U3 <sup>1</sup>	500 kbps, 3 kV signal, and power isolated RS-485 transceiver	Analog Devices	<a href="#">ADM2561EEBZ</a>
1	U3 <sup>1</sup>	500 kbps, 5.7 kV signal, and power isolated RS-485 transceiver	Analog Devices	<a href="#">ADM2861EEBZ</a>
3	VCC, VIO, VISO	Test points, red	Components Corporation	TP-105-01-02

<sup>1</sup> The [ADM2561E](#) is the device for the EVAL-ADM2561EEBZ, and the [ADM2861E](#) is the device for the EVAL-ADM2861EEBZ board.

## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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