CrossLink-NX Evaluation Board

User Guide

FPGA-EB-02028-1.3

November 2020

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
caBGA	Chip Array Ball Grid Array
CMOS	Complementary Metal-Oxide Semiconductor
DIP	Dual Inline Package
DNI	Do Not Install
ESD	Electro Static Discharge
FMC LPC	FPGA Mezzanine Low Pin Count Connector
FPGA	Field Programmable Logic Array
FTDI	Future Technology Devices International
GPIO	General Purpose Input/Output
I^2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LVDS	Low-Voltage Differential Signaling
PMOD	Peripheral Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

1. Introduction

The Lattice Semiconductor CrossLink™-NX Evaluation Board allows designers to investigate and experiment with the features of the CrossLink-NX Field Programmable Gate Array (FPGA). The features of the CrossLink-NX Evaluation Board can assist engineers with the rapid prototyping and testing of their specific designs.

The CrossLink-NX Evaluation Board is part of the CrossLink-NX Evaluation Kit, which includes the following:

- CrossLink-NX Evaluation Board pre-loaded with the shipping demo design
- 12 V AC/DC power adapter and international plug adapters
- Lattice Radiant® Software license information
- USB-A to USB-B (Mini) Cable for programming FPGA through a PC
- Quick Start Guide

The contents of this user guide include top-level functional descriptions of the various portions of the development board, descriptions of the on-board headers, diodes and switches and a complete set of schematics.

1.1. CrossLink-NX Evaluation Board

The CrossLink-NX Evaluation Board features the CrossLink-NX FPGA in the 400-ball caBGA package (LIFCL-40-9BG400C) w the ability to expand the usability of the CrossLink-NX with Raspberry Pi, PMOD, FMC LPC connector, along with access to PCIe channel. 118 wide range I/O and 37 high speed differential pairs are available for user-defined applications.

Figure 1.1 shows the top view of the CrossLink-NX Evaluation Board. Figure 1.2 shows the bottom view of the board. Figure 2.1 shows the jumper locations.

1.2. Features

The CrossLink-NX Evaluation Board includes the following features:

- CrossLink-NX FPGA (LIFCL-40-9BG400C)
- General Purpose Input/Output (GPIO) breakout with Raspberry Pi, PMOD, and FMC connector
- MIPI CSI-2 Camera connector and D-PHY connector
- 118 wide range I/O and 37 high speed differential pair I/O with on board termination
- x1 Gen2 PCIe interface
- USB-B connection for device programming and Inter-Integrated Circuit (I^2C) utility
- On-board Boot Flash – 128 Mbit Serial Peripheral Interface (SPI) Flash, with Quad read feature
- Eight input DIP switches, four push buttons, three status LEDs and 14 LEDs for demo purposes
- Lattice Radiant® Software programming support
- Multiple reference clock sources
- Potentiometer for ADC test

Caution: The CrossLink-NX Evaluation Board contains ESD-sensitive components. ESD safe practices should be followed while handling and using the development board.

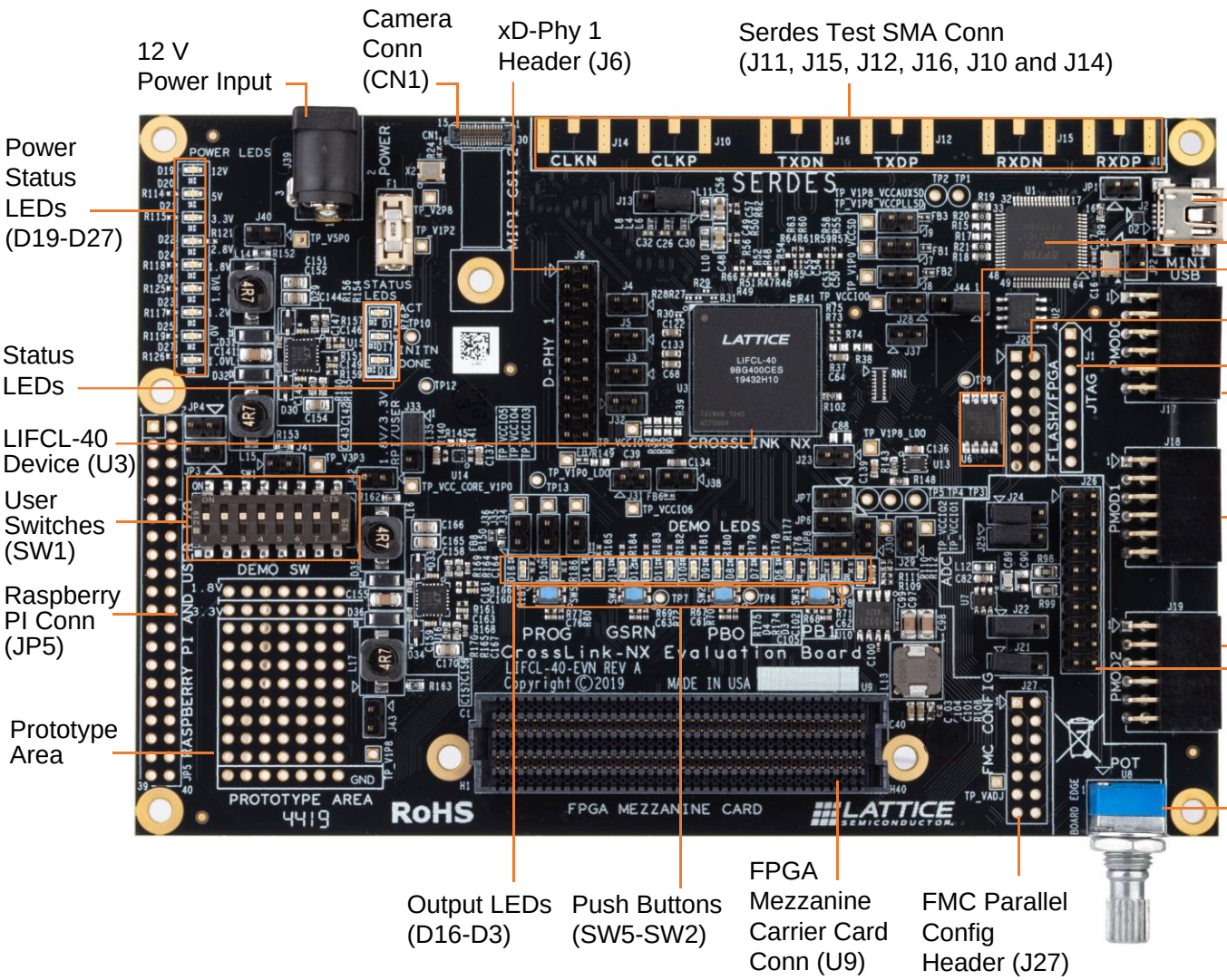

Figure 1.1. Top View of CrossLink-NX Evaluation Board

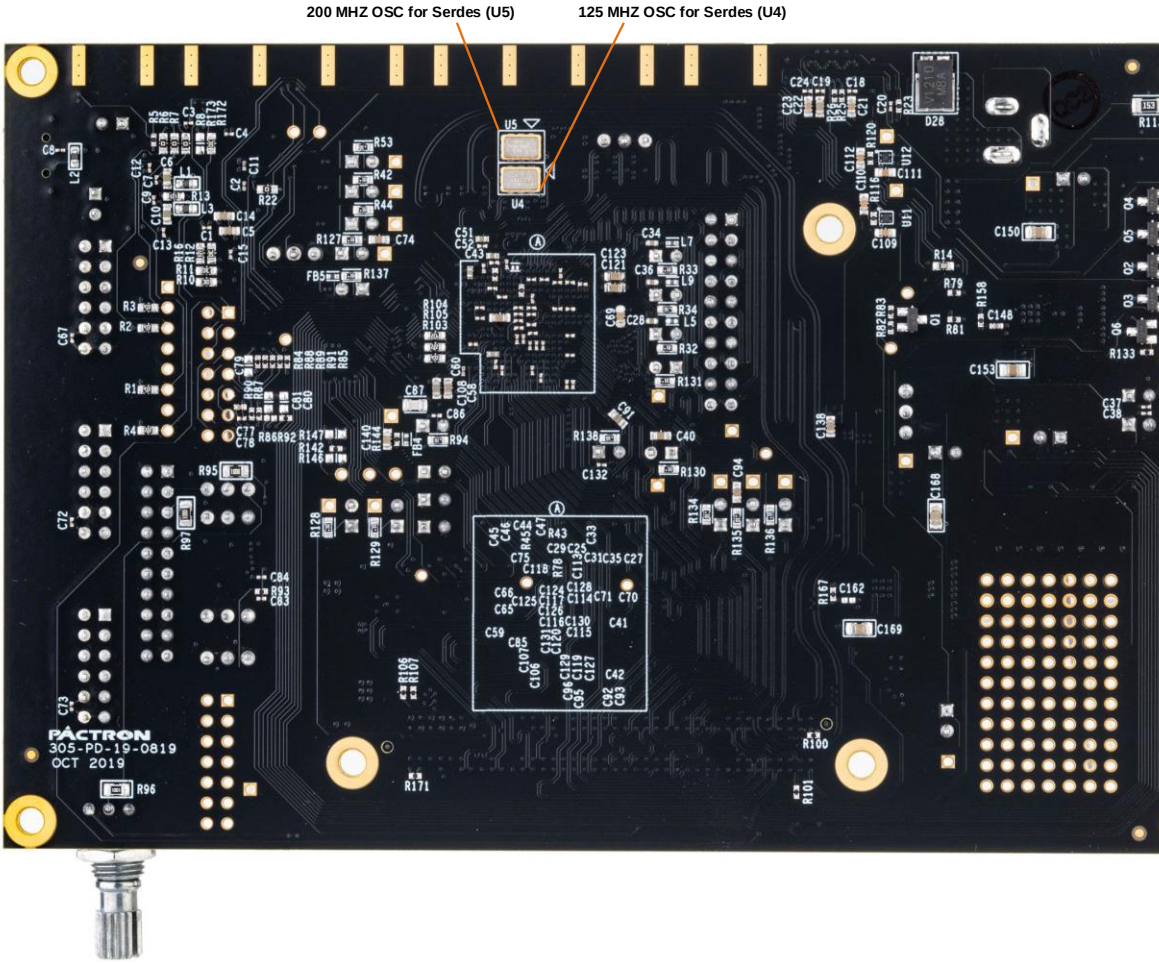

Figure 1.2. Bottom View of CrossLink-NX Evaluation Board

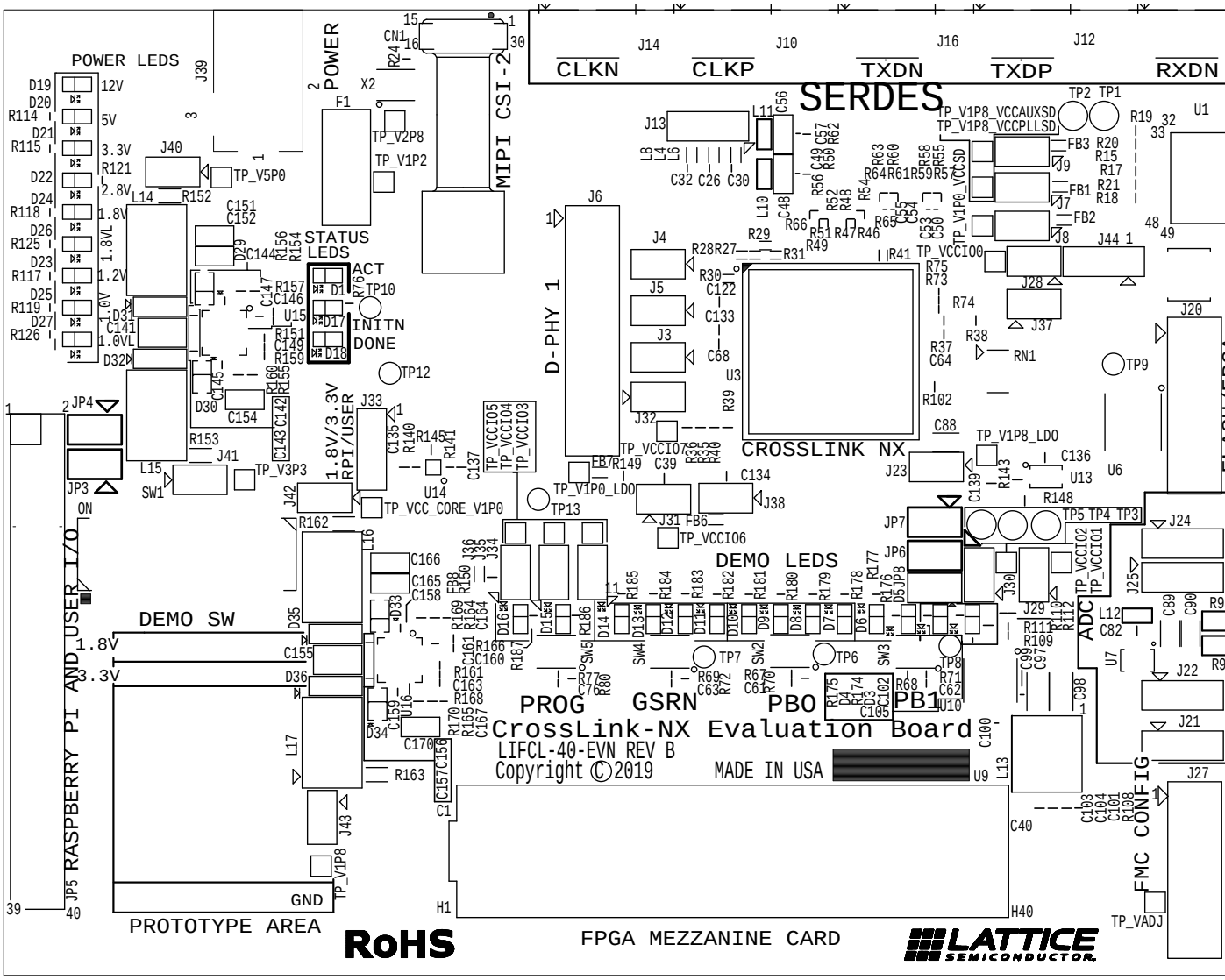

Figure 1.3. Silkscreen of CrossLink-NX Evaluation Board

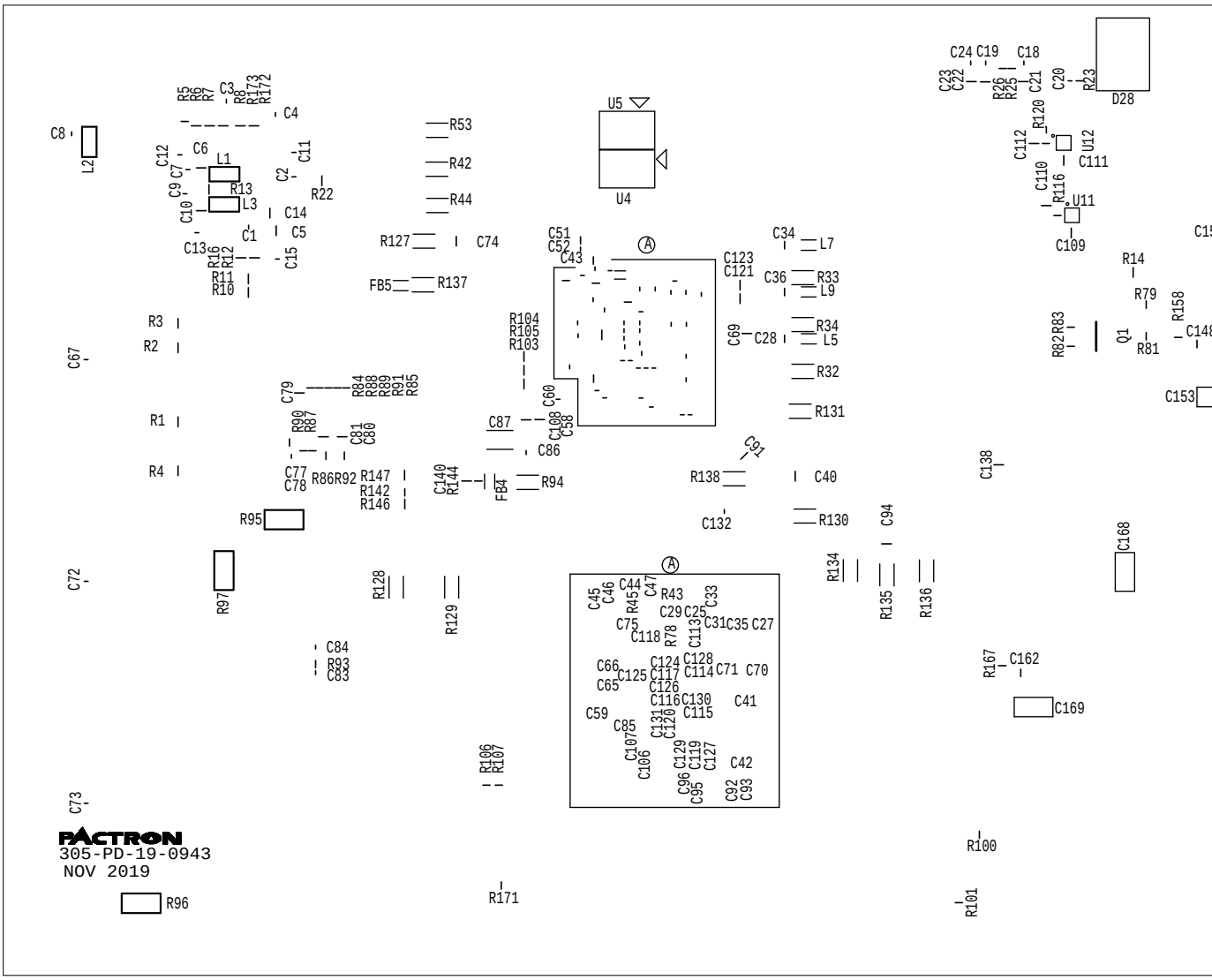

Figure 1.4. Silkscreen of CrossLink-NX Evaluation Board (Bottom)

1.3. CrossLink-NX Device

The CrossLink-NX Evaluation Board features the CrossLink-NX device in a 400-ball caBGA package, also referred to as LIFCL-40-9BG400C. For more information on the capabilities of CrossLink-NX, see CrossLink-NX Family Data Sheet (FPGA-DS-02049).

1.4. Applying Power to the Board

Power LEDs light after applying 12 V power to CrossLink-NX Evaluation Board to indicate the board is functioning. An Early I/O demo design is programmed into on-board boot flash as the default pattern. With this pattern, LED0 (D3) (mapped an early I/O) immediately turns on as soon as 12 V power is supplied to the board. After about two seconds, as configuration is successfully completed, DONE LED (D18) lights, and LED2 (D5) and LED3 (D6) light alternately in a heartbeat pattern.

2. Jumpers and Test Connection

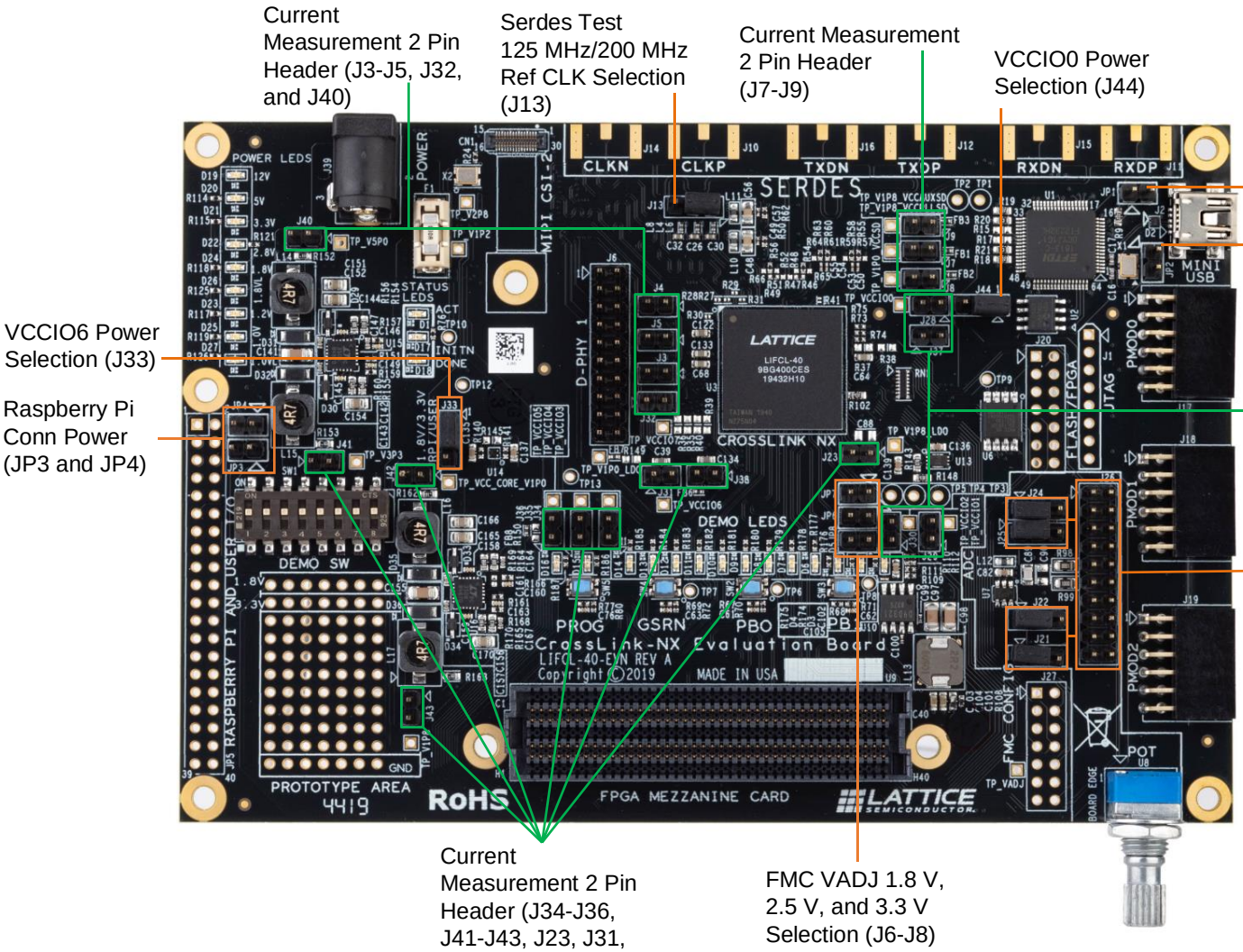

Figure 2.1. Top View of CrossLink-NX Evaluation Board – Jumper Locations

Table 2.1. Jumper Table

Part	Description	Setting
JP1	FTDI Reset Jumper	Default Open (active FTDI)/Short (reset FTDI)
JP2	FTDI Oscillator Jumper	Default Short (12 MHz OSC connected)/Open (12 MHz OSC unconnected)
JP3	Raspberry Pi Connector Power	Default Open (Raspberry Pi self-power)/Short (3.3v applies Paspberry Pi connector)
JP4	Raspberry Pi Connector Power	Default Open (Raspberry Pi self-power)/Short (5.0v applies Paspberry Pi connector)
JP6, JP7, and JP8	VADJ Selection Jumper For FMC LPC Carrier Connector	NO Jumper -> 1.5 V (JP6, JP7, and JP8 open)
		Only JP8* Short -> 1.8 V
		Only JP7* Short -> 2.5 V
		Only JP6* Short -> 3.3 V
J13	125 MHz / 200 MHz OSC Selection Jumper	Default 1–2 (125 MHz)/2-3 (200 MHz)
J21	ADC_REFP0 Selection Jumper	Default 1–2 (V1P8_ADC_VREF)/2-3 (J26 connector Input Voltage)
J22	ADC_REFP1 Selection Jumper	Default 1–2 (V1P8_ADC_VREF)/2-3 (J26 connector Input Voltage)
J24	ADC_DN0 Selection Jumper	Default 1-2 (Disable), 2-3 (J26 connector) To select POT, wire jumper: J24-1 to J25-2 and J24-2 to J25-1.
J25	ADC_DP0 Selection Jumper	
J44	VCCIO0 Supply Voltage Selection Jumper	Default 1–2 (3.3 V)/2-3 (1.8 V)
J33	VCCIO6 Supply Voltage Selection Jumper	Default 1–2 (3.3 V)/2-3 (1.8 V)
J3,J4,J5,J7,J8,J9, J23,J28,J29,J30, J31,J32,J34,J35, J36,J37,J38,J40, J41,J42, and J43	Current Measurement 2 Pin Header	—

***Note**: Only one jumper at a time. Otherwise, damage could occur.

3. Power Scheme

The CrossLink-NX Evaluation Board has most of its power supplied by onboard regulators powered by an external 12 V power. Refer to Appendix A. CrossLink-NX Evaluation Board Schematics to see the details of these power supply options. Figure 3.1 shows the high-level power supply architecture of the board. Table shows the voltage options available for the various VCCIO supplies.

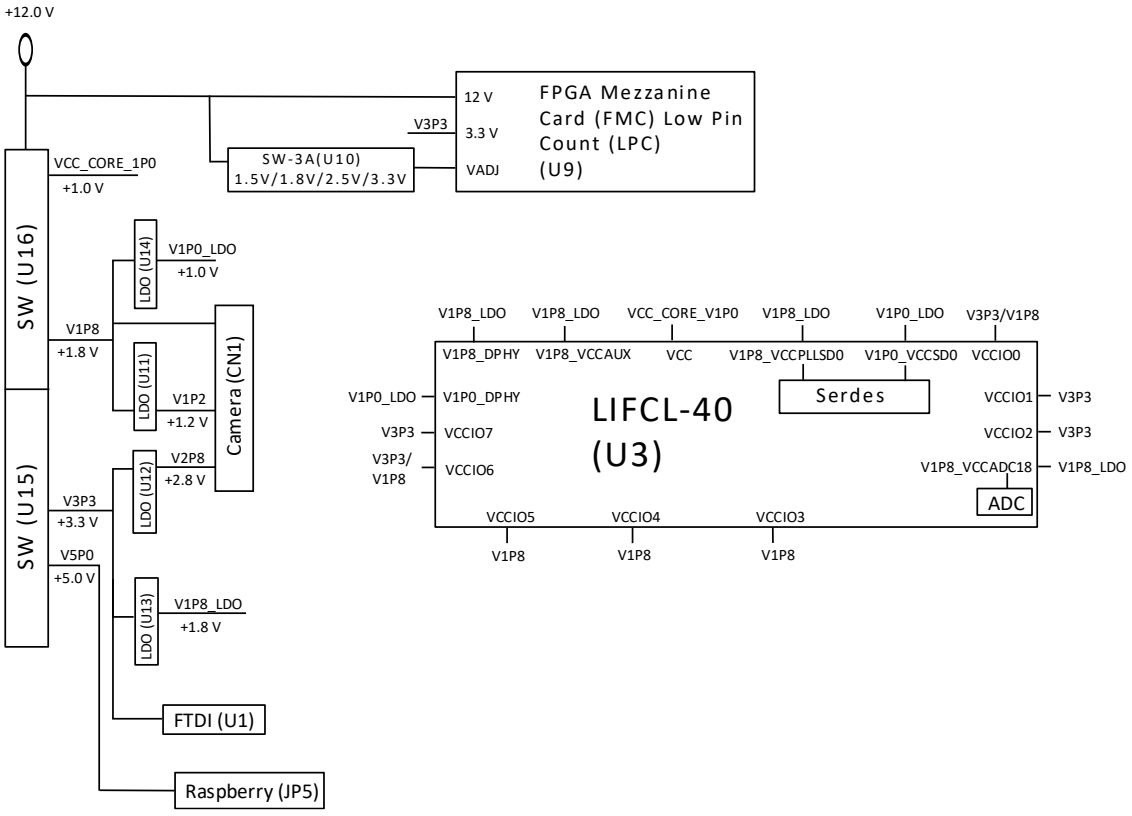

Figure 3.1. Board Power Scheme

Table 3.1. CrossLink-NX VCCIO Supply Options

VCCIO Bank	Selection	V3P3	V1P8
VCCIO0	J44 Connector	Default	Selectable
VCCIO1	—	Fixed	N/A
VCCIO2	—	Fixed	N/A
VCCIO3	—	N/A	Fixed
VCCIO4	—	N/A	Fixed
VCCIO5	—	N/A	Fixed
VCCIO6	J42 Connector	Default	Selectable
VCCIO7	—	Fixed	N/A

4. Programming and I²C

The JTAG/SPI programming architecture and I²C interface of the CrossLink-NX Evaluation Board is shown in Figure 4.1.

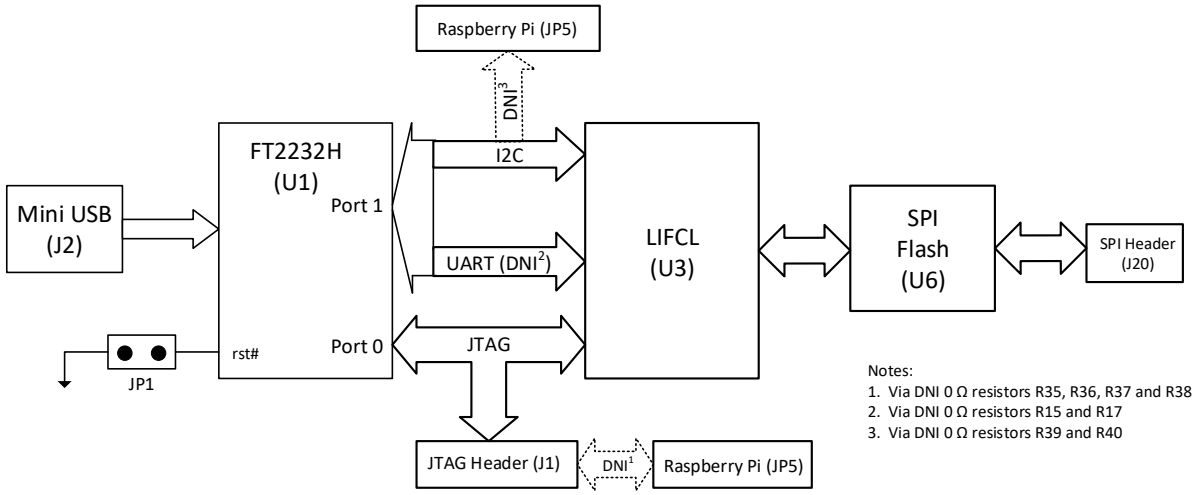

Figure 4.1. Configuration and I²C Architecture

4.1. JTAG Download Interface

The CrossLink-NX Evaluation Board has a built-in download controller for programming the CrossLink-NX device. It uses an FT2232H Future Technology Devices International (FTDI) part to convert USB to JTAG. To use the built-in download cable, connect the USB cable from a PC with Radiant Programmer tool installed to the mini USB connector on the board (J2). A mini USB to USB-A cable is included in the CrossLink-NX Evaluation Kit. The USB hub on the PC detects the cable of the USB function on Port 0, making the built-in cable available for use with the Radiant programming software.

4.2. Alternate JTAG Download Interface

J1 is an 8-pin standalone JTAG header used with an external Lattice download cable that is available separately, when the FTDI part is disabled from the JTAG chain after setting the JP1 jumper. A USB download cable can be attached to the board using J1 to interface with the CrossLink-NX. For details on the connection between the USB download cable and J1, refer to Programming Cable User's Guide (FPGA-UG-02042).

J1 can also be used as test point when USB to JTAG is working. Additionally, you can enable the JTAG access path through the Raspberry Pi header (JP5) for customer applications. This is done by connecting the JP5 header to the J1 header through some onboard resistors. The JTAG connections between J1 and JP5 are listed in Table .

Table 4.1. JTAG Connections

J1 Pin Number	JTAG Signal Name	CrossLink-NX Ball Location for JTAG	Raspberry Pi Header (JP8) Pin Number	J1 to JP5 Isolation (Assembly)	Raspberry Pi GPIO
1	VCCIO1	—	—	—	—
2	TDO	F19	10	R36 (DNI)	IO15
3	TDI	F17	11	R38 (DNI)	IO17
4	—	—	—	—	—
5	—	—	—	—	—
6	TMS	F15	12	R37 (DNI)	IO18
7	GND	—	—	—	—
8	TCK	G18	8	R35 (DNI)	IO14

4.3. JTAG to MSPI Pass-through Interface

The download controller can also access the JTAG to MSPI pass-through circuit that allows the slave SPI Flash to be erased, programmed, and read with Radiant Programmer.

4.4. SPI Flash Device Selection in Programmer

The Flash device on this board is a Macronix MX25L12833F.

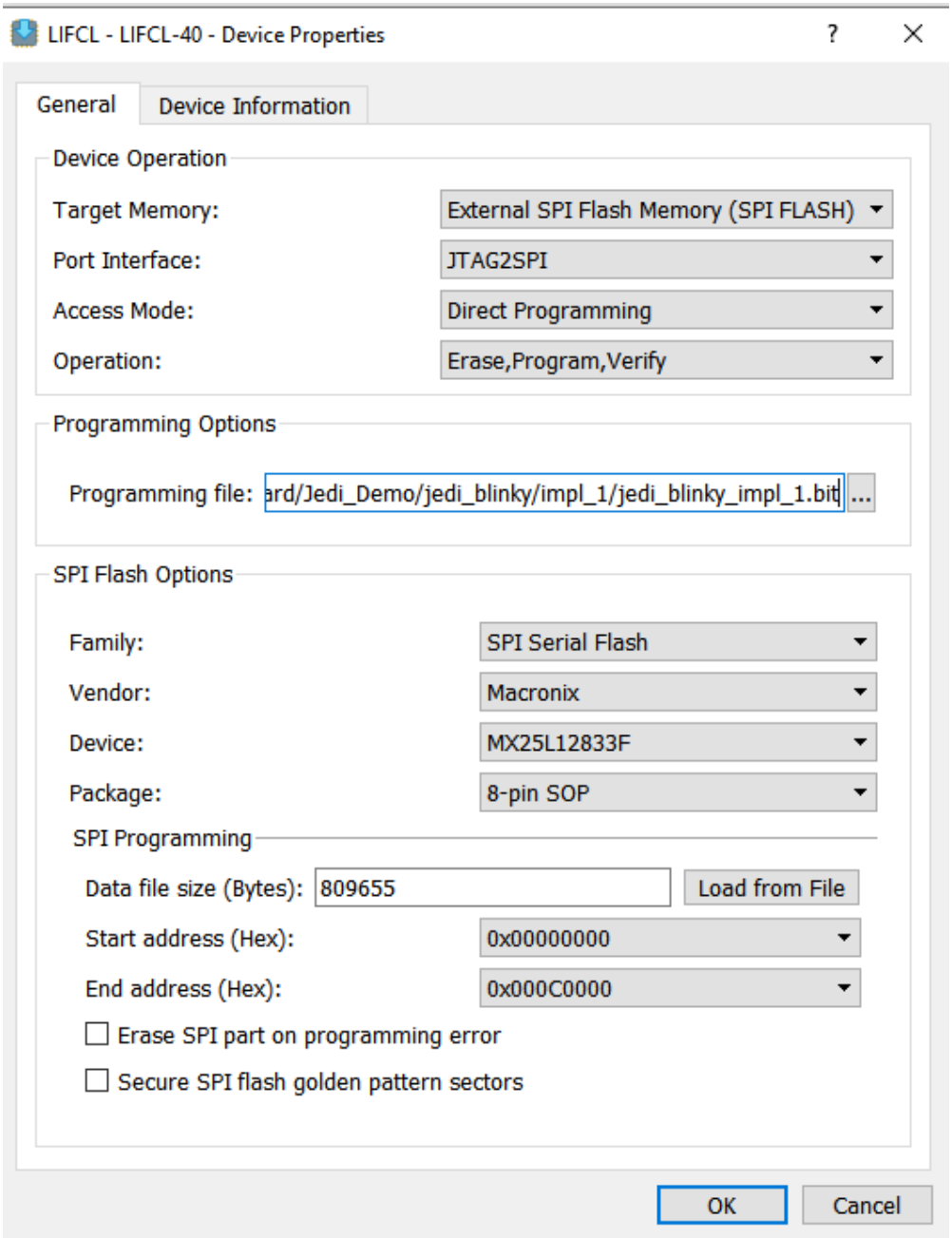

Figure 4.2. SPI Flash Operation Dialog

You may proceed with the Flash device programming by following the procedure in CrossLink-NX sysCONFIG Usage Guide (FPGA-TN-02099).

4.5. Other JTAG Configuration Pins

The CrossLink-NX Evaluation Board provides test points for other JTAG configuration pins as shown in Table .

Table 4.2. Other JTAG Signals

Signal Name	CrossLink-NX Ball Location	Test Point	Push Button
PROGRAMN	E11	—	SW5
INITN	D11	TP10	—
DONE	D12	TP12	—

For more information on CrossLink-NX JTAG and SPI programming, refer to CrossLink-NX sysCONFIG Usage Guide (FPGA-TN-02099).

5. CrossLink-NX Clock Sources

The CrossLink-NX Evaluation Board has three options for the CrossLink-NX clock sources:

Table 5.1. Clock Sources

Clock Frequency	Signal Name	CrossLink-NX Ball Location	Clock Source	Comments
12 MHz	12 MHz	L13	U1	JP2 installed. JP1 removed.
200 MHz	200 MHz/200 MHz_n	C12/ C11	U5	Insert R65 & R66, remove R54 & R56
125 MHz	125 MHz/125 MHz_n	C12/ C11	U4	Insert R54 & R56, remove R65 & R66

6. Control Buses – I²C, UART, and SPI

This section describes the topology of the various configuration and communication buses.

6.1. I²C

The CrossLink-NX Evaluation Board uses the I²C bus to support CrossLink-NX configuration, and optionally to support Raspberry Pi communication. The global I²C bus has the signal names SDA and SCL and they are routed close to Raspberry Pi header as shown in Figure 4.1 and in more detail in Figure 6.1.

Raspberry Pi connector is connected to a dedicated CrossLink-NX GPIO bank with a direct local I²C bus. Local I²C bus can optionally connect to the global I²C bus through resistors. The local I²C connections are summarized in Table .

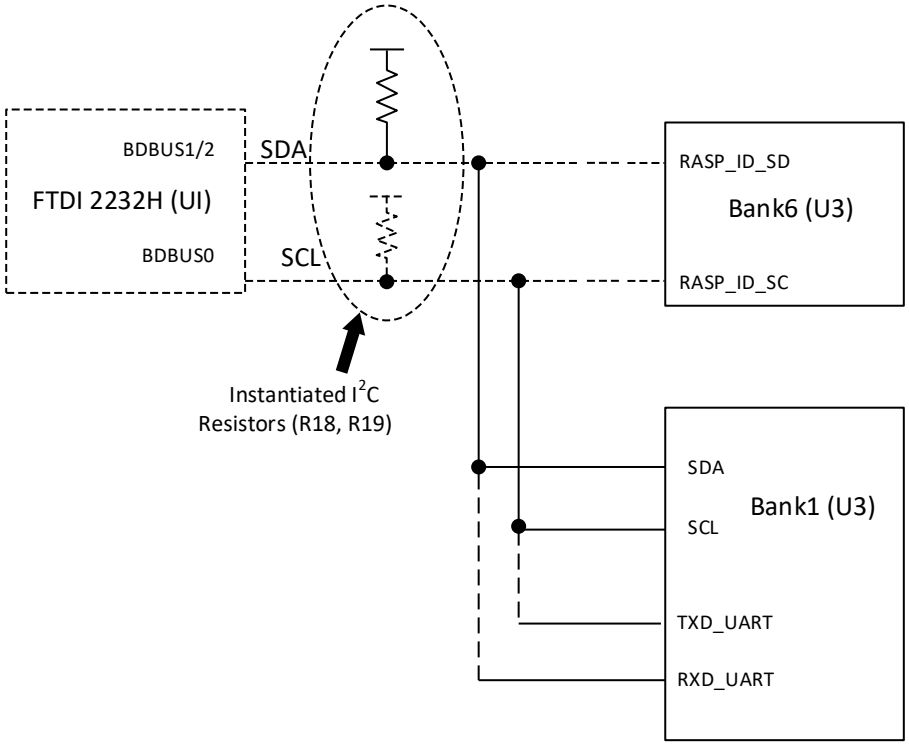

Figure 6.1. I²C Architecture and UART Options

Table 6.1. I²C Global Bus Connections

CrossLink-NX Bank	Component (Reference)	Header Pin	CrossLink-NX - 85 Ball	Local Signal Name (Global I²C Signal)	Resistor
6	Raspberry Pi header (JP5)	27	M7	RASP_ID_SD (SDA)	R40 (DNI)
		28	M4	RASP_ID_SC (SCL)	R39 (DNI)

6.2. UART Topology

The board provides support for UART configuration by providing an uninstalled connection between the FTDI and CrossLink-NX. Two 0 Ω resistors (R16 and R17) can be installed to connect Port 1 to two general purpose I/O (PR8A/F16 and PR10A/F18) in Bank 6 as shown in Figure 6.1.

6.3. SPI Topology

6.3.1. SPI Configuration

One of the major functions of SPI connections on the board is to support CrossLink-NX configuration from the SPI Flash or the Parallel Configuration Header. The CrossLink-NX Evaluation Board can support both Master SPI (MSPI) and Slave SPI (SSPI) modes for CrossLink-NX configuration.

Table 6.2. CrossLink-NX SPI Connections

Signal Name	CrossLink-NX Ball	Parallel Configuration Header Pin
SPI_MCLK	E12	12
DQ0_MOSI	D13	5
DQ1_MISO	D15	7
CSSPIN	E13	8
DQ2	D14	11
DQ3	D16	9
MCSNO	E16	3

7. LEDs and Switches

This section describes the CrossLink-NX Evaluation Board LEDs and switches that can be used in demo and customer designs.

7.1. DIP Switch

Eight CrossLink-NX pins are connected to the SW1 DIP switch to allow for manually actuated inputs to the FPGA. One side of each switch is connected to GPIOs within the VCCIO2 bank and pulled up through 4.7 kΩ resistors. The other side is grounded. The designated pins are connected as shown in Table .

Table 7.1. Eight-Position DIP Switch Signals

Signal Name	CrossLink-NX Ball	CrossLink-NX Bank
SWITCH0	N14	2
SWITCH1	M14	2
SWITCH2	M16	2
SWITCH3	M15	2
SWITCH4	N15	2
SWITCH5	N16	2
SWITCH6	M17	2
SWITCH7	M18	2

7.2. General Purpose Push Buttons

The CrossLink-NX Evaluation Board provides three push button switches – SW2, SW3 and SW4 for demos and user applications. Two of the buttons control pre-defined functional pins, and the third is generic. Pressing these buttons drives a logic level “0” to the corresponding I/O pins.

Table 7.2. Push Button Switch Signals

Signal Name	CrossLink-NX Ball	Push Button Reference	Logic Level at Button Pressed
GSRN	G19	SW4	0
PROGRAMN	E11	SW5	0
PUSHBUTTON0	G14	SW2	0
PUSHBUTTON1	G15	SW3	0

Information on PROGRAMN, refer to CrossLink-NX sysCONFIG Usage Guide (FPGA-TN-02099). SW2 is intended to be used as a global set/reset pin when active low, but can be substituted for another function if the user desires. SW2 and SW3 can be used as a generic input.

7.3. General Purpose LEDs

The CrossLink-NX Evaluation Board provides fourteen LEDs that are connected to I/O within Bank 1 & 0. The LEDs are lighted when the output is driven LOW.

Table 7.3. General Purpose LED Signals

Signal Name	CrossLink-NX Ball	CrossLink-NX Bank / Color
LED0	E17	1 (Green)
LED1	F13	1 (Green)
LED2	G13	1 (Green)
LED3	F14	1 (Green)
LED4	L16	1 (Green)
LED5	L15	1 (Green)
LED6	L20	1 (Green)
LED7	L19	1 (Green)
LED8	R17	2 (Green)
LED9	R18	2 (Green)
LED10	U20	2 (Green)
LED11	T20	2 (Green)
LED12	W20	2 (Yellow)
LED13	V20	2 (Yellow)

7.4. Indicator LEDs

Table lists various LEDs and describes their purpose.

Table 7.4. Various LED Signals

LEDs	Signal Name	CrossLink-NX Ball	Color	Purpose
D1	UART_ACT	F18	Green	If installed, lights in UART mode
D17	INITN	D11	Red	Lights if configuration error
D18	DONE	D12	Green	Lights if successful configuration
D19	+12.0 V	—	Green	Lights if voltage present (external connection)
D20	+5.0 V	—	Green	Lights if voltage present
D21	+3.3 V	—	Green	Lights if voltage present
D22	+2.8 V	—	Green	Lights if voltage present
D23	+1.2 V	—	Green	Lights if voltage present
D24	+1.8 V	—	Green	Lights if voltage present
D25	+1.0 V (VCC_CORE_V1P0)	—	Green	Lights if voltage present
D26	+1.8 V (V1P8_LDO)	—	Green	Lights if voltage present
D27	+1.0 V (V1P0_LDO)	—	Green	Lights if voltage present

8. Headers/Connectors and LIFCL-40 Device Ball Mapping

This section describes the CrossLink-NX Evaluation Board headers/connectors and ball mapping.

8.1. FMC LPC Connector

Table 8.1. FMC LPC Header Pin Connections

U9 Pin Name	Signal Name	LIFCL-40 Ball	U9 Pin Name	Signal Name	LIFCL-40 Ball
C1	GND	—	D1	PS_POR_B	—
C2	TXDP_FMC	—	D2	GND	—
C3	TXDN_FMC	—	D3	GND	—
C4	GND	—	D4	REFCLKP_FMC	—
C5	GND	—	D5	REFCLKN_FMC	—
C6	RXDP_FMC	—	D6	GND	—
C7	RXDN_FMC	—	D7	GND	—
C8	GND	—	D8	FMC_LA01_CC_P	W13
C9	GND	—	D9	FMC_LA01_CC_N	V12
C10	FMC_LA06_P	W9	D10	GND	—
C11	FMC_LA06_N	Y9	D11	FMC_LA05_P	R5
C12	GND	—	D12	FMC_LA05_N	R6
C13	GND	—	D13	GND	—
C14	FMC_LA10_P	W10	D14	FMC_LA09_P	V6
C15	FMC_LA10_N	Y10	D15	FMC_LA09_N	U7
C16	GND	—	D16	GND	—
C17	GND	—	D17	FMC_LA13_P	R9
C18	FMC_LA14_P	W11	D18	FMC_LA13_N	P9
C19	FMC_LA14_N	Y11	D19	GND	—
C20	GND	—	D20	FMC_LA17_P	U10
C21	GND	—	D21	FMC_LA17_N	V10
C22	FMC_LA18_CC_P	R8	D22	GND	—
C23	FMC_LA18_CC_N	T8	D23	FMC_LA23_P	P11
C24	GND	—	D24	FMC_LA23_N	R11
C25	GND	—	D25	GND	—
C26	FMC_LA27_P	Y13	D26	FMC_LA26_P	T13
C27	FMC_LA27_N	Y14	D27	FMC_LA26_N	T14
C28	GND	—	D28	GND	—
C29	GND	—	D29	FMC_TCK	—
C30	FMC_SCL	—	D30	FMC_TDI	—
C31	FMC_SDA	—	D31	FMC_TDO	—
C32	GND	—	D32	V3P3	—
C33	GND	—	D33	FMC_TMS	—
C34	GND	—	D34	NO Connect	—
C35	12V	—	D35	GND	—
C36	GND	—	D36	V3P3	—
C37	12V	—	D37	GND	—
C38	GND	—	D38	V3P3	—
C39	V3P3	—	D39	GND	—
C40	GND	—	D40	V3P3	—
G1	GND	—	H1	FMC_VREF	T6 Y18

U9 Pin Name	Signal Name	LIFCL-40 Ball	U9 Pin Name	Signal Name	LIFCL-40 Ball
G2	FMC_CLK1_P	R7	H2	FMC_PRSNT	—
G3	FMC_CLK1_N	T7	H3	GND	—
G4	GND	—	H4	FMC_CLK0_P	Y12
G5	GND	—	H5	FMC_CLK0_N	W12
G6	FMC_LA00_CC_P	V11	H6	GND	—
G7	FMC_LA00_CC_N	U11	H7	FMC_LA02_P	Y2
G8	GND	—	H8	FMC_LA02_N	Y3
G9	FMC_LA03_P	W6	H9	GND	—
G10	FMC_LA03_N	Y6	H10	FMC_LA04_P	V1
G11	GND	—	H11	FMC_LA04_N	W1
G12	FMC_LA08_P	Y7	H12	GND	—
G13	FMC_LA08_N	Y8	H13	FMC_LA07_P	W7
G14	GND	—	H14	FMC_LA07_N	V7
G15	FMC_LA12_P	U1	H15	GND	—
G16	FMC_LA12_N	T1	H16	FMC_LA11_P	P10
G17	GND	—	H17	FMC_LA11_N	R10
G18	FMC_LA16_P	P7	H18	GND	—
G19	FMC_LA16_N	P8	H19	FMC_LA15_P	W8
G20	GND	—	H20	FMC_LA15_N	V9
G21	FMC_LA20_P	T10	H21	GND	—
G22	FMC_LA20_N	T11	H22	FMC_LA19_P	U12
G23	GND	—	H23	FMC_LA19_N	T12
G24	FMC_LA22_P	V14	H24	GND	—
G25	FMC_LA22_N	U14	H25	FMC_LA21_P	P13
G26	GND	—	H26	FMC_LA21_N	R13
G27	FMC_LA25_P	R12	H27	GND	—
G28	FMC_LA25_N	P12	H28	FMC_LA24_P	W14
G29	GND	—	H29	FMC_LA24_N	W15
G30	FMC_LA29_P	Y15	H30	GND	—
G31	FMC_LA29_N	Y16	H31	FMC_LA28_P	U15
G32	GND	—	H32	FMC_LA28_N	V16
G33	FMC_LA31_P	Y17	H33	GND	—
G34	FMC_LA31_N	W17	H34	FMC_LA30_P	V17
G35	GND	—	H35	FMC_LA30_N	U16
G36	ADC_IN1P	—	H36	GND	—
G37	ADC_IN1N	—	H37	VREF2_CON	—
G38	GND	—	H38	NO Connect	—
G39	VADJ	—	H39	GND	—
G40	GND	—	H40	VADJ	—

8.2. Parallel FMC Configuration Header

Table 8.2. Parallel FMC Configuration J27 Pin Connections

J27 Pin Name	Signal Name	LIFCL-40 Ball
1	VCCIO2	—
2	VCCIO2	—
3	FMC_TCK	P19
4	PS_POR_B	N19
5	GND	—
6	GND	—
7	FMC_TDI	P20
8	FMC_PRSNT	N20
9	FMC_TDO	P17
10	FMC_SCL	M20
11	GND	—
12	GND	—
13	FMC_TMS	P18
14	FMC_SDA	M19

8.3. Raspberry Pi Board GPIO Header

The CrossLink-NX Evaluation Board provides a 40-pin receptacle which is compatible with the GPIO header of Raspberry Pi 2/3 serial models, or can be used for general purpose I/O.

Table 8.3. Raspberry Pi JP8 Header Pin Connections

JP5 Pin Name	Signal Name	LIFCL-40 Ball
1	VSP3*	—
2	RASP_5V*	—
3	RASP_IO02	L6
4	RASP_5V*	—
5	RASP_IO03	L5
6	GND	—
7	RASP_IO04	M3
8	RASP_IO14	M2
9	GND	—
10	RASP_IO15	L1
11	RASP_IO17	L2
12	RASP_IO18	R2
13	RASP_IO27	R1
14	GND	—
15	RASP_IO22	P2
16	RASP_IO23	P1
17	VSP3*	—
18	RASP_IO24	K7
19	RASP_IO10	N4
20	GND	—
21	RASP_IO09	K6
22	RASP_IO25	K5
23	RASP_IO11	N7

JP5 Pin Name	Signal Name	LIFCL-40 Ball
24	RASP_IO08	P6
25	GND	—
26	RASP_IO07	N5
27	RASP_ID_SD	M7
28	RASP_ID_SC	M4
29	RASP_IO05	K8
30	GND	—
31	RASP_IO06	L7
32	RASP_IO12	L8
33	RASP_IO13	M5
34	GND	—
35	RASP_IO19	M6
36	RASP_IO16	N6
37	RASP_IO26	P5
38	RASP_IO20	R3
39	GND	—
40	RASP_IO21	R4

***Note**: 3.3 V and 5 V provide the power to the Raspberry Pi board when JP3 and JP4 are installed. When JP3 and JP4 are not installed, Raspberry Pi needs its own 3.3 V and 5 V power.

When connecting directly to a Raspberry Pi board, depending on the individual setup, there may need to be an adapter to avoid mechanical interference between the two boards. A generic 40-pin (2×20), 100-mil spacing header extender serves this function. Alternately, the two boards can be connected by a length of ribbon cable with 2×20 connectors on either end.

8.4. Camera Connector

Table 8.4. Camera CN1 Connector Pin Connections

CN1 Pin Name	Signal Name	LIFCL-40 Ball
1	NO Connect	—
2	CAM0_CLKN	B1
3	CAM0_CLKP	A2
4	GND	—
5	CAM0_3N	B4
6	CAM0_3P	A4
7	GND	—
8	CAM0_1N	B3
9	CAM0_1P	A3
10	GND	—
11	CAM0_0N	C1
12	CAM0_0P	B2
13	GND	—
14	CAM0_2N	D1
15	CAM0_2P	C2
16	GND	—
17	GND	—
18	V2P8	—
19	NO Connect	—
20	CAM0_MCLK	—

CN1 Pin Name	Signal Name	LIFCL-40 Ball
21	NO Connect	—
22	CAM_SDA	W5
23	CAM_SCL	Y5
24	CAM_RESET	W18
25	V1P2	—
26	V1P8	—
27	GND	—
28	GND	—
29	V2P8	—
30	GND	—

8.5. D-PHY1 Header

Table 8.5. D-PHY1 J6 Header Pin Connections

J6 Pin Name	Signal Name	LIFCL-40 Ball
1	GND	—
2	GND	—
3	DPHY1_CKP	A8
4	DPHY1_CKN	B8
5	GND	—
6	GND	—
7	DPHY1_DP0	A7
8	DPHY1_DN0	B7
9	GND	—
10	GND	—
11	DPHY1_DP1	A9
12	DPHY1_DN1	B9
13	GND	—
14	GND	—
15	DPHY1_DP2	A6
16	DPHY1_DN2	B6
17	GND	—
18	GND	—
19	DPHY1_DP3	A10
20	DPHY1_DN3	B10

8.6. PMOD Header

The J17, J18 and J19 header can be used as GPIO or as a connector to a PMOD interface.

Table 8.6. J17, J18 and J19 Header Pin Connections

Pin Name	Signal Name	LIFCL-40 Ball
J17 Pin Name		
1	PMOD0_1	D10
2	PMOD0_2	D9
3	PMOD0_3	D7
4	PMOD0_4	D8
5	PMOD0_7	D6
6	PMOD0_8	D5
7	PMOD0_9	D4
8	PMOD0_10	D3
J18 Pin Name		
1	PMOD1_1	E10
2	PMOD1_2	E9
3	PMOD1_3	E7
4	PMOD1_4	E8
5	PMOD1_7	E4
6	PMOD1_8	E3
7	PMOD1_9	E2
8	PMOD1_10	F1
J19 Pin Name		
1	PMOD2_1	J2
2	PMOD2_2	J1
3	PMOD2_3	K2
4	PMOD2_4	K1
5	PMOD2_7	K3
6	PMOD2_8	K4
7	PMOD2_9	D17
8	PMOD2_10	E18

8.7. JTAG Header

The J1 header is used to access the JTAG port of the CrossLink-NX or the Raspberry Pi interface.

Table 8.7. J1 Header Pin Connections

J1 Pin Name	Signal Name	LIFCL-40 Ball
1	VCCIO1	—
2	TDO	F19
3	TDI	F17
4	No Connect	—
5	No Connect	—
6	TMS	F15
7	GND	—
8	TCK	E19

8.8. Parallel Configuration Header

The J27 header is used to access the SPI port of the CrossLink-NX.

Table 8.8. J27 Header Pin Connections

J27Pin Name	Signal Name	LIFCL-40 Ball
1	VCCIO2	—
2	VCCIO2	—
3	FMC_TCK	P19
4	PS_POR_B	N19
5	GND	—
6	GND	—
7	FMC_TDI	P20
8	FMC_PRSNT	N20
9	FMC_TDO	P17
10	FMC_SCL	M20
11	GND	—
12	GND	—
13	FMC_TMS	P18
14	FMC_SDA	M19

8.9. ADC Test Header

Table 8.9. J26 Header Pin Connections

J26 Pin Name	Signal Name	LIFCL-40 Ball
1	GND	—
2	GND	—
3	J24 PIN3	—
4	GND	—
5	J25 PIN3	—
6	GND	—
7	GND	—
8	GND	—
9	ADC_IN1P	T17
10	GND	—
11	ADC_IN1N	U17
12	GND	—
13	GND	—
14	GND	—
15	VREF2_CON	—
16	GND	—
17	GND	—
18	GND	—
19	VREF1_CON	—
20	GND	—

9. Software Requirements

The following software versions are required to develop designs for the CrossLink-NX Evaluation Board:

- Lattice Radiant Software 2.0 or later
- Lattice Radiant Programmer 2.0 or later

10. Storage and Handling

Static electricity can shorten the life span of electronic components. Observe these tips to prevent damage that can occur from electrostatic discharge:

- Use antistatic precautions such as operating on an antistatic mat and wearing an antistatic wristband.
- Store the development board in the provided packaging.
- Touch a metal USB housing to equalize voltage potential between you and the board.

11. Ordering Information

Table 11.1. Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
CrossLink-NX Evaluation Board	LIFCL-40-EVN	

Appendix A. CrossLink-NX Evaluation Board Schematics

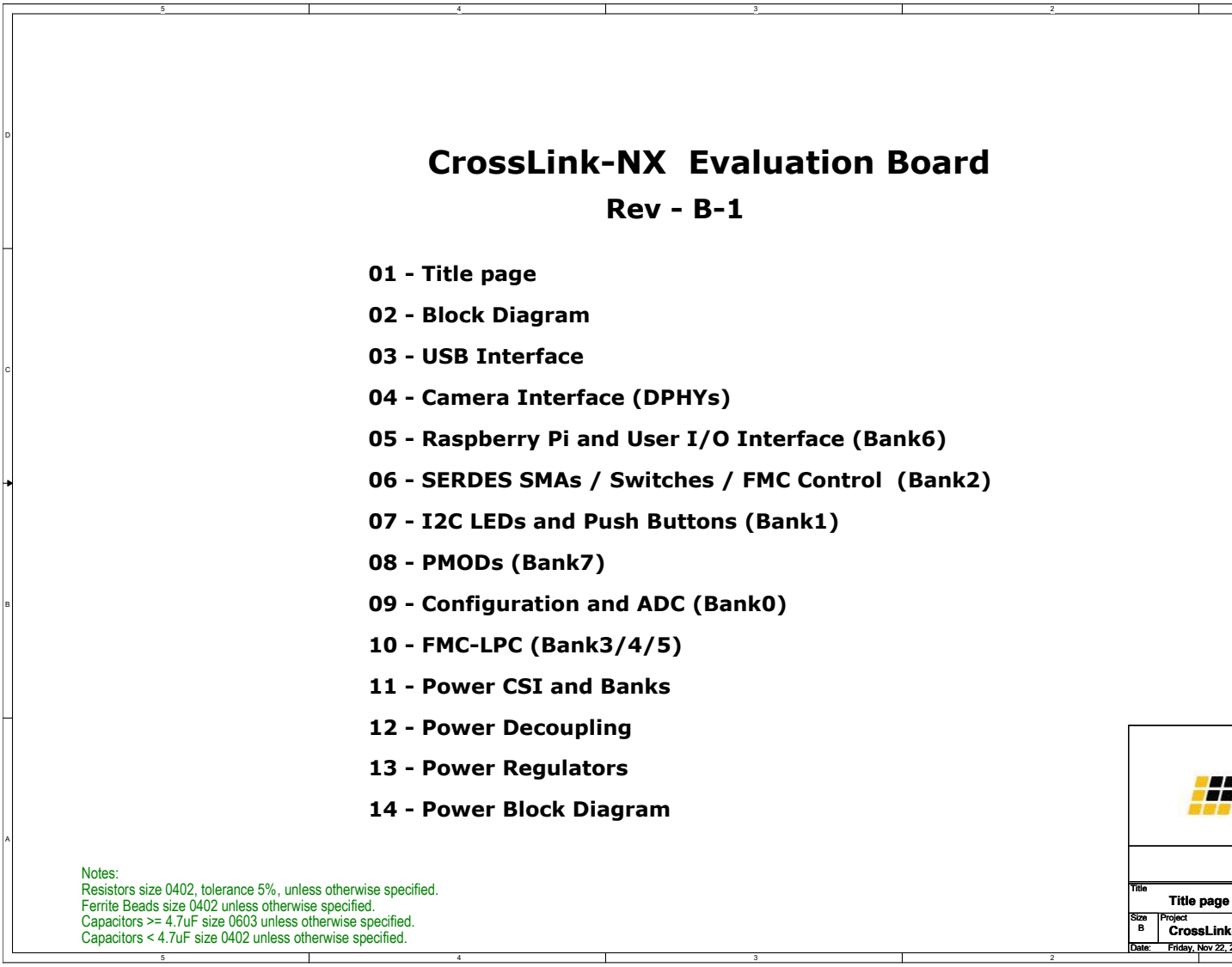

Figure A.1. Title Page

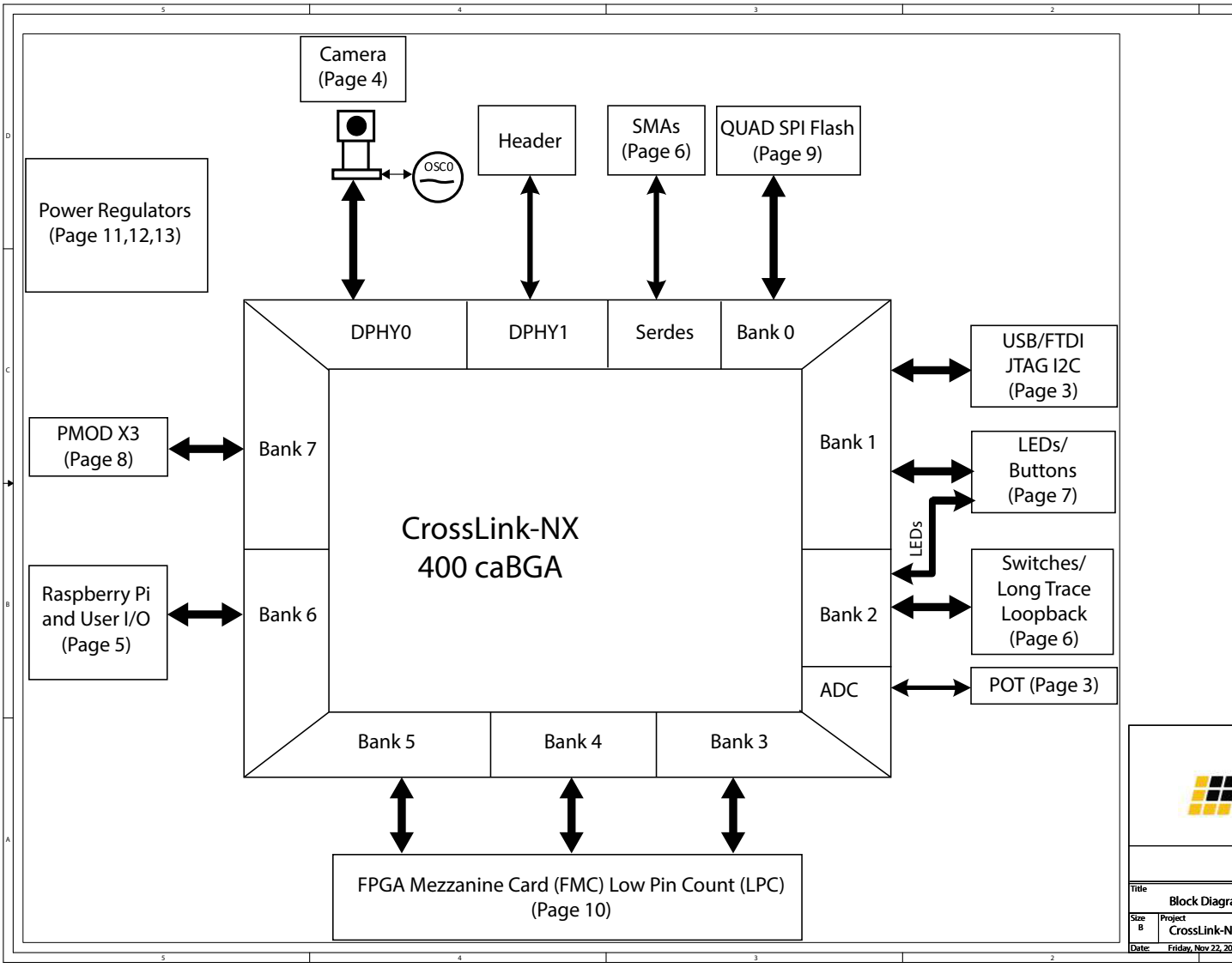

Figure A.2. Block Diagram

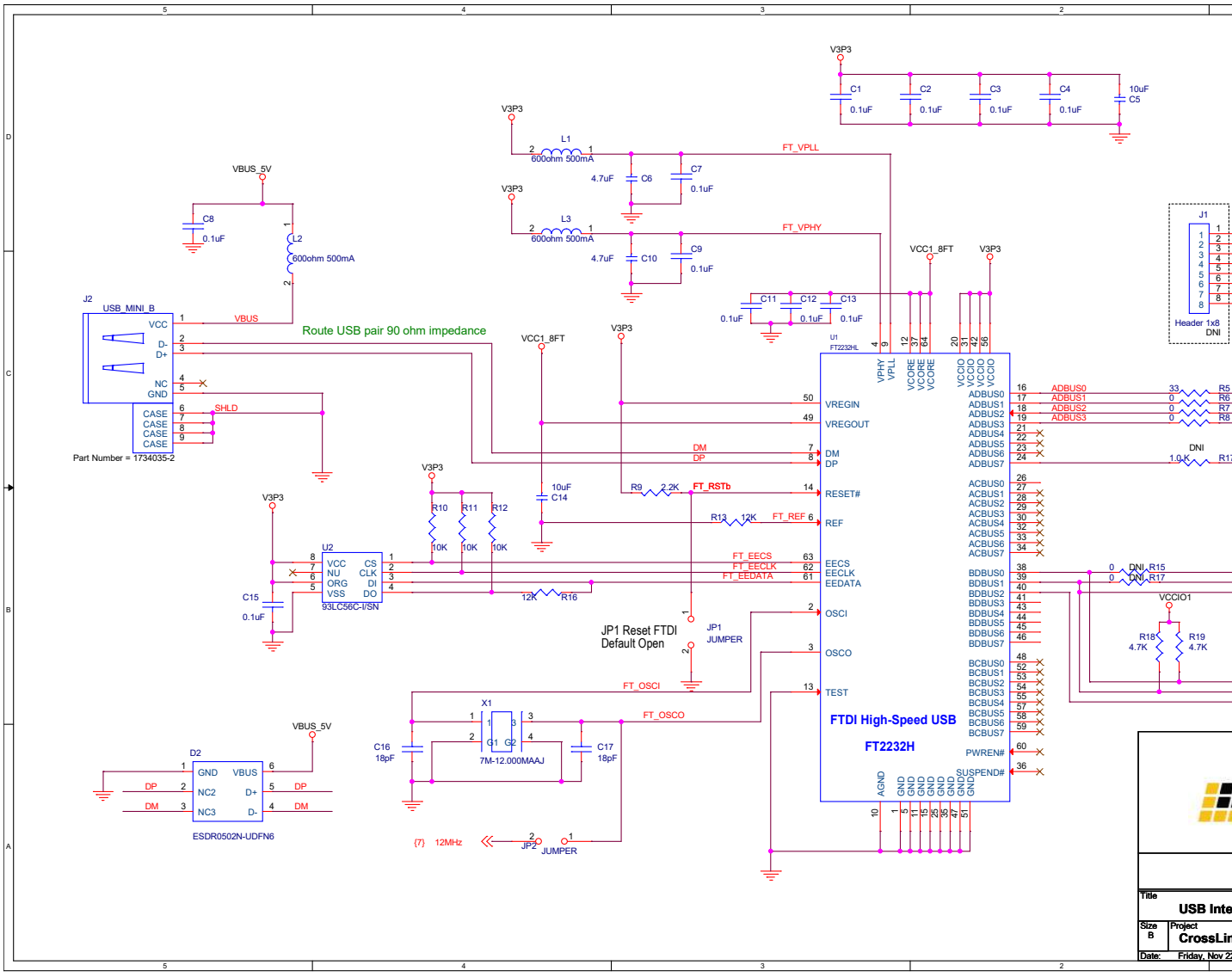

Figure A.3. USB Interface

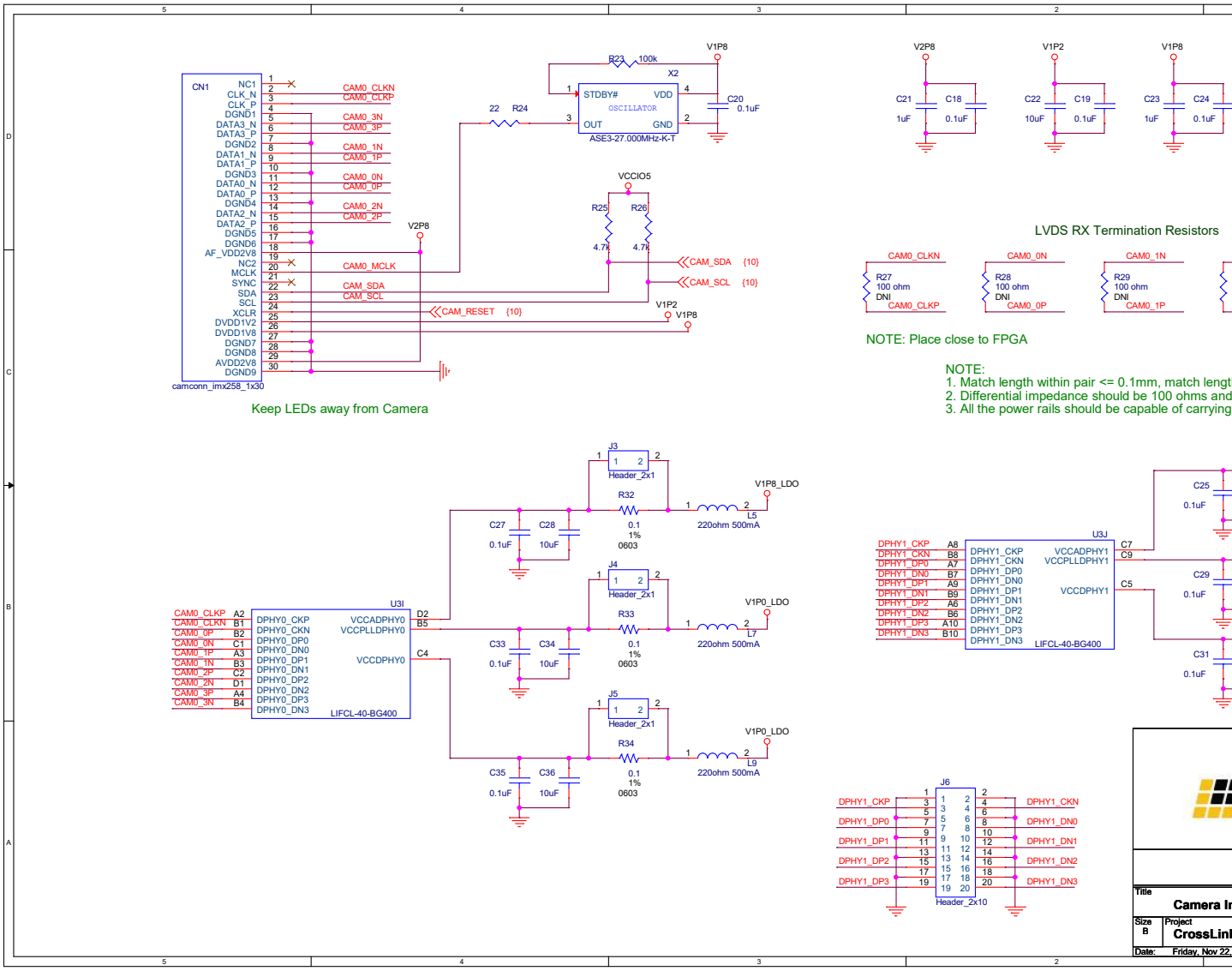

Figure A.4. Camera Interface (DPHYs)

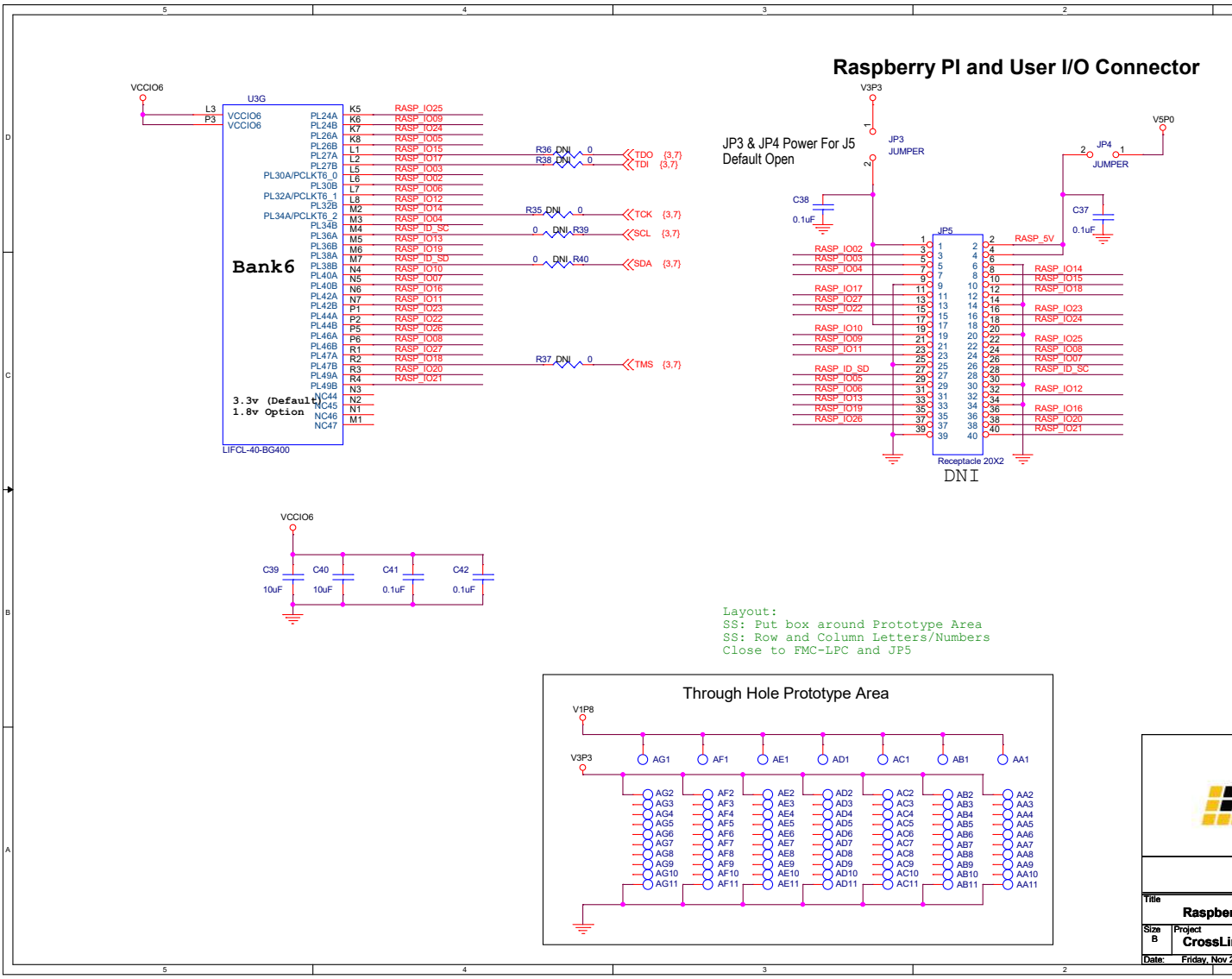

Figure A.5. Raspberry Pi and User I/O Interface

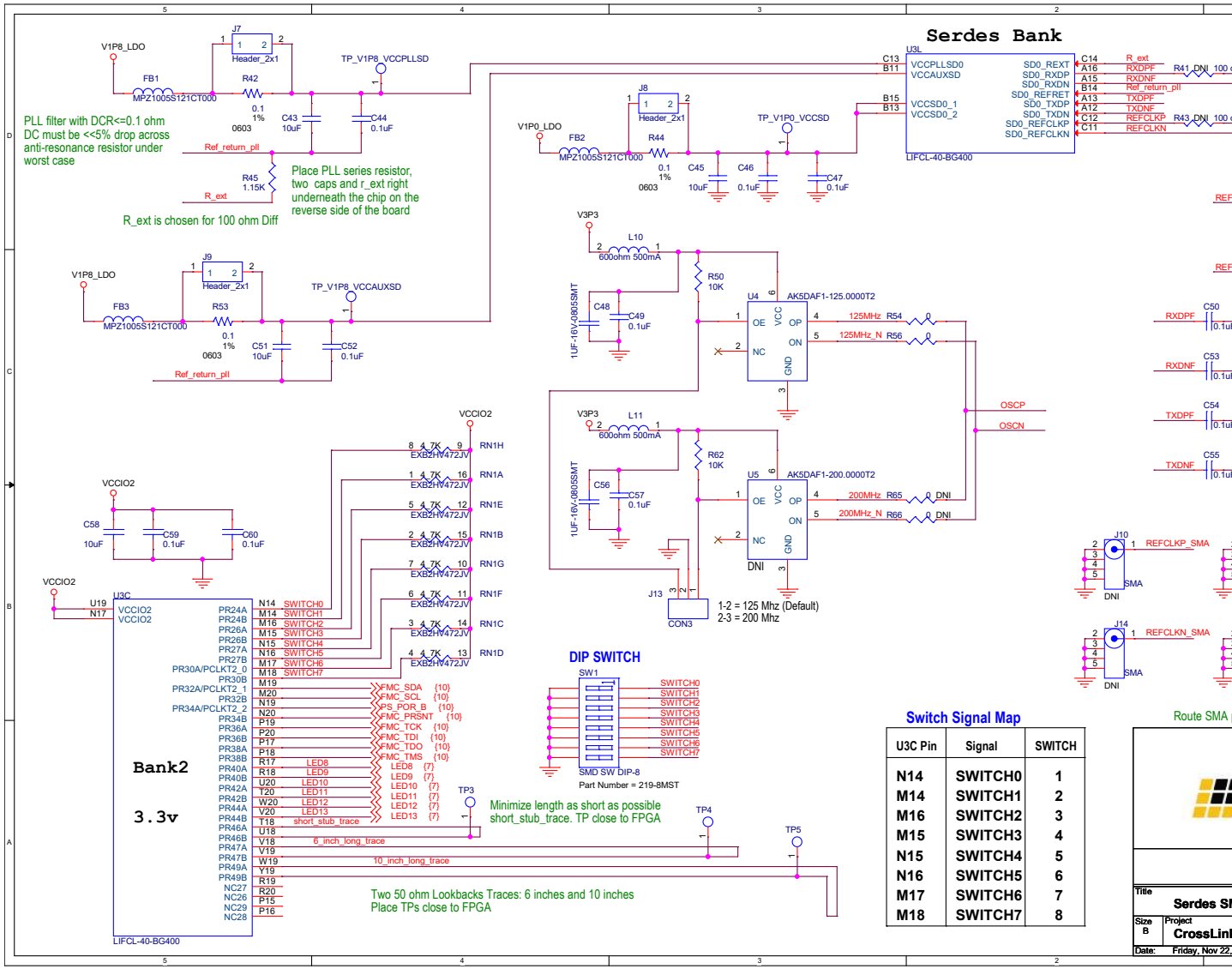

Figure A.6. SERDES SMAs/Switches/FMC Control

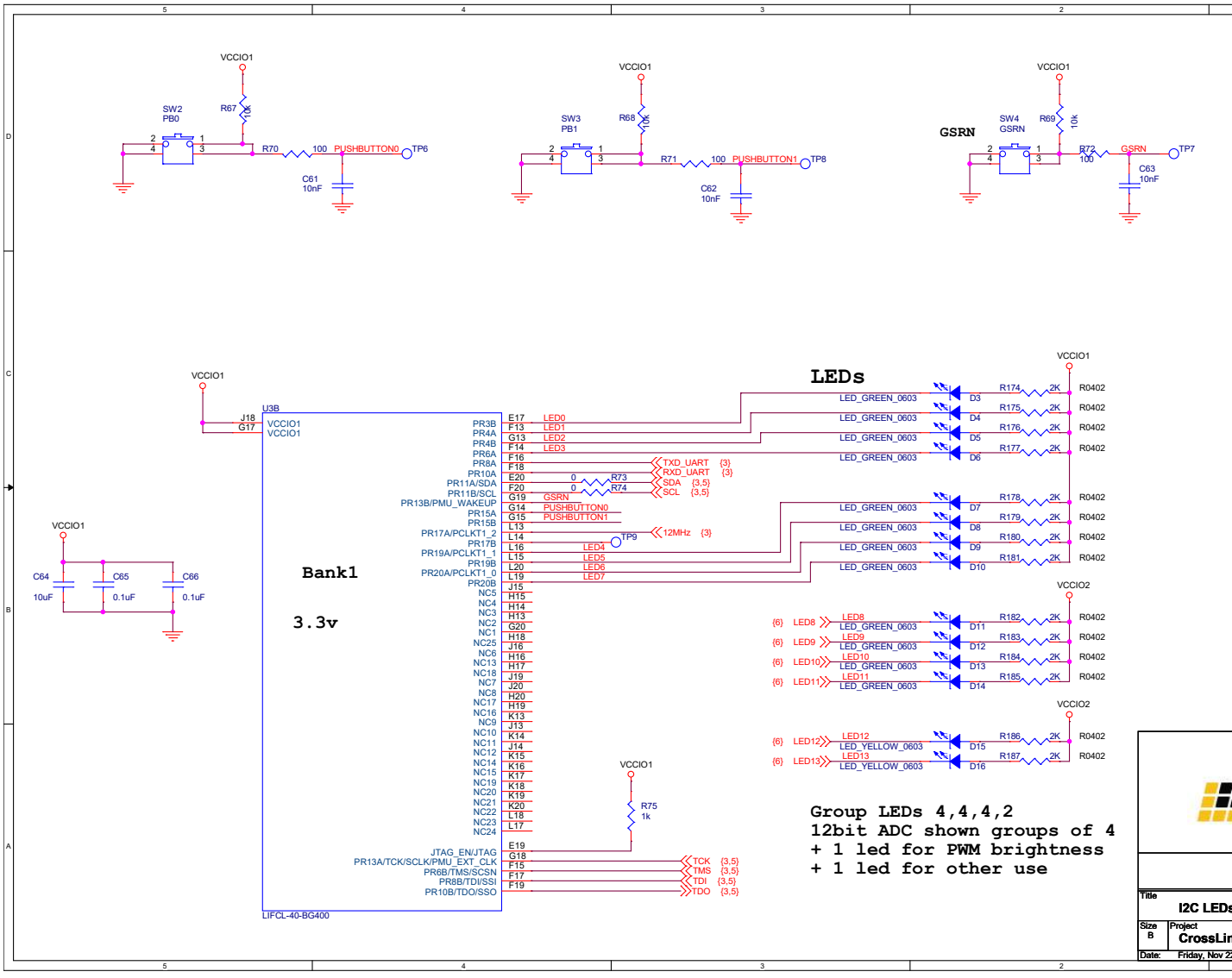

Figure A.7. I2C LEDs and Push Buttons

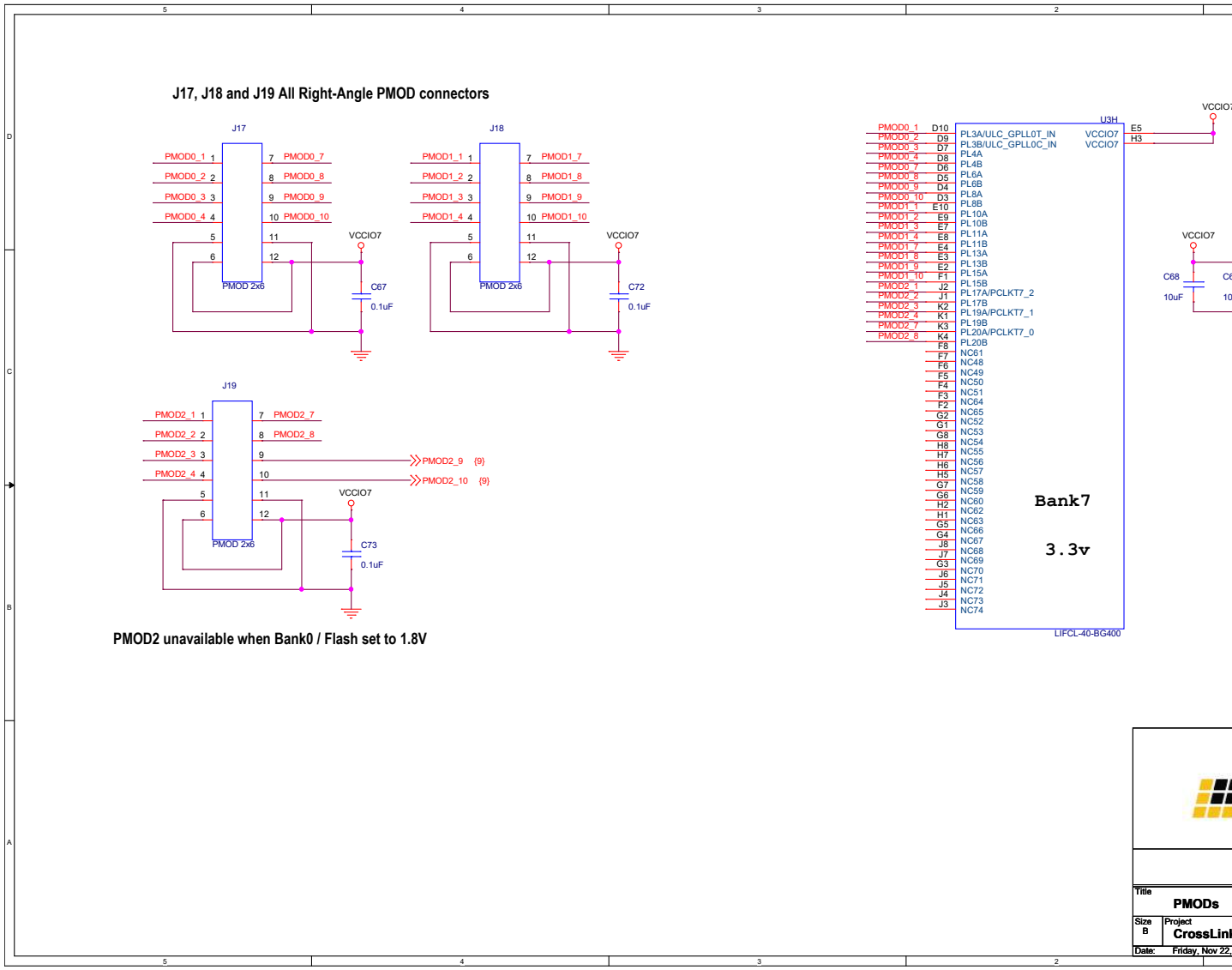

Figure A.8. PMODs

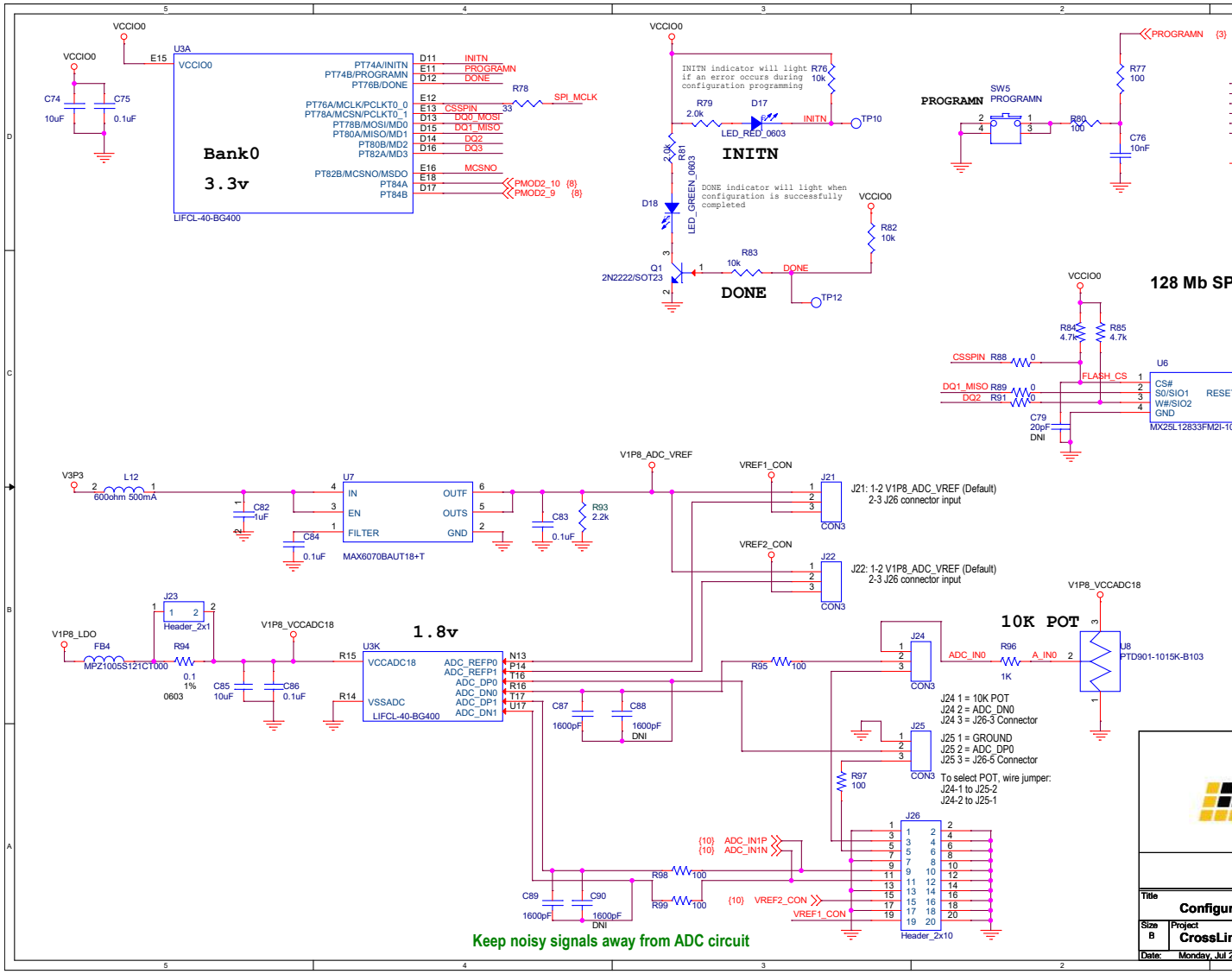

Figure A.9. Configuration and ADC

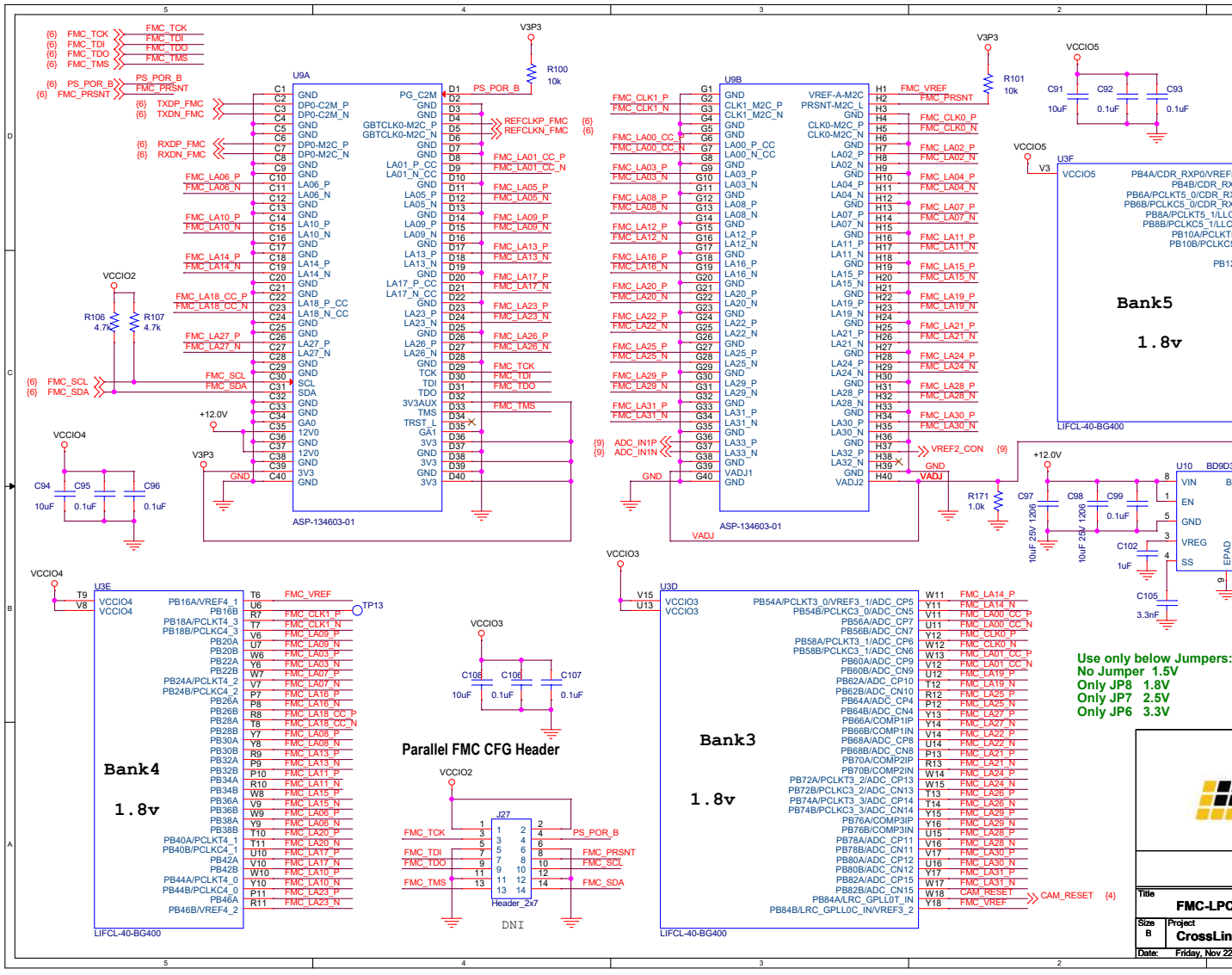

Figure A.10. FMC-LPC

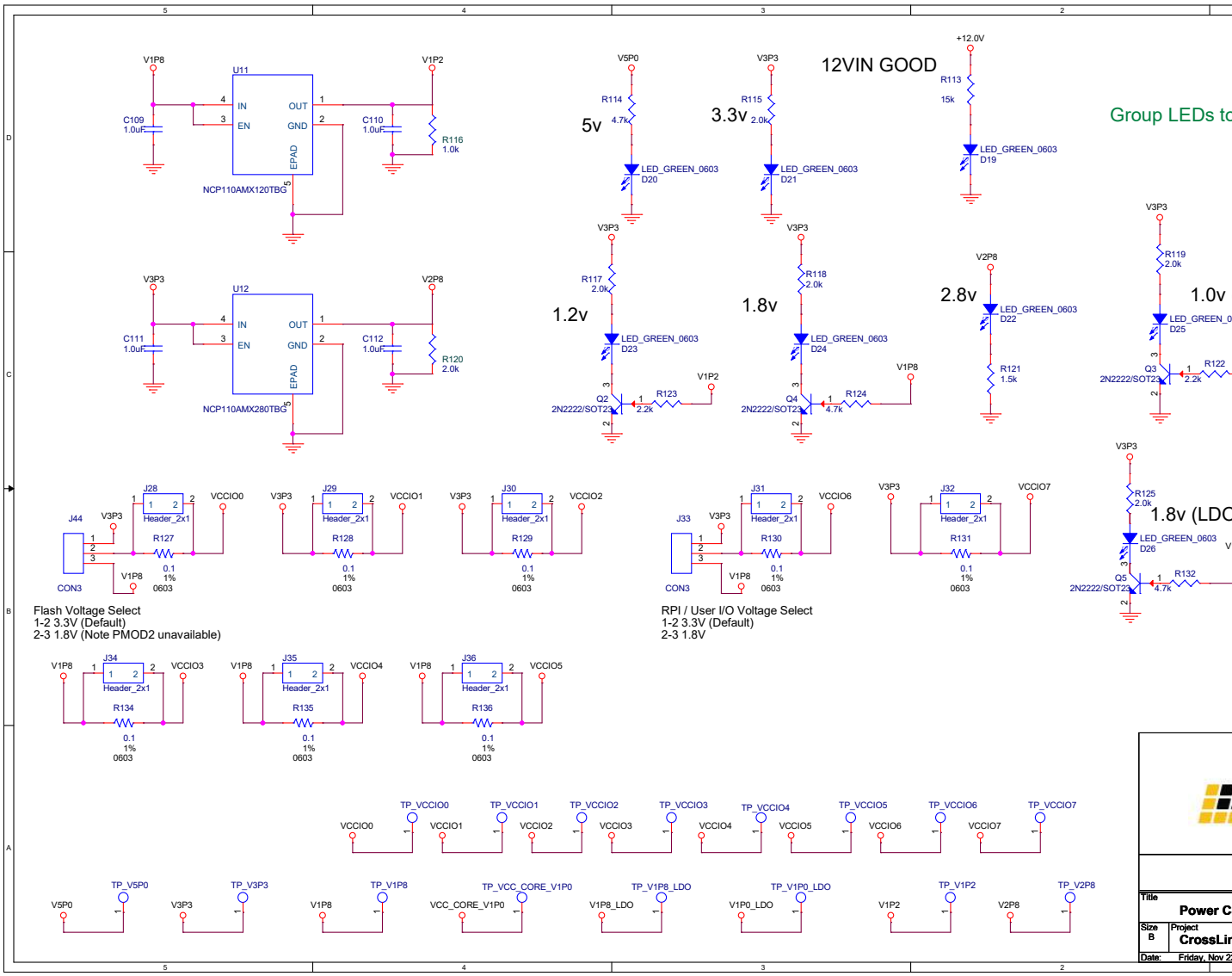

Figure A.11. Power CSI and Banks

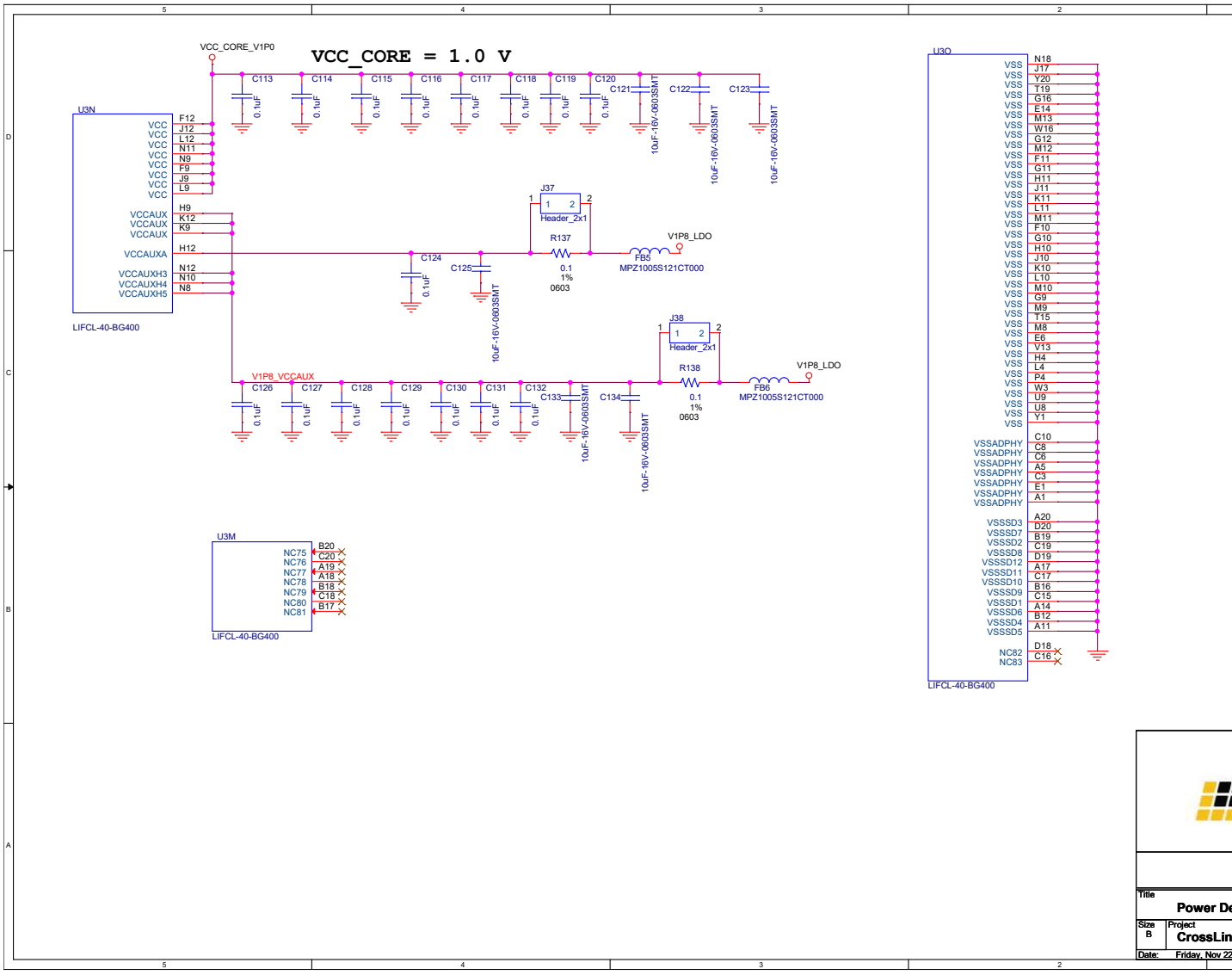

Figure A.12. Power Decoupling

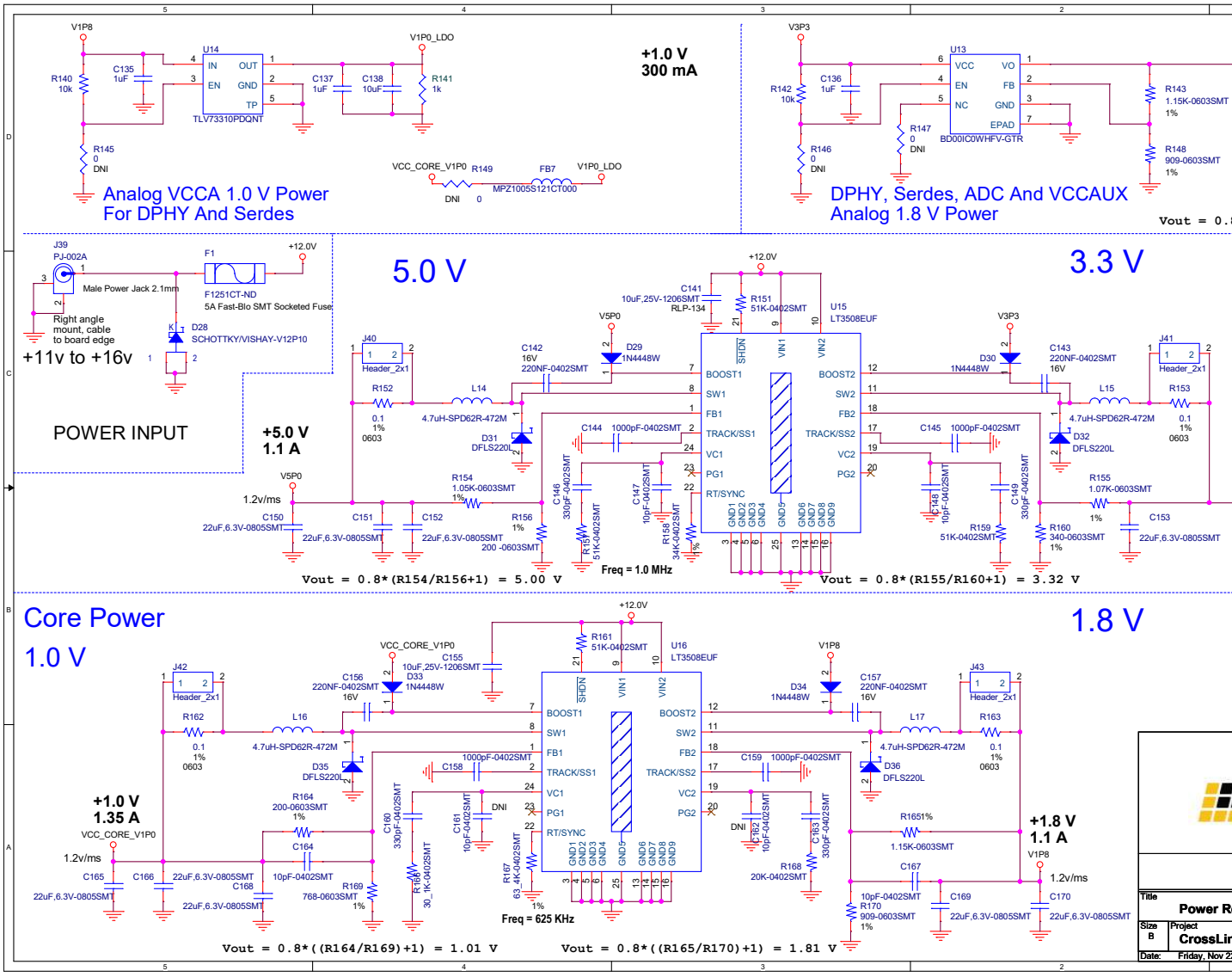

Figure A.13. Power Regulators

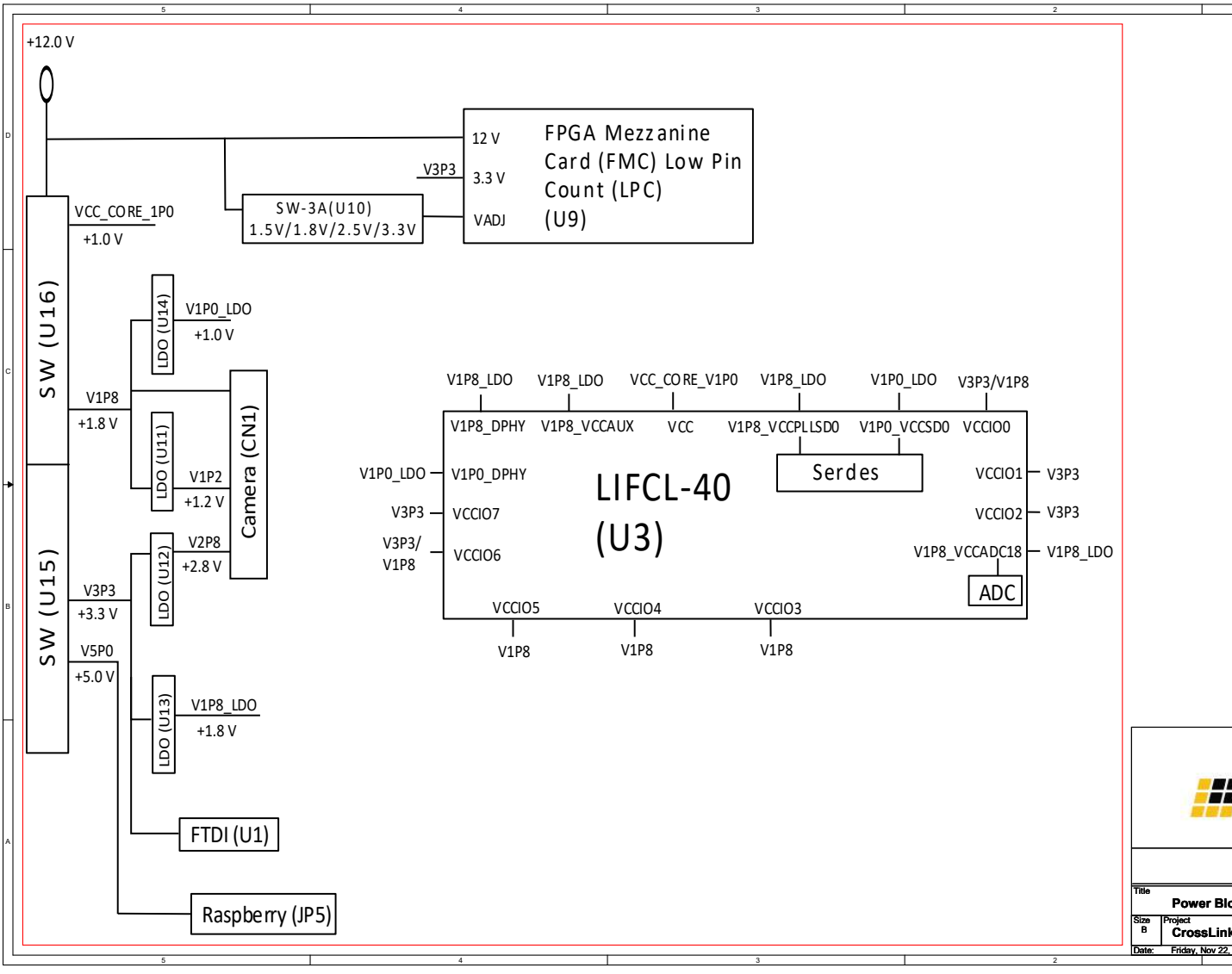

Figure A.14. Power Block Diagram

Appendix B. CrossLink-NX Evaluation Board Bill of Materials

Item	Reference	Qty	Part	PCB Footprint	Comments	Part Number	Manufacture
1	AG1,AF1,AE1,AD1,AC1, AB1,AA1,AG2,AF2,AE2, AD2,AC2,AB2,AA2,AG3, AF3,AE3,AD3,AC3,AB3, AA3,AG4,AF4,AE4,AD4, AC4,AB4,AA4,AG5,AF5, AE5,AD5,AC5,AB5,AA5, AG6,AF6,AE6,AD6,AC6, AB6,AA6,AG7,AF7,AE7, AD7,AC7,AB7,AA7,AG8, AF8,AE8,AD8,AC8,AB8, AA8,AG9,AF9,AE9,AD9, AC9,AB9,AA9,AG10,AF10, AE10,AD10,AC10,AB10, AA10,AG11,AF11,AE11, AD11,AC11,AB11,AA11	77	T POINT R	TP	DNL	—	—
2	CN1	1	camconn_imx258_1x30	camconn	—	24-5804-030-000-829+	Kyocera / Sur Optical
3	C1,C2,C3,C4,C7,C8,C9, C11,C12,C13,C15,C18, C19,C20,C24,C25,C27, C29,C31,C33,C35,C37, C38,C41,C42,C44,C46, C47,C49,C50,C52,C53, C54,C55,C57,C59,C60, C65,C66,C67,C70,C71, C72,C73,C75,C78,C83, C84,C86,C92,C93,C95, C96,C99,C100,C106, C107,C113,C114,C115, C116,C117,C118,C119, C120,C124,C126,C127, C128,C129,C130,C131, C132	73	0.1uF 0201	C0201	—	GRM033R61E104KE14J	Murata
4	C5,C14,C22,C39,C40, C58,C64,C68,C69,C74, C91,C94,C108,C121, C122,C123,C125,C133, C134,C138,C140	21	10uF-0603SMT	C0603	—	CL10A106MO8NQNC	Samsung

Item	Reference	Qty	Part	PCB Footprint	Comments	Part Number	Manufacture
5	C6,C10	2	4.7uF-0603SMT	C0603	—	CL10A475KA8NQNC	Samsung
6	C16,C17	2	18pF	C0402	—	CL05C180JB5NNNC	Samsung
7	C21,C23,C82,C102, C109,C110,C111,C112, C135,C136,C137,C139	12	1uF	C0603	—	TMK107B7105KA-T	Taiyo Yuden
8	C26,C28,C30,C32,C34, C36,C43,C45,C51,C85	10	10uF	C0402	—	CL05A106MP8NUB8	Samsung
9	C48,C56	2	1UF-16V-0805SMT	RLP-133	—	CL21B105KOFNNNG	Samsung
10	C61,C62,C63,C76,C77	5	10nF	RLP-130-A	—	GRM155R61C103KA01D	Murata
11	C79,C80,C81	3	20pF	RLP-132	DNL	—	—
12	C87,C89	2	1600pF	C0805	—	C0805C162J5GAC7800	Kemet
13	C88,C90	2	1600pF	C0805	DNL	C0805C162J5GAC7800	Kemet
14	C97,C98,C141,C155	4	10uF 25V 1206	C1206	—	TMK316BJ106KL-T	Taiyo Yuden
15	C101	1	0.1nF	C0603	—	CC0603JRNPO9BN101	Yageo
16	C103,C104	2	22uF	C0603	—	GRM188R61A226ME15D	Murata
17	C105	1	3.3nF	C0201	—	GRM033R71E332KA12D	Murata
18	C142,C143,C156,C157	4	220NF-0402SMT	RLP-130-A	—	CL05A224KO5NNNC	Samsung
19	C144,C145,C158,C159	4	1000pF-0402SMT	RLP-130-A	—	CL05B102KB5NFNC	Samsung
20	C146,C149,C160,C163	4	330pF-0402SMT	RLP-130-A	—	CL05B331KB5NNNC	Samsung
21	C147,C148,C164,C167	4	10pF-0402SMT	RLP-130-A	—	CL05C100CB5NNNC	Samsung
22	C150,C151,C152,C153,C 154,C165,C166,C168, C169,C170	10	22uF,6.3V-0805SMT	RLP-133	—	CL21A226KPCLRNC	Samsung
23	C161,C162	2	10pF-0402SMT	RLP-130-A	DNL	—	—

Item	Reference	Qty	Part	PCB Footprint	Comments	Part Number	Manufacture
24	D1,D3,D4,D5,D6,D7,D8, D9,D10,D11,D12,D13, D14,D18,D19,D20,D21, D22,D23,D24,D25,D26, D27	23	LED_GREEN_0603	APT1608	—	150060GS75000	Wurth
25	D2	1	ESDR0502N-UDFN6	UDFN6_040	—	ESDR0502NMUTBG	ON semi
26	D15,D16	2	LED_YELLOW_0603	APT1608	—	150060YS75000	Wurth
27	D17	1	LED_RED_0603	APT1608	—	150060RS75000	Wurth
28	D28	1	SCHOTTKY/VISHAY-V12P10	V12P10	—	V12P10-M3/86A	Vishay
29	D29,D30,D33,D34	4	1N4448W	1N4448W	—	1N4448WS	On Semi
30	D31,D32,D35,D36	4	DFLS220L	DFLS220L	—	DFLS220L-7	Diodes Incorporated
31	FB1,FB2,FB3,FB4,FB5, FB6,FB7,FB8	8	MPZ1005S121CT000	FB0402	—	MPZ1005S121CT000	TDK Corporat
32	F1	1	F1251CT-ND	154010	—	0154010.DR	Littelfuse Inc.
33	JP1,JP2,JP3,JP4,JP6,JP7, JP8	7	JUMPER	Header_1x2	—	61300211121	Wurth
34	JP5	1	Receptacle 20X2	HDR254-2X20_socket	DNL	ESQ-120-23-T-D	Samtec Inc.
35	J1	1	Header 1x8	hdr_amp_87220_8_1x8_100	DNL	22284081	Molex
36	J2	1	USB_MINI_B	USB_MINI_B-1734035-2	—	1734035-2	TE Connectivi AMP Connect
37	J3,J4,J5,J7,J8,J9,J23,J28, J29,J30,J31,J32,J34,J35, J36,J37,J38,J40,J41,J42, J43	21	Header_2x1	Header_2x1	Regular 100 Mil Header	—	—
38	J6,J26	2	Header_2x10	Header_2x10	—	61302021121	Wurth
39	J10,J11,J12,J14,J15,J16	6	SMA	901-10309	DNL	901-10309	Amphenol

Item	Reference	Qty	Part	PCB Footprint	Comments	Part Number	Manufacture
40	J13,J21,J22,J24,J25,J33, J44	7	CON3	CON3	Default : Pin 1 and 2	61300311121	Wurth
41	J17,J18,J19	3	PMOD 2x6	PPPC062LJBN -RC	—	PPPC062LJBN-RC	Sullins
42	J20,J27	2	Header_2x7	Header_2x7	DNL	—	—
43	J39	1	PJ-002A	pj_002a_3p	—	694106301002	Wurth
44	L1,L2,L3,L10,L11,L12	6	600ohm 500mA	fb0603	—	BLM18AG601SN1D	Murata
45	L4,L5,L6,L7,L8,L9	6	220ohm 500mA	FB0402	—	CIM05U221NC	Samsung
46	L13	1	2.2uH SPM6530T-2R2M	SPM6530T-2R2M	—	SPM6530T-2R2M	TDK Corporat
47	L14,L15,L16,L17	4	4.7uH-SPD62R-472M	SPD62R	—	SPD62R-472M	API Delevan I
48	Q1,Q2,Q3,Q4,Q5,Q6	6	2N2222/SOT23	MMBT2222AL T-1	—	MMBT2222ALT1G	ON Semiconducto
49	RN1	1	EXB2HV472JV	EXB-2HV	—	EXB2HV472JV	Panasonic
50	R1,R2,R3,R102,R103, R104	6	4.7K	R0603	—	RC0603FR-074K7L	yageo
51	R4,R9,R105	3	2.2K	R0603	—	RC0603FR-072K2L	yageo
52	R5,R78	2	33	R0402	—	ERJ-2RKF33R0X	Panasonic
53	R6,R7,R8,R20,R21,R22	6	0	R0603	—	RC0603JR-070RL	Yageo
54	R10,R11,R12,R172	4	10K	R0603	—	RC0603FR-0710KL	Yageo
55	R13,R16	2	12K	R0603	—	RC0603FR-0712KL	yageo
56	R14	1	2K-0603SMT	RLP-101	—	RC0603FR-072KL	Yageo
57	R15,R17,R35,R36,R37, R38,R39,R40,R145, R146,R147,R149,R150	13	0	R0603	DNL	RC0603JR-070RL	Yageo
58	R18,R19	2	4_7K-0603SMT	RLP-101	—	CRCW06034K70FKEA	Vishay

Item	Reference	Qty	Part	PCB Footprint	Comments	Part Number	Manufacture
59	R23	1	100k	R0402	—	ERJ-2RKF1003X	Panasonic
60	R24	1	22	R0402	—	ERJ-2RKF22R0X	Panasonic
61	R25,R26,R84,R85,R87, R106,R107,R114,R124, R132	10	4.7k	R0402	—	ERJ-2GEJ472X	Panasonic
62	R27,R28,R29,R30,R31, R41,R43	7	100 ohm 0201	R0201	DNL	RC0201FR-07100RL	Yageo
63	R32,R33,R34,R42,R44, R53,R94,R127,R128, R129,R130,R131,R134, R135,R136,R137,R138, R152,R153,R162,R163	21	0.1	603	—	ERJ-3RSFR10V	Panasonic
64	R45	1	1.15K-0402SMT	R0402	—	RC0402FR-071K15L	Yageo
65	R46,R49,R54,R55,R56,R 58,R60,R63,R73,R74,R8 8,R89,R90,R91,R92	15	0	R0402	—	ERJ-2GE0R00X	Panasonic
66	R47,R48,R51,R52,R57, R59,R61,R64,R65,R66	10	0	R0402	DNL	ERJ-2GE0R00X	Panasonic
67	R50,R62,R67,R68,R69, R76,R82,R83,R100, R101,R140,R142	12	10K	RLP-100	—	RC0402FR-0710KL	Yageo
68	R70,R71,R72,R77,R80	5	100	R0402	—	RC0402FR-07100RL	Yageo
69	R75,R108,R116,R141, R144,R171	6	1.00k 1%	R0402	—	ERJ-2RKF1001X	Panasonic
70	R79,R81,R115,R117, R118,R119,R120,R125, R126	9	2.0k	R0402	—	ERJ-2RKF2001X	Panasonic
71	R86	1	1k	R0402	DNL	ERJ-2RKF1001X	Panasonic
72	R93,R122,R123,R133	4	2.2k	R0402	—	ERJ-2RKF2201X	Panasonic
73	R95,R97,R98,R99	4	100	R0805	—	ERJ-6ENF1000V	Panasonic
74	R96	1	1K	R0805	—	ERJ-6ENF1001V	Panasonic

Item	Reference	Qty	Part	PCB Footprint	Comments	Part Number	Manufacture
75	R109	1	1.02k 1%	R0402	—	ERJ-2RKF1021X	Panasonic
76	R110	1	2.55k 1%	R0402	—	ERJ-2RKF2551X	Panasonic
77	R111	1	750 1%	R0402	—	ERJ-2RKF7500X	Panasonic
78	R112	1	422 1%	R0402	—	ERJ-2RKF4220X	Panasonic
79	R113	1	15k	RLP-103	—	ERJ-8GEYJ153V	Panasonic
80	R121	1	1.5k	R0402	—	ERJ-2GEJ152X	Panasonic
81	R143,R165	2	1.15K-0603SMT	RLP-101	—	RC0603FR-071K15L	Yageo
82	R148,R170	2	909-0603SMT	RLP-101	—	RC0603FR-07909RL	Yageo
83	R151,R157,R159,R161	4	51K-0402SMT	RLP-100	—	RC0402FR-0751KL	yageo
84	R154	1	1.05K-0603SMT	RLP-101	—	RC0603FR-071K05L	Yageo
85	R155	1	1.07K-0603SMT	RLP-101	—	RC0603FR-071K07L	Yageo
86	R156,R164	2	200 -0603SMT	RLP-101	—	RC0603FR-07200RL	Yageo
87	R158	1	34K-0402SMT	RLP-100	—	RC0402FR-0734KL	Yageo
88	R160	1	340-0603SMT	RLP-101	—	RC0603FR-07340RL	Yageo
89	R166	1	30_1K-0402SMT	RLP-100	—	ERJ-2RKF3012X	Panasonic
90	R167	1	63_4K-0402SMT	RLP-100	—	ERJ-2RKF6342X	Panasonic
91	R168	1	20K-0402SMT	RLP-100	—	ERJ-2RKF2002X	Panasonic
92	R169	1	768-0603SMT	RLP-101	—	RC0603FR-07768RL	Yageo
93	R173	1	1.0 K	R0603	DNL	RC0603FR-071KL	Yageo

Item	Reference	Qty	Part	PCB Footprint	Comments	Part Number	Manufacture
94	R174,R175,R176,R177, R178,R179,R180,R181, R182,R183,R184,R185, R186,R187	14	2K	R0402	—	ERJ-2GEJ202X	Panasonic
95	SW1	1	SMD SW DIP-8	219-8MST	—	219-8MST	CTS Electrocompo ts
96	SW2,SW3,SW4,SW5	4	Push Button	4psmd_switch	—	434153017835	Wurth
97	TP_VCCIO1,TP_VCCIO2, TP_VCCIO3,TP_VCCIO4, TP_VCCIO5,TP_VCCIO6, TP_VCCIO7, TP_VCC_CORE_V1P0, TP_V1P0_VCCSD, TP_V1P0_LDO, TP_V1P2, TP_V1P8_VCCPLLSD, TP_V1P8_VCCAUXSD, TP_V1P8_LDO, TP_V1P8,TP_V2P8, TP_V3P3,TP_V5P0, TP_VCCIO0,TP_VADJ	20	TP_S_40_63	tp_s_40_63	DNL	—	—
98	TP1,TP2,TP3,TP4,TP5	5	TP_S_40_63	TP	DNL	—	—
99	TP6,TP7,TP8,TP9,TP10, TP12,TP13	7	TestPoint	TP50	DNL	—	—
100	U1	1	FT2232HL	tqfp64_0p5_12p2x12p2_h1p6	Customer Supplied	FT2232HL	FTDI
101	U2	1	93LC56C-I/SN	so8_50_244	—	93LC56C-I/SN	Microchip
102	U3	1	LIFCL-40-BG400	LIFCL-40-BG400	Customer Supplied	—	—
103	U4	1	AK5DAF1-125.0000T2	XTAL_AK5DAF1	—	AK5DAF1-125.0000T2	Abracon LLC
104	U5	1	AK5DAF1-200.0000T2	XTAL_AK5DAF1	DNL	AK5DAF1-200.0000T2	Abracon LLC
105	U6	1	MX25L12833FM2I-10G	SO8_MX25L12833FM2I10G	—	MX25L12833FM2I-10G	Macronix

Item	Reference	Qty	Part	PCB Footprint	Comments	Part Number	Manufacture
106	U7	1	MAX6070BAUT18+T	SOT23-6_MAX6070	—	MAX6070BAUT18+T	Maxim Integr
107	U8	1	PTD901-1015K-B103	PTD901_1015K_B103	—	PTD901-1015K-B103	Bourns Inc.
108	U9	1	ASP-134603-01	ASP_134603_01	—	ASP-134603-01	Samtec Inc.
109	U10	1	BD9D321EFJ	HTSOP_8_BD9D321	—	BD9D321EFJ-E2	Rohm Semiconducto
110	U11	1	NCP110AMX120TBG	4XDFN_NCP110	—	NCP110AMX120TBG	ON Semiconducto
111	U12	1	NCP110AMX280TBG	4XDFN_NCP110	—	NCP110AMX280TBG	ON Semiconducto
112	U13	1	BD00IC0WHFV-GTR	6HVSOF_BD00IC0WHFV	—	BD00IC0WHFV-GTR	Rohm Semiconducto
113	U14	1	TLV73310PDQNT	4X2SON	—	TLV73310PDQNT	Texas Instruments
114	U15,U16	2	LT3508EUF	LT3508EUF	—	LT3508EUF#PBF	Linear Technology/Analog Devices
115	X1	1	7M-12.000MAAJ	xtal_4p_7m	—	7M-12.000MAAJ-T	TXC
116	X2	1	ASE3-27.000MHz-K-T	27MHZ	—	ASE3-27.000MHz-K-T	ABRACON
117	Shunt For Headers (BOM Line Item 40): J13,J21,J22,J24,J25,J33,J44	7	—	—	—	SPC02SYAN	Sullins Connectors Solutions
118	CN1	1	Camera Module with IMX258	—	DNL	—	—
119	Camera Bracket	1	—	—	DNL	—	—
120	#8-32 Screw	1	—	—	DNL	—	—
121	CrossLink NX Evaluation Board PCB RevB	1	—	—	—	305-PD-19-0943	PACTRON

Appendix C. Fast Configuration Issues

Early versions of the Evaluation Board were assembled with LIFCL-40-9BG400CES (ES suffix, Engineering Sample) devices. With -ES silicon, an Early I/O Release enabled bitstream is not compatible with the direct SRAM configuration *Fast Configuration* operation in Lattice Radiant Programmer. If attempted, the configuration operation will fail, since the board has Early I/O bitstream burned in onboard flash. Erasing flash and power cycling the board is suggested before executing *Fast Configuration*. Otherwise, you should select the SRAM *Erase, Program, Verify* operation in Lattice Radiant Programmer.

Appendix D. Schematics Updates for ADC Test

Early versions of the schematic (Appendix A) contained errors, with pin swaps in Bank 0 and ADC symbol parts (reference designators U3A and U3K, respectively). These symbol errors have been corrected in the current schematic (Revision B-1 and later).

As a result of the original error, the ADC channel 0 test access circuit is connected incorrectly: J24 is connected to the negative input and J25 is connected to the positive input (see Figure A.9).

To effectively utilize the ADC test access circuit on the Crosslink-NX Evaluation Board Revision B, follow these guidelines:

- For single-ended use, voltages applied to J25-2 should be positive relative to voltages applied to J24-2. Do not use shunt position 1-2 for either J24 and J25.
- For single-ended testing utilizing the voltage generated by the 10 KΩ potentiometer U8:
  - Use a jumper wire to connect J24-1 and J25-2, connecting the POT to channel 0 POS input (ADC_DP0).
  - Use a jumper wire to connect J24-2 and J25-1, connecting channel 0 NEG input (ADC_DN0) to ground.
- For differential testing, connect the signals directly to Pin 2 of J24 and J25, or use header J26.
- To route the ADC signals to header J26, use shunt positions 2-3 of both J24 and J25 to connect ADC_DN0 to connector J26-3 and ADC_DP0 to connector J26-5.

References

Lattice Semiconductor Documents

Related documents available from your Lattice Semiconductor sales representative are listed on the table below.

Document	Title
FPGA-UG-02042	Programming Cables
FPGA-DS-02049	CrossLink-NX Family Data Sheet
FPGA-TN-02099	CrossLink-NX sysCONFIG Usage Guide

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.3, November 2020

Section	Change Summary
Headers/Connectors and LIFCL-40 Device Ball Mapping	Made the following revisions in Table 8.1. FMC LPC Header Pin Connections. • Changed G32 pin to V16 • Changed G34 pin to W17
—	Corrected table numbering in chapters 7 and 8.

Revision 1.2, August 2020

Section	Change Summary
Introduction	Added Figure 1.3. Silkscreen of CrossLink-NX Evaluation Board and Figure 1.4. Silkscreen of CrossLink-NX Evaluation Board (Bottom).
Jumpers and Test Connection	Updated J24 and J25 usage for ADC testing in Table 2.1. Jumper Table.
Appendix A. CrossLink Evaluation Board Schematics	Updated schematics to version B-1.
Appendix D. Schematics Updates for ADC Test	Added this section.

Revision 1.1, March 2020

Section	Change Summary
Introduction	• Added Potentiometer for ADC test feature. • Added call-outs to Figure 1.2. Bottom View of CrossLink-NX Evaluation Board. • Updated the CrossLink-NX Device and the Applying Power to the Board sections.
Appendix C. Fast Configuration Issues	Added this section.

Revision 1.0, December 2019

Section	Change Summary
All	Initial release

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