Five Output Power System for Zynq-7020 All Programmable SoC

June 2016 Rev. 1.0.1

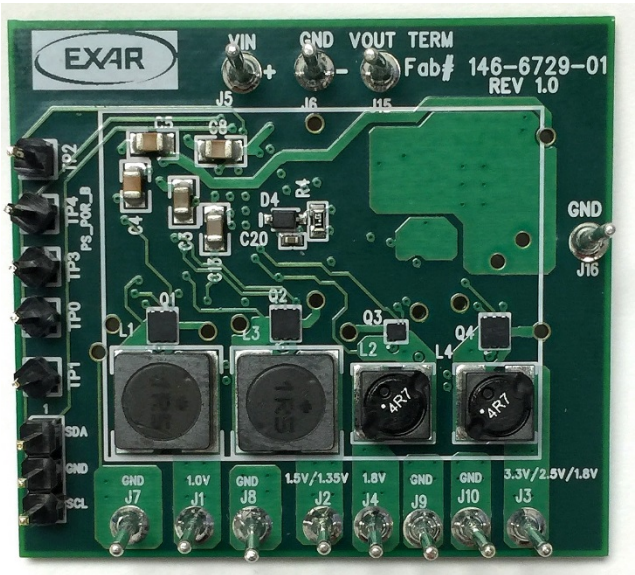
GENERAL DESCRIPTION

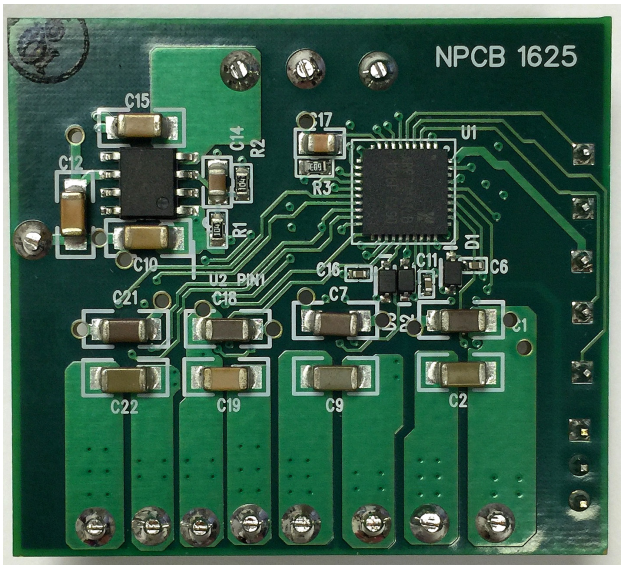
This reference design is a complete five-output power system designed to power a Xilinx Zynq-7020 All Programmable (AP) SoC and associated DDR3 memory in Industrial Ethernet applications. This reference design is focused on Industrial Ethernet applications leveraging HMS's Anybus IP on Xilinx. Although the power requirements of the core system building blocks remain relatively constant, the flexibility of Exar's Universal PMICs provides a power solution that can power the wider system requirements, whether a motor control board or human interface module.

The power system provides V_{CCPINT}, V_{CCINT} and V_{CCBRAM} 1.00V, V_{CCO_DDR} programmable to 1.2/1.35/1.5V, V_{TT} 0.60/0.675/0.75V, V_{CCAUX} and V_{CCADC} 1.8V and V_{CCO} programmable from 1.8V to 3.3V. The entire power system fits in less than one square inch. The order and ramp rates for each supply are programmed to accommodate Zynq-7020 sequencing requirements. All power supply operations can be controlled over an I^2C interface. Faults, output voltages and currents can also be monitored. 4 GPIO signals are available and can be programmed to provide the status of power good signals, enables, and faults. The board is supported by PowerArchitect™ 4.x and connects to the Exar Communications Module (XR77XXEVB-XCM-V80).

FEATURES

- **Xilinx Zynq-7020 All Programmable SoC Power System**
  - 4 Channel Power System using XRP7714 Programmable Digital PWM Switching Controller
  - V_{CCPINT}, V_{CCINT} and V_{CCBRAM} 1.0V
  - V_{CCO_DDR} programmable to 1.2/1.35/1.5V
  - V_{TT} 0.60/0.675/0.75V
  - V_{CCO} programmable to from 1.8V to 3.3V
  - V_{CCAUX} and V_{CCADC} 1.8V
- **I^2C Interface**
  - Programming
  - Monitoring
  - Control

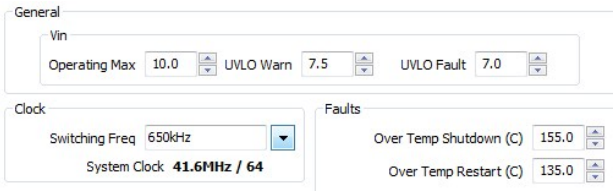




ZYNQ-7020 AP SOC POWER SOLUTION

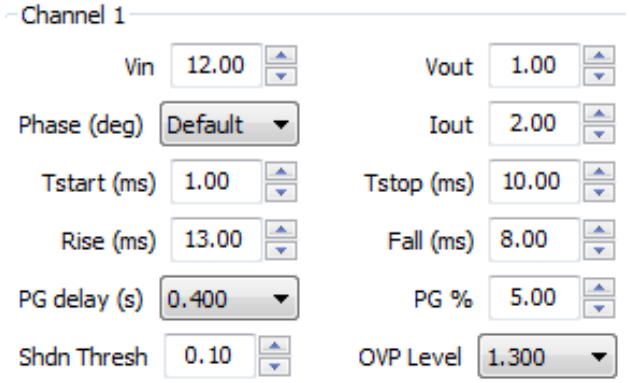
The Zynq-7020 AP SoC power reference design provides 4 output voltages. The order and ramp rates for each output are programmed to accommodate Zynq-7020 AP SoC sequencing requirements.

The power system was designed to operate at 650kHz as a good trade-off between space and efficiency.



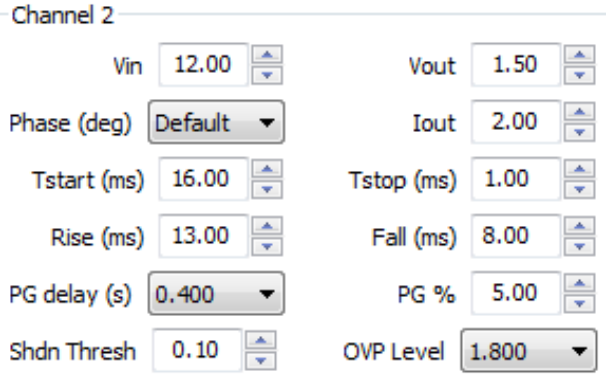
Output 1/Channel 1 Configuration

Channel 1 is designed to provide 1V to V_{CCINT}, V_{CCBRAM} and V_{CCPINT} Zynq-7020 AP SoC rails at 2.0A. However, the hardware is capable of supporting output currents up to 3Amps.



Output 2/Channel 2 Configuration

Channel 2 provides 1.5V to the DDR3 SDRAM subsystem as well as the DDR3 block inside the Zynq-7020 AP SoC. In addition, it sources the XRP2997 DDR Bus Termination Regulator which provides termination voltage for the DDR3 SDRAM signals. The channel is configured for a 2.0A output, but the hardware is capable of supporting up to a 3Amp load.

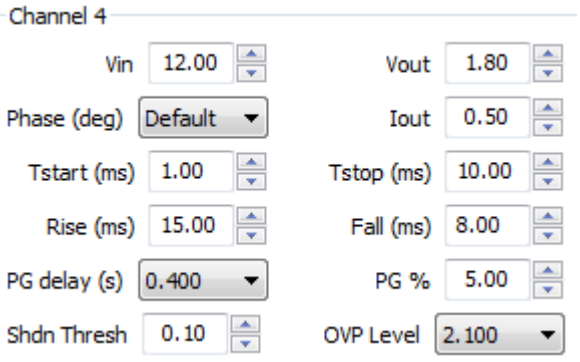


Output 3/Channel 3 Configuration

Channel 3 provides 2.5V to Zynq-7020 AP SoC IO banks (V_{CCO}) and peripherals in the system. The channel is configured for a 1.5A output, but the hardware is capable of supporting up to a 2Amp load.

Output 4/Channel 4 Configuration

Channel 4 is designed to provide 1.8V to V_{CCAUX} and V_{CCADC} Zynq-7020 AP SoC rails at 0.5A. The channel is configured for a 0.5A output, but the hardware is capable of supporting up to a 1.5Amp load.



LDOOUT

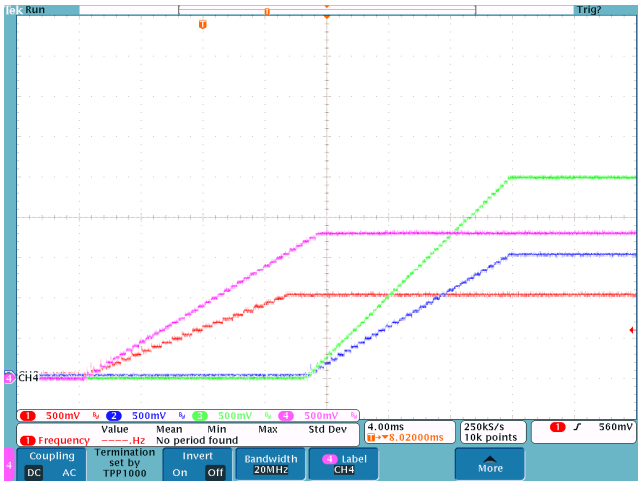
LDOOUT is routed to XRP2997 control pin enabling the device.

CHANNEL SEQUENCING

The XRP7714 sequencing has been designed to meet the Zynq-7020 AP SoC power up sequencing requirements.

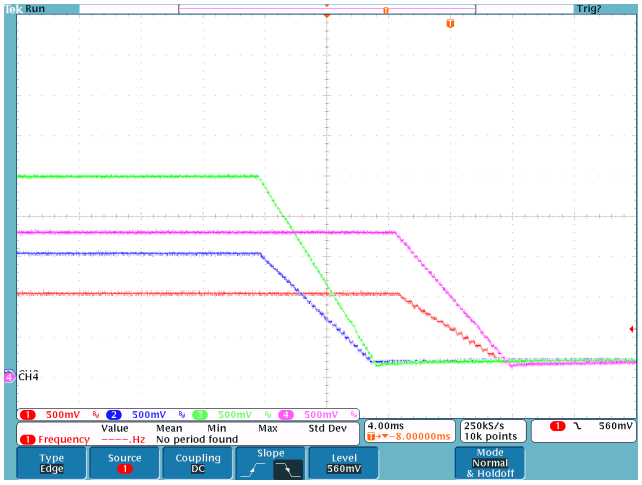
Power-On Sequencing

1. **1.0V** supply with 0.077V/msec ramp rate
2. **1.8V** supply with 0.12V/msec ramp rate
3. **1.5V and 2.5V supplies** - the 1.5V supply with 0.115V/msec ramp rate reaching the target level at the same time as the 2.5V supply with 0.192V/msec ramp rate.



Power-Down Sequencing

1. **1.5V and 2.5V supplies** – the 1.5V supply following 0.1875V/msec ramp down rate; the 2.5V supply following 0.3125V/msec ramp down rate. Both channels regulate down to the shutdown threshold of 100mV before switching stops.
2. **1.0V and 1.8V supplies** – the 1.0V supply following 0.125V/msec ramp down rate; the 1.8V supply following 0.225V/msec ramp down rate. Both channels regulate down to the shutdown threshold of 100mV before switching stops.



ZYNQ-7020 AP SOC POWER ON RESET

XRP7714 will generate a power on reset signal on GPIO3 to the Zynq-7020 AP SoC 400ms after the last rail is in regulation.

POWERING UP THE BOARD

The board hardware is provided capable of supporting an input voltage range of 5.5V to 15V with power connected directly to J5 (VIN) and J6 (GND).

I²C Interface

The Zynq-7020 AP SoC power reference design schematic shows an I²C interface connector (HDR2) to connect the Exar Communications Module (XR77XXEVB-XCM-V80 which has its own users guide available). This provides an interface with PowerArchitect™ 4.x allowing programming of the board.

Ensure the XCM is configured to use the on board pull-up resistors (check jumper settings).

If communication between Zynq-7020 AP SoC and XRP7714 is desired, ensure that the Zynq-7020 AP SoC system board has pull-up resistors installed.

For more information how to implement power subsystem control and monitoring via I²C bus refer to ANP-31.

Configuring the Board

The board is typically delivered with a XRP7714 which has not yet had its OTP memory burned with a specific configuration. This allows the user to select a different VIO voltage or DDR memory voltage than the one used in the default configuration file available from Exar's web site.

https://www.exar.com/products/zynq-7020

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at V_{IN} = 12V, f_{SW}=650kHz, $T_J = T_A$ = 25°C, unless otherwise specified

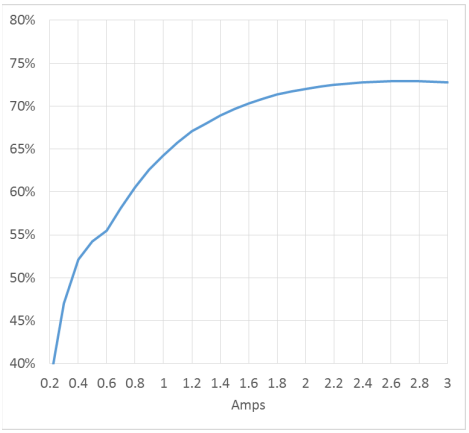


Fig. 1: Channel 1, 1.0V Efficiency

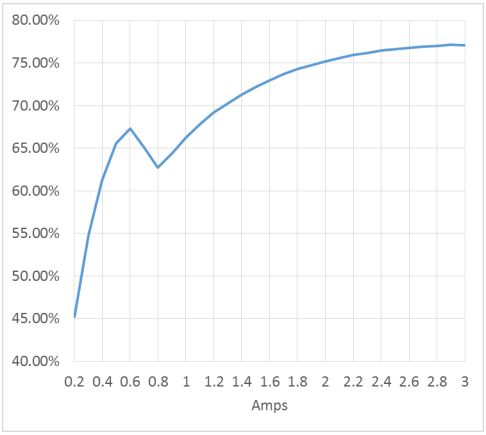


Fig. 2: Channel 2, 1.5V Efficiency

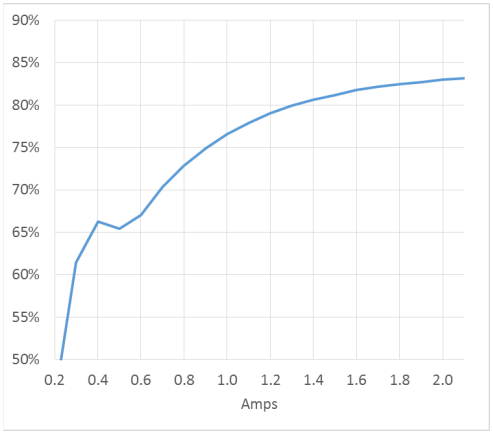


Fig. 3: Channel 3, 2.5V Efficiency

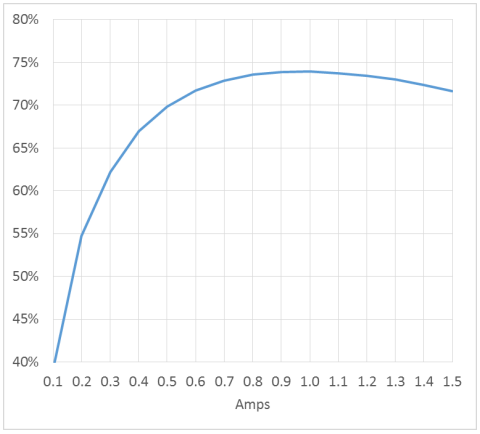


Fig. 4: Channel 4, 1.8V Efficiency

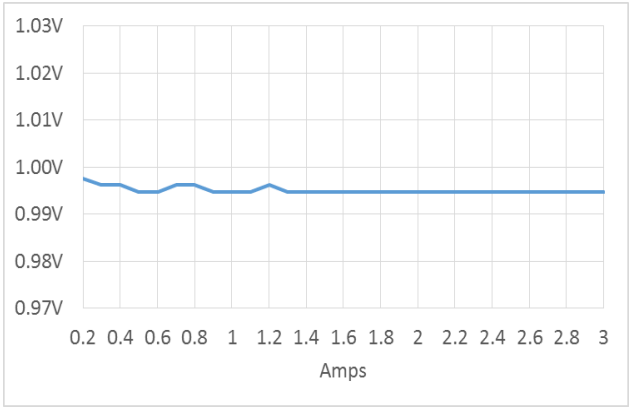


Fig. 5: Channel 1, 1.0V Load Regulation

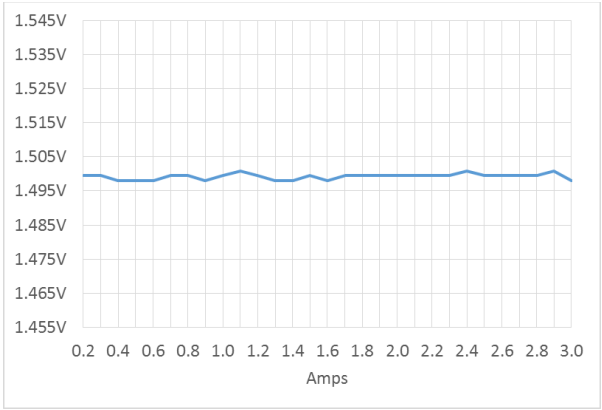


Fig. 6: Channel 2, 1.5V Load Regulation

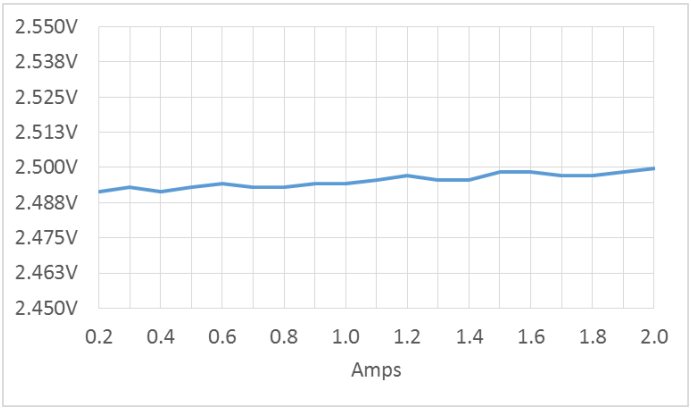


Fig. 7: Channel 3, 2.5V Load Regulation

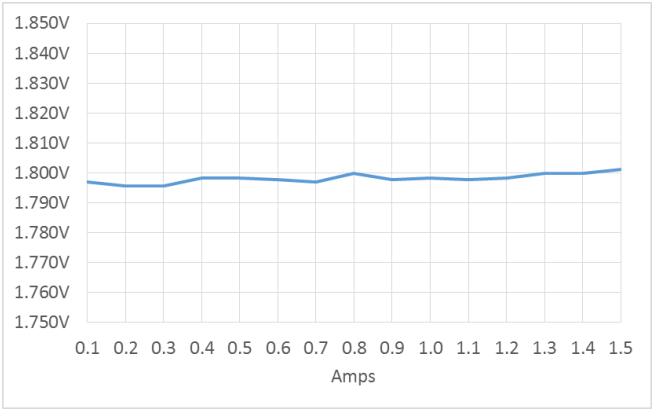


Fig. 8: Channel 4, 1.8V Load Regulation

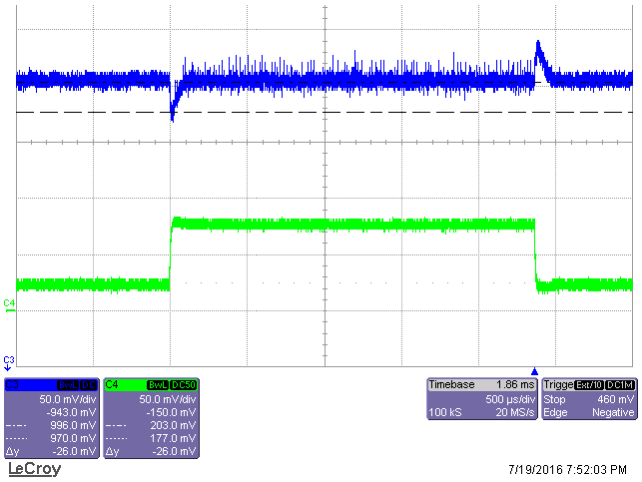


Fig. 9: Channel 1, 1.0V Load Transient
25% - 75% 5A/us

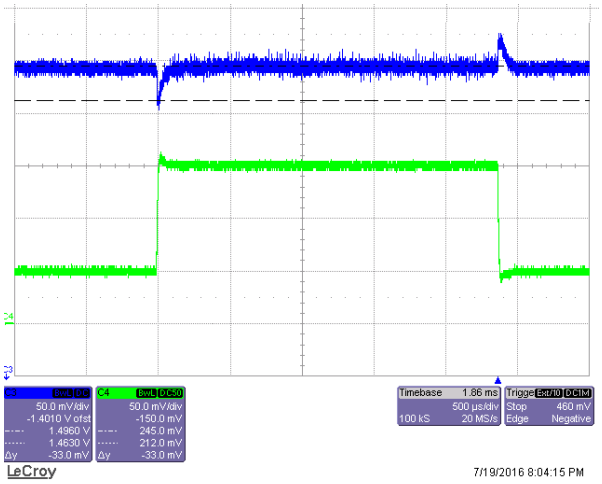


Fig. 10: Channel 2, 1.5V Load Transient
25% - 75% 5A/us

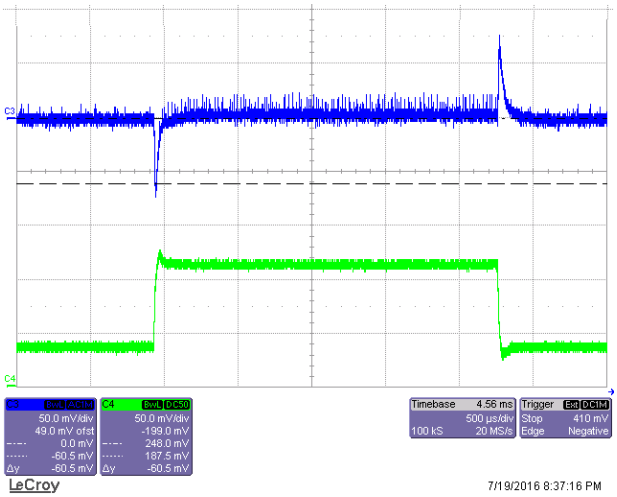


Fig. 11: Channel 3, 2.5V Load Transient
25% - 75% 5A/us

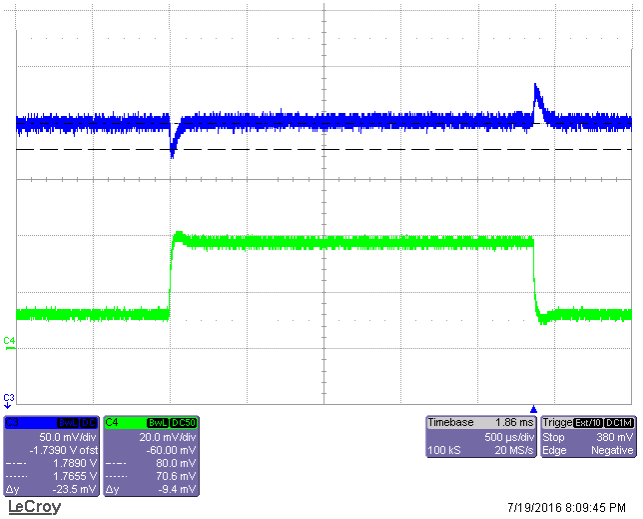


Fig. 12: Channel 4, 1.8V Load Transient
25% - 75% 5A/us

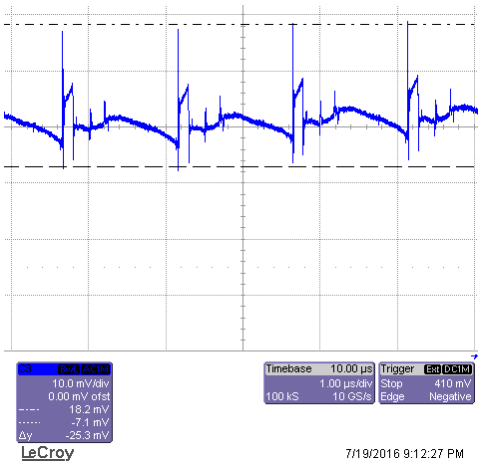


Fig. 13: Channel 1, 1.0V Full Load Output Ripple

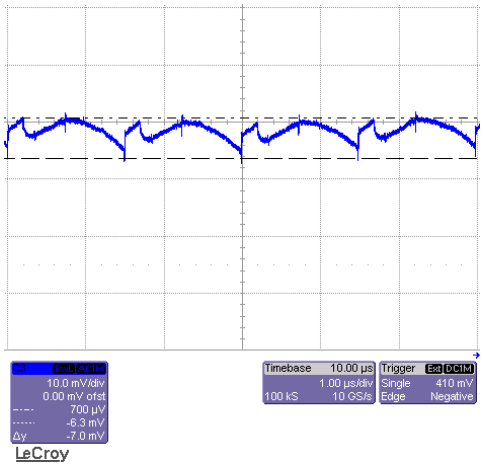


Fig. 14: Channel 2, 1.5VV Full Load Output Ripple

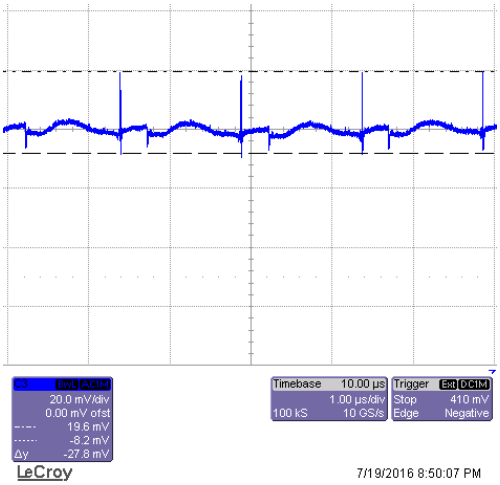


Fig. 15: Channel 3, 2.5V Full Load Output Ripple

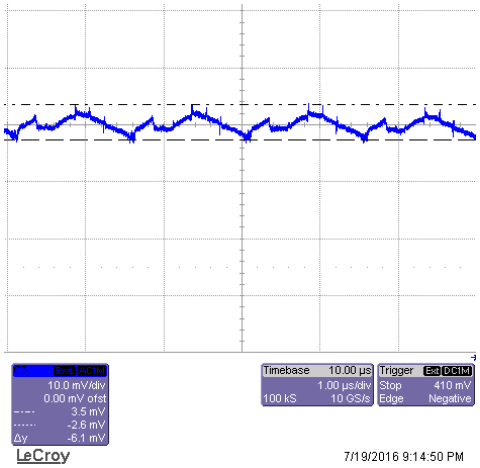


Fig. 16: Channel 4, 1.8V Full Load Output Ripple

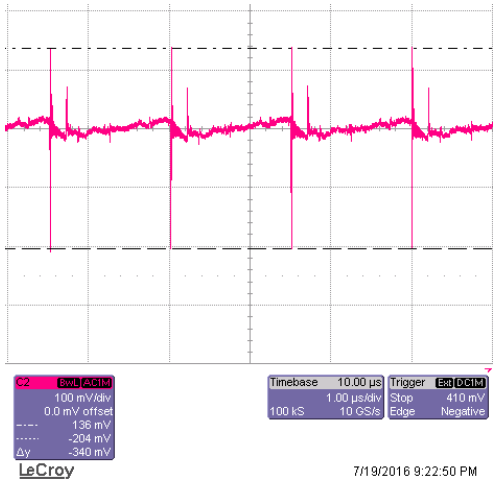
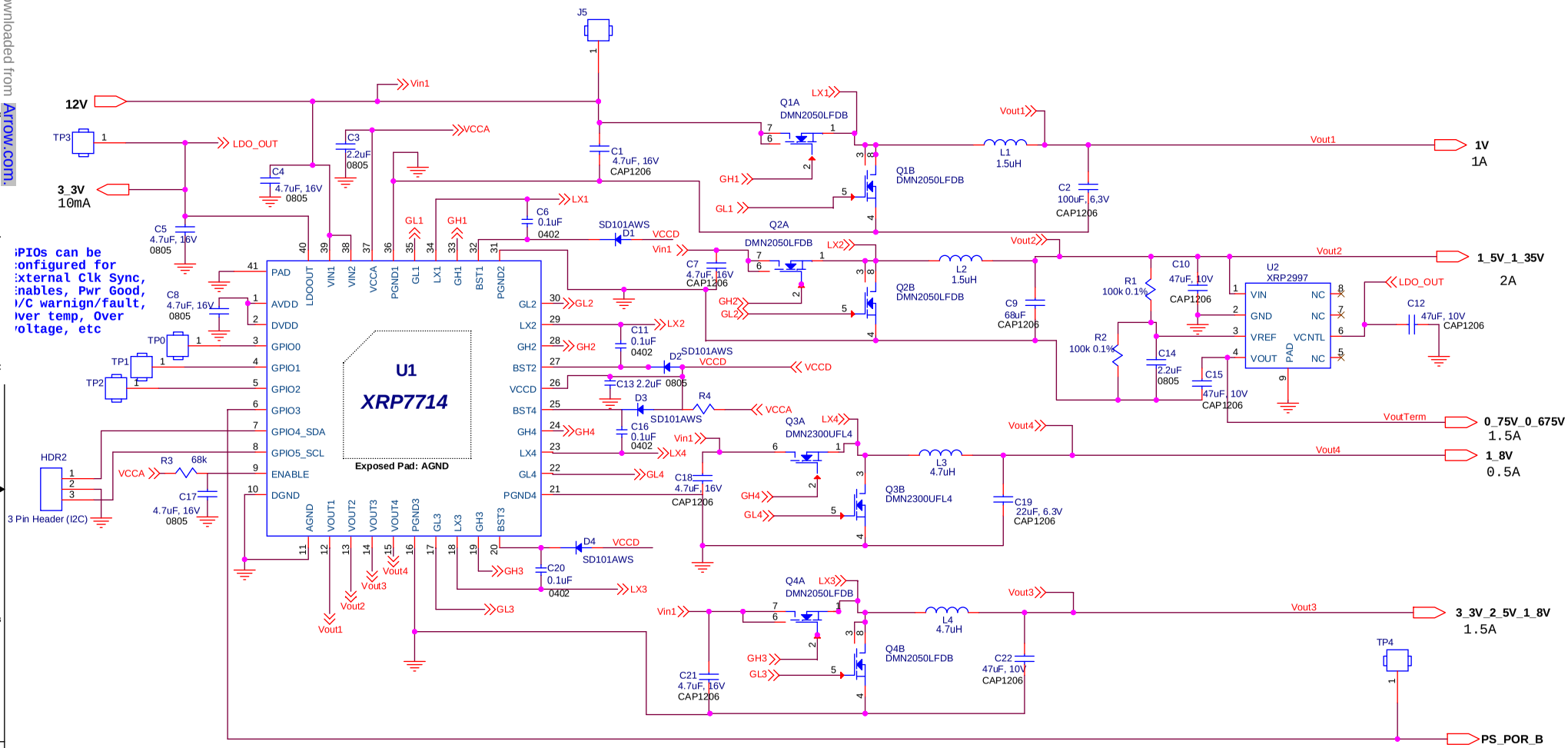


Fig. 17: Input Cap Ripple



Notes:
1) Meets all Zynq seq and dependency constraints
2) All higher value ceramics can be built out of multiples of 22uF to decrease cost.
3) All system requiremetns (eg Seq, O/C, O/V, O/T, enables, power good, etc) are configurable
4) Realtime readout of Vin, Vout, Iout, etc available via I2C
5) Output current can be programmed up to approx 3.5A/ch
6) Vout options programmable
7) PS_POR_B is correctly timed.

Title	Exar Xilinx Ind Enet V0.9 Version1	
Size B	Document Number	Rev 1.0
Date: Monday, June 13, 2016	Sheet 1 of 1	

BILL OF MATERIAL

Ref.	Qty	Manufacturer	Part Number	Size	Component
PCB	1	Exar	146-6730-01		XRP77114EVB_IND_V09_VER2
U1	1	Exar	XR7714ILB-F		
U2	1	Exar	XRP2997IDBTR-F	SOICD B08	2A, DDR I/II/II Bus Term. Regulator
Q1,Q2,Q4	3	Diodes, Inc.	DMN2050LFDB	U-DFN2020-6	Dual N-Ch. MOSFET, 20V,4.5A, 45mOhm
Q3	1	Diodes, Inc.	DMN2300UFL4	X2-DFN1310-6	Dual N-Ch. MOSFET, 20V,2.11A, 195mOhm
D1,D2,D3,D4	4	Diodes, Inc.	SD101AWS	SOD-323	SMT Barrier Diode, 60V, 15mA
L1,L2	2	Wurth Elektronik	7440620015	6.8X6.8MM	SMD Inductor 1.5uH, 4.3A, 14.0 mOhm
L3,L4	2	Wurth Elektronik	74408943047	4.8X4.8MM	SMD Inductor 4.7uH, 2.2A, 45.0 mOhm
C2,C9,C22	3	MURATA	GRM31CR60J107ME39L	1206	CERAMIC CAP. 100uF, 6.3V, X5R, 20%
C10, C12, C15, C19	4	MURATA	GRM31CR61A476KE15L	1206	CERAMIC CER, 47uF, 10V, X5R, 10%
C1,C7,C18,C21	4	MURATA	GRM31CR71H475KA12L	1206	CERAMIC CAP., 4.7uF, 50V, X7R, 10%
C4,C5,C8,C17	4	MURATA	GRM21BR71E475KA73L	0805	CERAMIC CAP., 4.7uF, 25V, X7R, 10%
C3,C13,C14	3	MURATA	GRM21BR71C225KA12L	0805	CERAMIC CAP., 2.2uF, 16V, X7R, 10%
C6,C11,C16,C20	4	MURATA	GRM155R71E104KE14D	0402	CERAMIC CAP., 0.1uF, 25V, X7R, 10%
R1,R2	2	PANASONIC	ERA-3AEB104V	0603	Resistor 100.0K Ohm, 0.1% 1/10W, SMD
R3	1	PANASONIC	ERJ-3EKF6802V	0603	Resistor 68.0K Ohm, 1/10W,1%,SMD
R4	1	PANASONIC	ERJ-3RQF1R0V	0603	Resistor 1.0 Ohm, 1/10W,1%,SMD
J7,J1,J8,J2,J4,J9,J10,J3,J16,J5,J6,J15	12	Vector Electronics	Vector Electronics	.042" Hole	PCB Pin
TP1,TP0,TP3,TP4,TP2	5	Wurth Electronics	61300111121	Test Point	Test Point
1-SCL,GND,SDA	1	Wurth Electronics	61300311121	Test Point	3 PIN HEADER

EVALUATION BOARD LAYOUT (FOR REFERENCE)

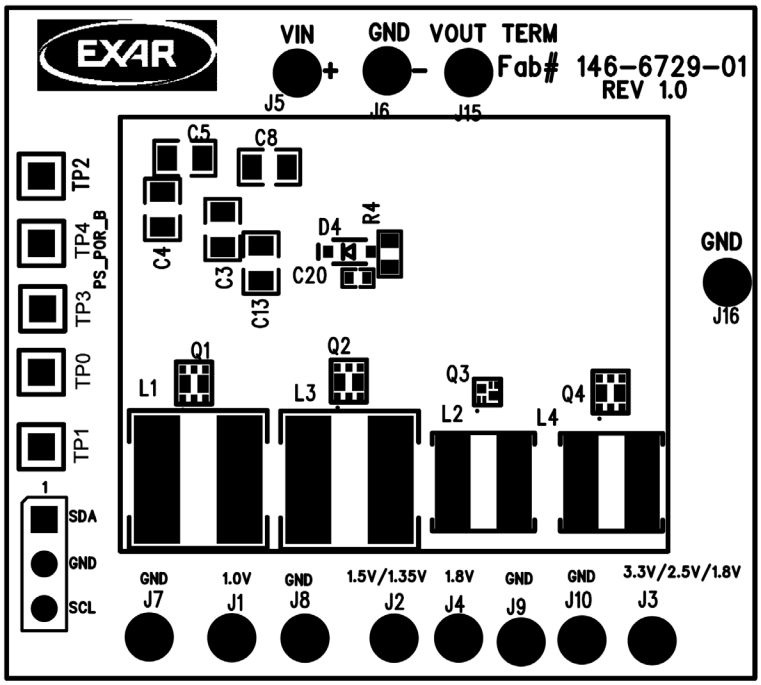


Figure 3: Component Placement Top Side

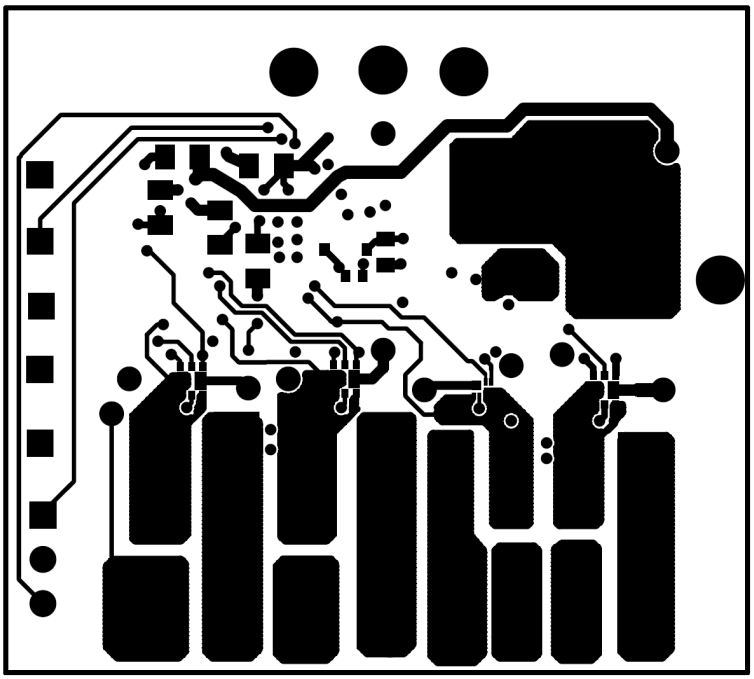


Figure 4: Top Layer

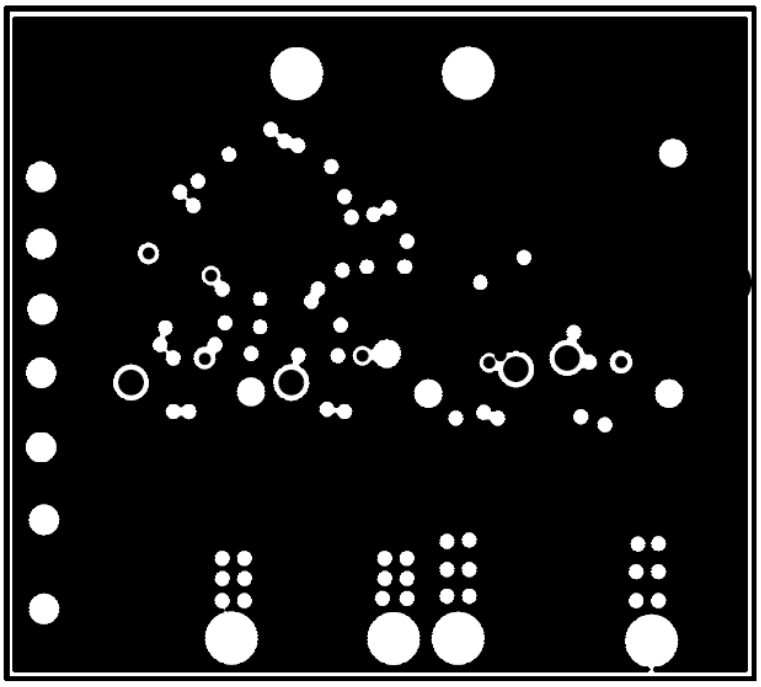


Figure 5: Ground Plane

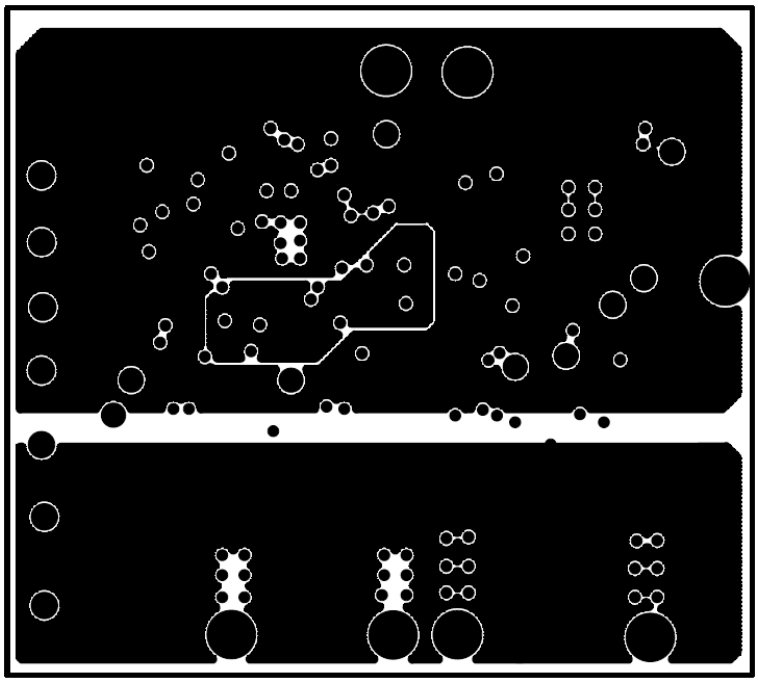


Figure 6: Mid-Layer

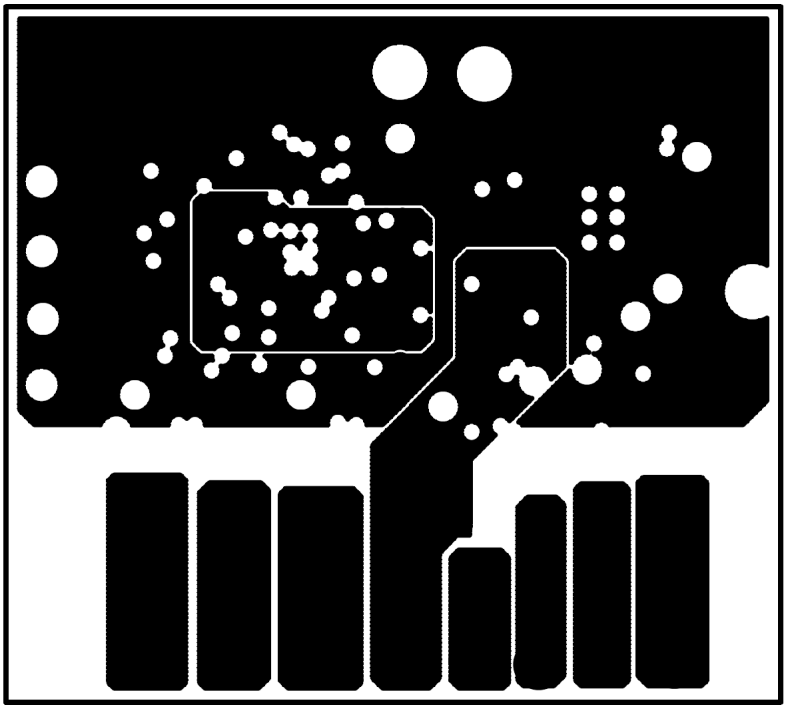


Figure 7: Mid-Layer 2

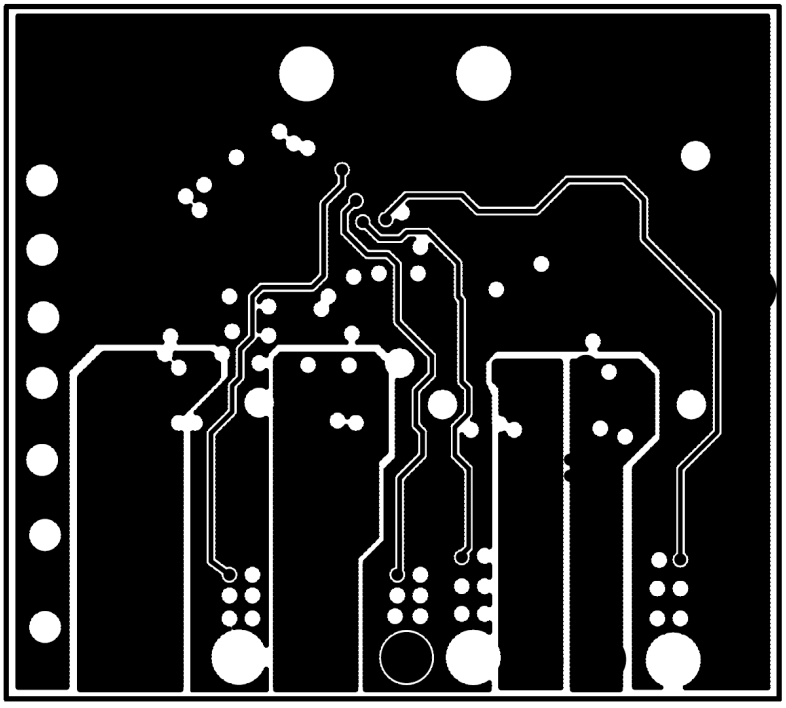


Figure 8: Mid-Layer 3

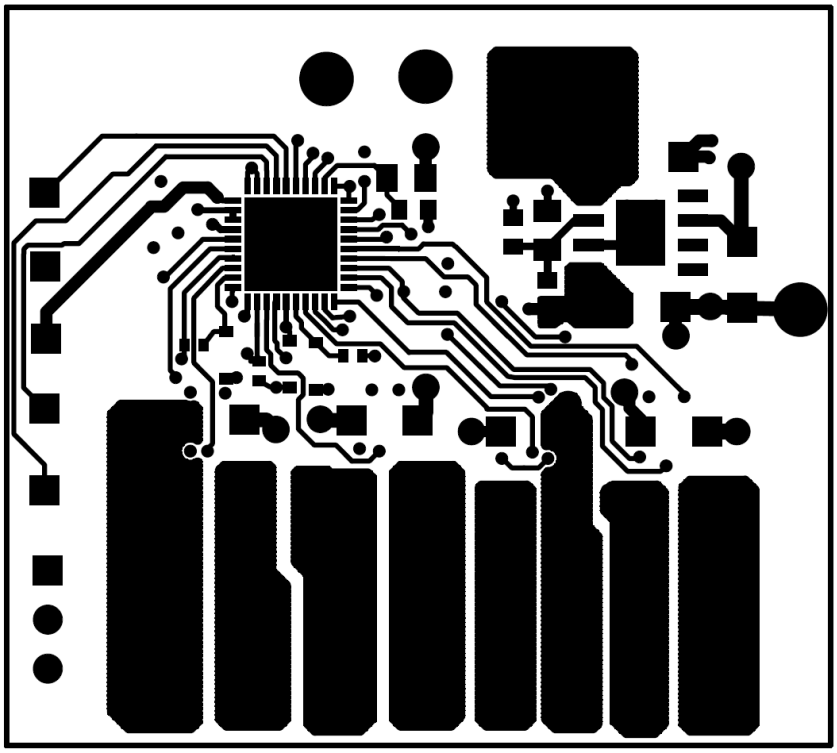


Figure 9: Bottom Layer

DOCUMENT REVISION HISTORY

Revision	Date	Description
1.0.0	06/22/2016	Initial release of document
1.0.1	07/19/2016	Added electrical characteristic curves

FOR FURTHER ASSISTANCE

Email: powertechsupport@exar.com
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Exar Technical Documentation: http://www.exar.com/TechDoc/default.aspx?

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NOTICE