

Evaluation board with STM32G081RB MCU

Introduction

The STM32G081B-EVAL Evaluation board is a high-end development platform for Arm[®] Cortex[®]-M0+ core-based STM32G081RBT6 microcontroller with USB Type-C[™] and Power Delivery controller interfaces (UCPD) compliant with USB Type-C r1.2 and USB PD specification r3.0, two I2Cs, two SPIs, five USARTs, one LP UART, one 12-bit ADC, two 12-bit DACs, two GP comparators, two LP timers, internal 32KB SRAM and 128KB Flash, CEC, SWD debugging support.

The full range of hardware features on the STM32G081B-EVAL Evaluation board includes the mother board, the legacy peripheral daughterboard and the USB Type-C and Power Delivery daughterboard, which help to evaluate all peripherals (USB Type-C connector with USB PD, motor control connector, RS232, RS485, Audio DAC, microphone ADC, TFT LCD, IrDA, IR LED, IR receiver, LDR, microSD[™] card, CEC on two HDMI connectors, smartcard slot, RF E2PROM and temperature sensor... etc.) and to develop applications. An ST-LINK/V2-1 is integrated on the board as embedded in-circuit debugger and programmer for the STM32 MCU

The daughterboard and extension connectors provide an easy way to connect a daughterboard or wrapping board for your specific application.

The USB Type-C and Power Delivery daughterboard features two independent USB-C ports controlled by STM32G0. USB-C port 1 is dual role power (DRP) and can provide up-to 45W of power. USB-C Port 2 is sink only. Both supports USB PD protocol and alternate mode functionality.

Figure 1. STM32G081B-EVAL board with legacy peripheral daughterboard

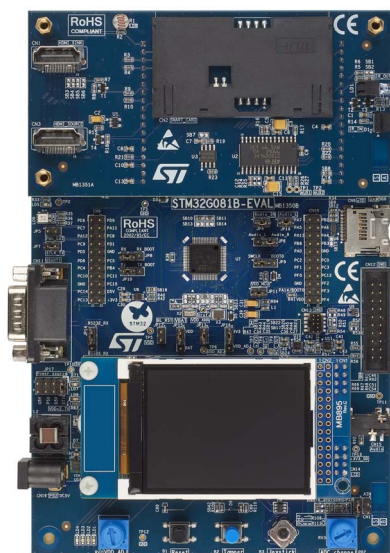


Figure 2. STM32G081B-EVAL board with UCPD daughterboard



Pictures are not contractual.

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1 Features

Mother board

- STM32G081RBT6 Arm^{®(a)} Cortex[®]-M0+ core-based microcontroller with 128 Kbytes of Flash memory and 32 Kbytes of RAM in LQFP64 package
- MCU voltage choice fixed 3.3 V or adjustable from 1.65 V to 3.6 V
- I²C compatible serial interface
- RTC with backup battery
- 8-Gbyte or more SPI interface microSD[™] card
- Potentiometer
- 4 color user LEDs and one LED as MCU low-power alarm
- Reset, Tamper and User buttons
- 4-direction control and selection joystick
- Board connectors:
 - 5 V power jack
 - RS-232 and RS485 communications
 - Stereo audio jack including analog microphone input
 - microSD[™] card
 - Extension I²C connector
 - Motor-control connector
- Board extension connectors:
 - Daughterboard connectors for legacy peripheral daughterboard or USB Type-C and Power Delivery daughterboard
 - Extension connectors for daughterboard or wire-wrap board
- Flexible power-supply options:
 - 5 V power jack
 - ST-LINK/V2-1 USB connector
 - Daughterboard
- On-board ST-LINK/V2-1 debugger/programmer with USB enumeration capability: mass storage, virtual COM port and debug port
- Comprehensive free software libraries and examples available with the STM32Cube package
- Support of a wide choice of Integrated Development Environments (IDEs) including IAR[™], Keil[®], GCC-based IDEs.



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Legacy peripheral daughterboard

- IrDA transceiver
- IR LED and IR receiver
- Light dependent resistor (LDR)
- Temperature Sensor
- Board connectors:
 - Two HDMI connectors with DDC and CEC
 - Smartcard slot

USB Type-C and Power Delivery daughterboard

- Multiplexer for USB3.1 Gen1 / DisplayPort™ input and Type-C port1 output
- Multiplexer for Type-C port2 input and DisplayPort output / USB2.0
- VCONN on Type-C port1
- USB PD on Type-C port1
- Board connectors:
 - Type-C port1 DRP (Dual Role Port)
 - Type-C port2 sink
 - DisplayPort input
 - DisplayPort output
 - USB 3.1 Gen1 Type-B receptacle
 - USB2.0 Type-A receptacle
 - 19 V power jack for USB PD

2 Product marking

Evaluation tools marked as “ES” or “E” are not yet qualified and are therefore not ready to be used as reference design or in production. Any consequences arising from such usage will not be at STMicroelectronics’ charge. In no event will STMicroelectronics be liable for any customer usage of these engineering sample tools as reference designs or in production.

‘E’ or ‘ES’ marking examples of location:

- on the targeted STM32 that is soldered on the board (for illustration of STM32 marking, refer to the section *Package information* in the STM32 datasheet at www.st.com).
- next to the evaluation tool ordering part number, that is stuck or silkscreen printed on the board

3 System requirements

- Windows® OS (7, 8 and 10), Linux® 64-bit or macOS®(a)
- USB Type-A to Micro-B cable

4 Development toolchains

- Keil® MDK-ARM^(b)
- IAR™ EWARM^(b)
- GCC-based IDEs

5 Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board MCU, is preloaded in the STM32 Flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from the www.st.com web page.

a. macOS® is a trademark of Apple Inc., registered in the U.S. and other countries.

b. On Windows only

6 Ordering information

To order the STM32G081B-EVAL Evaluation board, refer to [Table 1](#).

Table 1. Ordering information

Order code	Target STM32
STM32G081B-EVAL	STM32G081RB

7 Delivery recommendations

Some verifications are needed before using the board for the first time, to make sure that no damage occurred during shipment and that no components are unplugged or lost.

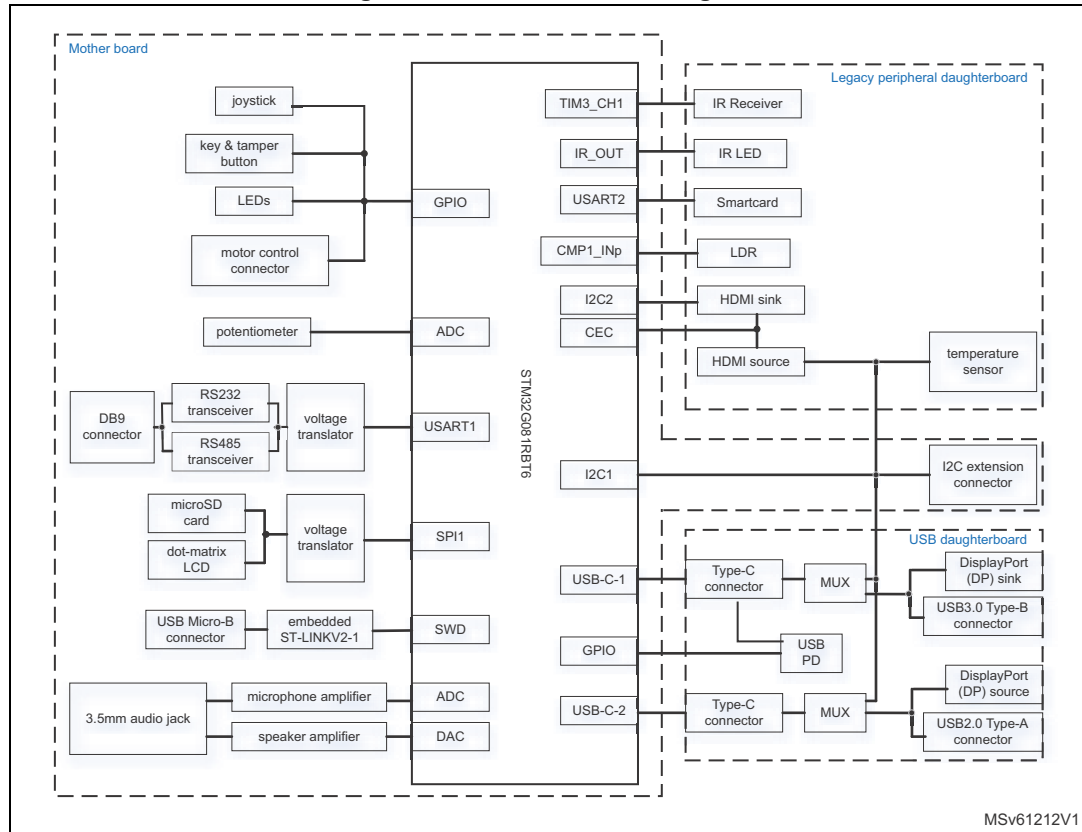
When the board is extracted from its plastic bag, check that no component remains in the bag. The main component to verify is microSD card which may have been ejected from the connector CN8 (right side of the board).

Caution: There is an explosion risk if the battery is replaced by an incorrect one. Make sure to dispose of used batteries according to the instructions.

8 Hardware layout and configuration

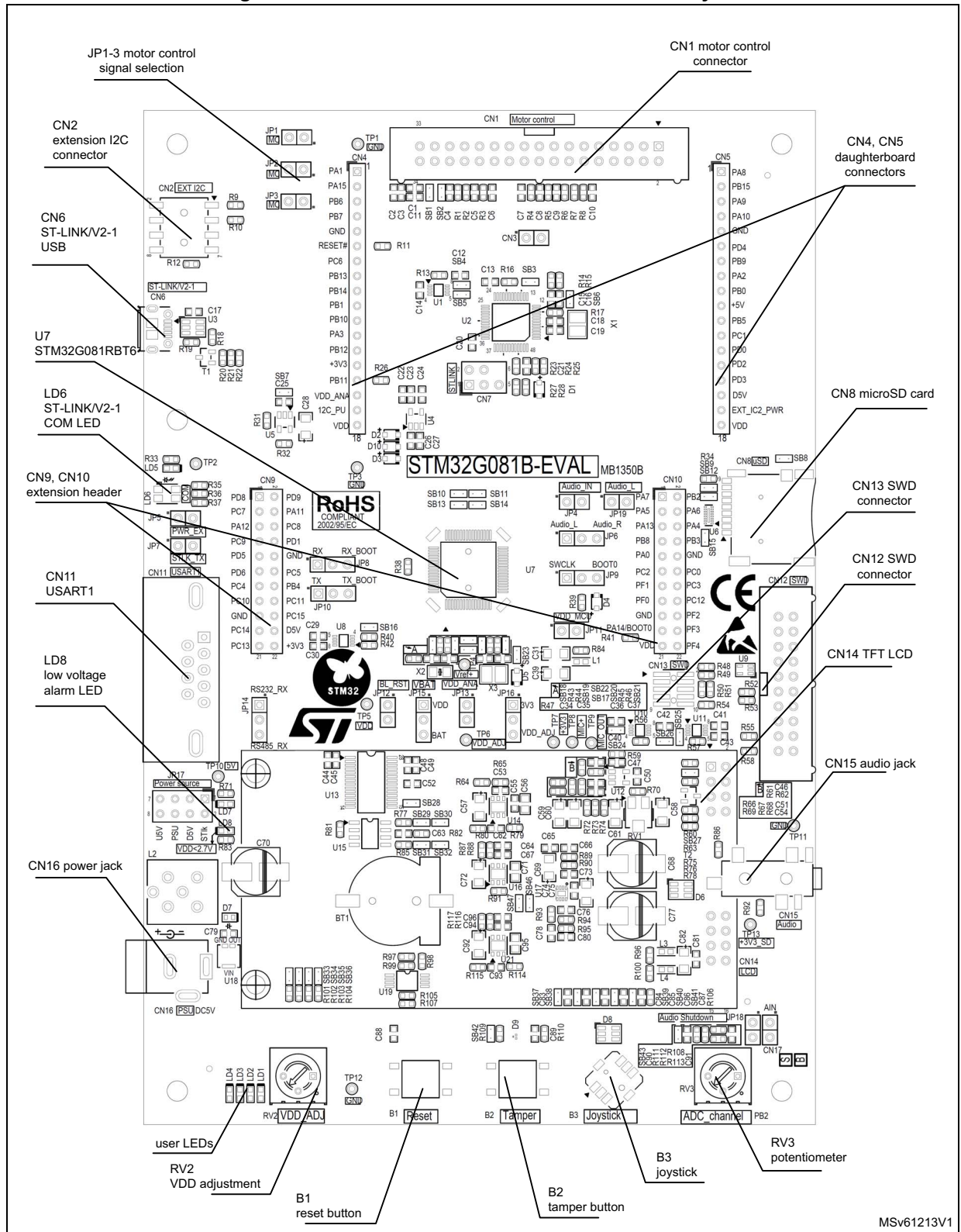
The STM32G081B-EVAL Evaluation board is designed around the STM32G081RBT6 (64-pin LQFP package). The hardware block diagram *Figure 3* illustrates the connection between STM32G081RBT6 and peripherals (motor control connector, RS232, RS485, Audio DAC, microphone ADC, TFT LCD, CAN, IrDA, IR LED, IR receiver, LDR, MicroSD card, CEC on two HDMI connectors, Smartcard slot, Temperature sensor... etc.) and *Figure 4* help users to locate these features on the Evaluation board.

Figure 3. Hardware block diagram



MSv61212V1

Figure 4. STM32G081B-EVAL Evaluation board layout



MSv61213V1

Figure 5. Legacy peripheral daughterboard

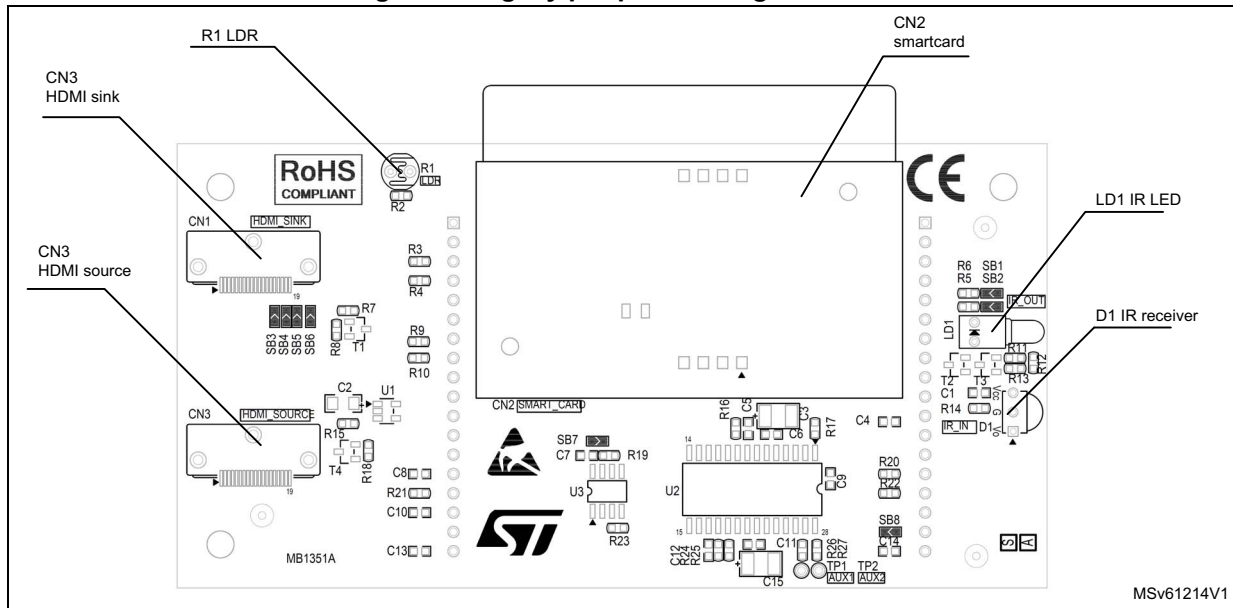
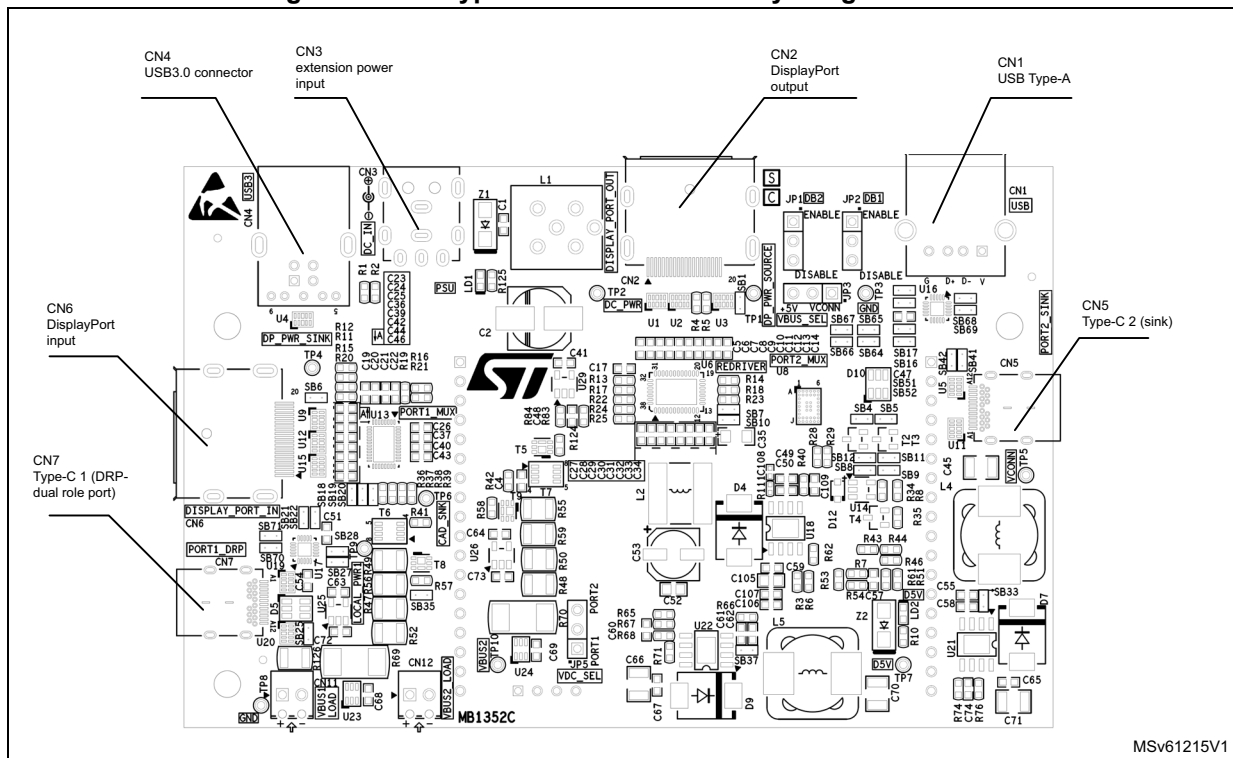


Figure 6. USB Type-C and Power Delivery daughterboard



8.1 Embedded ST-LINK/V2-1

The ST-LINK/V2-1 programming and debugging tool is integrated on the STM32G081B-EVAL Evaluation board. Compared to ST-LINK/V2 the changes are listed below.

The new features supported on ST-LINK/V2-1 are:

- USB software enumeration
- Virtual COM port interface on USB
- Mass storage interface on USB
- USB power management request for more than 100 mA power on USB

This feature is no longer supported on ST-LINK/V2-1:

- SWIM interface

For all general information concerning debugging and programming features common between V2 and V2-1 refer to *ST-LINK/V2 in-circuit debugger/programmer for STM8 and STM32 User manual (UM1075)* in the www.st.com website.

Note: It is possible to power the board via CN6 (Embedded ST-LINK/V2-1 USB connector) even if an external tool is connected to CN12 or CN13 (External SWD connector).

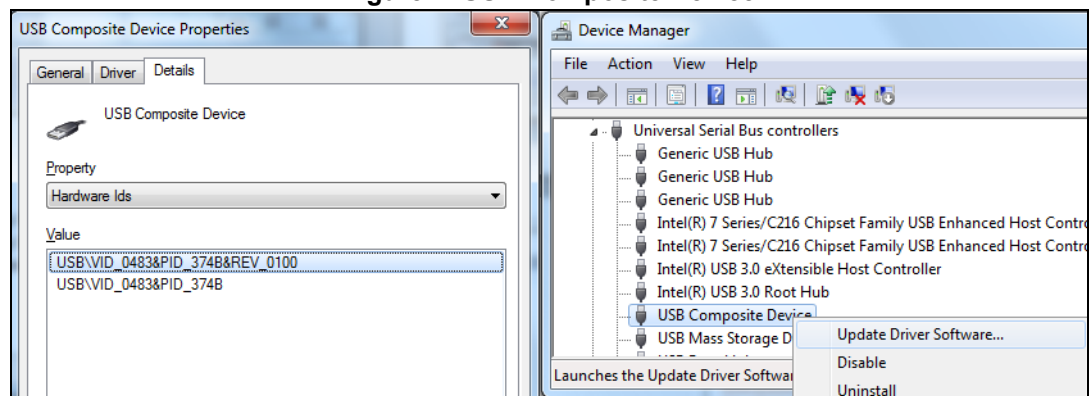
8.1.1 Drivers

The ST-LINK/V2-1 requires a dedicated USB driver, which can be found on www.st.com for Windows PC (7, 8 or 10).

In case the STM32G081B-EVAL Evaluation board is connected to the PC before the driver is installed, some STM32G081B-EVAL interfaces may be declared as “Unknown” in the PC device manager. In this case, the user must install the driver files, and update the driver of the connected device from the device manager.

Note: Prefer using the “USB Composite Device” handle for a full recovery.

Figure 7. USB Composite Device



8.1.2 ST-LINK/V2-1 firmware upgrade

The ST-LINK/V2-1 embeds a firmware upgrade mechanism for in-situ upgrade through the USB port. As the firmware may evolve during the lifetime of the ST-LINK/V2-1 product (for example new functionality, bug fixes, support for new microcontroller families), it is recommended to visit the www.st.com website before starting to use the STM32G081B-EVAL board and periodically, to stay up-to-date with the latest firmware version.

8.2 Power supply

The STM32G081B-EVAL Evaluation mother board is designed to be powered by 5 V DC power supply and is protected by PolyZen from wrong power plug-in event. It is possible to configure the mother board to use any of the following four sources for the power supply:

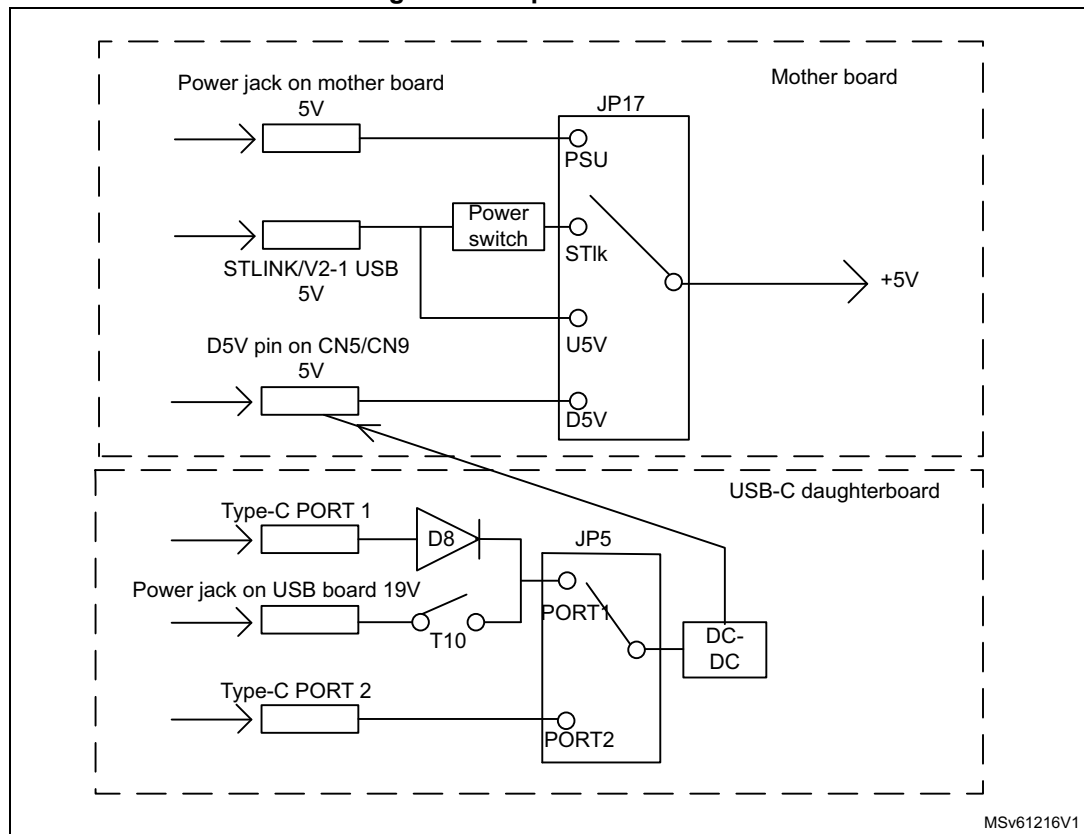
- 5 V DC power adapter connected to CN16, the power Jack on the board (Power Supply Unit on silk screen of JP17 (PSU)). The external power supply is not provided with the board.
- 5 V DC power with 500 mA limitation from CN6, the USB Micro-B connector of STLINK/V2-1 (USB 5 V power source on silkscreen of JP17 (STIk)). If the USB enumeration succeeds, the ST-LINK U5V power is enabled, by asserting the PWR_EN pin. This pin is connected to a power switch, which powers the board. This power switch features also a current limitation to protect the PC in case of short-circuit on the board. If overcurrent (more than 500 mA) happens on the board, the LED LD5 lights up.
- 5 V DC power from CN6 directly, the USB Micro-B connector of STLINK/V2-1 (USB 5 V power source on silkscreen of JP17 (U5V)).
- 5 V DC power from CN5 or CN9, the extension connector for daughterboard power source (D5V) on silkscreen of JP19).

The UCPD daughterboard uses its own 19V power adapter to support USB PD, in this case the mother board uses D5V from the UCPD daughterboard to supply all circuits on STM32G081B-EVAL Evaluation board. D5V of the UCPD daughterboard has three sources as below:

- 19 V DC power adapter connected to CN3 on the UCPD daughterboard
- Power from Type-C Port1 CN7 on the UCPD daughterboard
- Power from Type-C port2 CN5 on the UCPD daughterboard

19 V DC power adapter and Type-C Port1 sources are automatically selected by circuit (D8 and T10 on the UCPD daughterboard). Refer to Table15 for detail.

Figure 8. 5 V power structure



The STM32G081B-EVAL Evaluation board can be powered from the ST-LINK/V2-1 USB connector CN6 with a PC, but only the ST-LINK/V2-1 circuit has the power before USB enumeration, because the host PC only provides 100 mA to the boards at that time. During the USB enumeration, the STM32G081B-EVAL board requires 300 mA power from the host PC. If the host is able to provide the required power, the enumeration succeeds, the power transistor U5 is switched ON, the red LED LD7 is turned ON, and thus the STM32G081B-EVAL board is powered and can consume maximum 300 mA current. If the host PC is not able to provide the requested power, the enumeration fails. Therefore the STM32 part including the extension board is not powered. As a consequence the red LED LD7 remains turned OFF. In this case it is mandatory to use an external power supply to supply extra power.

E5V (from PSU) or D5V can be used as external power supply in case current consumption of the STM32G081B-EVAL board exceeds the allowed current on USB. In this condition it is still possible to use USB for communication, for programming or debugging only, but it is mandatory to power the board first using E5V or D5V, and then connecting the USB cable to the PC. Proceeding this way ensures that the enumeration succeeds thanks to the external power source.

The following power sequence procedure must be respected:

1. Connect jumper JP17 for PSU or D5V side
2. Check that JP5 is removed
3. Connect the external power source to PSU or D5V (daughterboard mounted)
4. Check red LED LD7 is turned ON
5. Connect the PC to USB connector CN6

If this order is not respected, the board may be powered by VBUS first then E5V or D5V, and the following risks may be encountered:

1. If more than 300 mA current is needed by the board, the PC may be damaged or current can be limited by PC. As a consequence the board is not powered correctly.
2. 300 mA is requested at enumeration (since JP5 must be OFF), so there is risk that request is rejected and enumeration does not succeed if PC can't provide such current. Consequently the board is not powered (LED LD7 remains OFF).

In case the STM32G081B-EVAL board is powered by an USB charger through CN6, there is no USB enumeration needed. User can set JP17 to U5V to allow the board to be powered anyway from CN6.

The power source is selected by setting the related jumpers JP17, JP15 and JP16 as described in table 2.

Table 2. Power source related Jumpers

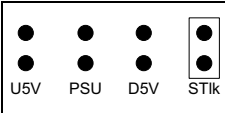
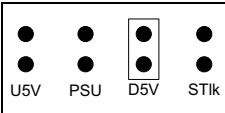
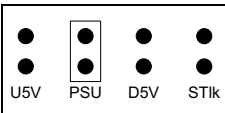
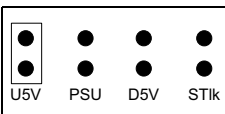
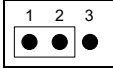
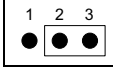
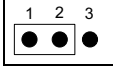
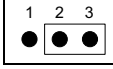
Jumper	Description
JP17	JP17 is used to select one of the four possible power supply resources. Only for power supply from USB (CN6) of ST-LINK/V2-1 to STM32G081B-EVAL, JP17 is set as shown on the right: 
	Only for power supply from the daughterboard connectors (CN5 or CN9) to STM32G081B-EVAL, JP17 is set as shown on the right: (default Setting) 
	Only for power supply jack (CN16) to the STM32G081B-EVAL, JP17 is set as shown on the right: 
	Only for power supply from USB (CN6) to STM32G081B-EVAL without current limited, JP17 is set as shown on the right: 

Table 2. Power source related Jumpers (continued)

Jumper	Description
JP15	The Vbat pin of STM32G081RBT6 is connected to VDD when JP15 is set as shown on the right (default setting): 
	The Vbat pin of STM32G081RBT6 is connected to 3V battery when JP15 is set as shown on the right: 
JP16	The VDD pin of STM32G081RBT6 is connected to 3.3V when JP16 is set as shown on the right (default setting), when the UCPD daughterboard is used, this setting is mandatory: 
	The VDD pin of STM32G081RBT6 is connected to VDD_ADJ when JP16 is set as shown on the right: 

Note: The VDD_MCU Idd measurement can be done by current meter which mounted on JP11 when it is open. But JP11 is not allowed to be opened without current meter; otherwise STM32G081RBT6 would be damaged due to lacking of power supply on its power pins.

Note: LD8 is lit when VDD < 2.7 V and in this case IOs and some Analog IPs of STM32G081RBT6 work with degraded performances.

Note: The UCPD daughterboard works with VDD=3.3V, so it is mandatory to close JP16 pin1 and pin2.

The LED LD7 is lit when the STM32G081B-EVAL Evaluation board is powered by the 5V correctly.

Table 3 shows the low voltage limitations that might apply depending on the characteristics of some peripheral components. Components might work incorrectly when the power level is lower than the limitation.

Table 3. Low voltage limitation

Board	peripheral	component	IO name	Low voltage limitation
Mother board	Audio amplifier	U17	Audio input	2.2V
Mother board	Microphone amplifier	U12	Audio output	2.7V
Legacy daughterboard	Smartcard	CN2	USART1	2.7V

8.3 Clock references

Two clock sources are available on STM32G081B-EVAL Evaluation board for STM32G081RBT6 and RTC embedded.

- X2, 32KHz Crystal for embedded RTC
- X3, 8MHz Crystal for the STM32G081RBT6 microcontroller, it can be disconnected by removing R45 and R46 when internal RC clock is used

Table 4. 32 KHz crystal X2 related solder bridges

Jumper	Description
SB18	PC14 is connected to 32KHz crystal when SB18 is open (default setting).
	PC14 is connected to extension connector CN9 when SB18 is closed. In such case R43 must be removed to avoid disturbance due to the 32Khz quartz.
SB19	PC15 is connected to 32KHz crystal when SB19 is open (default setting).
	PC15 is connected to extension connector CN9 when SB19 is closed. In such case R44 must be removed to avoid disturbance due to the 32Khz quartz.

Table 5. 8 MHz crystal X3 related solder bridges

Jumper	Description
SB20	PF0 is connected to 8MHz crystal when SB20 is open (default setting).
	PF0 is connected to extension connector CN10 when SB20 is closed. In such case R45 must be removed to avoid disturbance due to the 8Mhz quartz.
SB21	PF1 is connected to 8MHz crystal when SB21 is open (default setting).
	PF1 is connected to extension connector CN10 when SB21 is closed. In such case R46 must be removed to avoid disturbance due to the 8Mhz quartz.

8.4 Reset source

The general reset of the STM32G081B-EVAL Evaluation board is active low and the reset sources include:

- Reset button B1
- Debugging Tools from SWD connector CN12 and CN13
- Daughterboard from CN4
- Embedded ST-LINK/V2-1
- RS232 connector CN11 for ISP.

Note: The jumper JP12 to be closed for RESET handled by pin8 of RS232 connector CN11 (CTS signal), please refer to [Section 8.6.2](#) for detail.

8.5 Boot Option

The STM32G081B-EVAL Evaluation board is able to boot from:

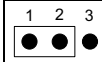
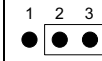
- Embedded User Flash
- System memory with boot loader for ISP
- Embedded SRAM for debugging

The boot option is configured by closing JP9 pin2-3 and setting one jumper cap on CN10 among pin 17, pin 19 and pin 21 and one option bit (see [Table 6](#) and [Table 7](#)).

Table 6. Boot related jumper

Jumper configuration	Bit25 in USER OPTION BYTES	Boot from
CN10 pin 19 and pin 17 closed by jumper	X	STM32G081B-EVAL boot from User Flash (default setting)
CN10 pin 19 and pin 21 closed by jumper	0	STM32G081B-EVAL boot from Embedded SRAM
CN10 pin 19 and pin 21 closed by jumper	1	STM32G081B-EVAL boot from System Memory

Table 7. Boot0 related jumpers

Jumper	Description
JP9	PA14-BOOT0 is used as SWCLK when JP9 is set as shown on the right (default setting). 
	The Bootloader_BOOT0 is managed by pin 6 of connector CN11 (RS232 DSR signal) and it is connected to PA14-BOOT0 when JP9 is set as shown on the right. This configuration is used for boot loader application only. 

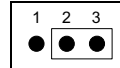
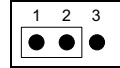
8.6 Peripherals on mother board

8.6.1 Audio

The STM32G081B-EVAL Evaluation board supports stereo audio playback and microphone recording by an external headset connected on audio jack CN15. Audio play is connected to DAC output of STM32G081RBT6 through an audio amplifier and microphone on headset is connected to ADC input of STM32G081RBT6 through a microphone amplifier. Audio amplifier can be enabled or disabled by setting of JP18 and mono/stereo playback can be chosen by setting of JP6, refer to [Table 8](#) for detail.

Table 8. Audio related jumpers

Jumper	Description
JP18	Speaker amplifier U17 is enabled when JP18 is closed (default setting)
	Speaker amplifier U17 is disabled when JP18 is open
JP19	PA4 is connected to VIN1 of Audio amplifier when JP19 is closed (default setting)
	PA4 is disconnected to VIN1 of Audio amplifier when JP19 is open
JP6	Mono playback is enabled when JP6 is set as shown on the right (default setting):
	Stereo playback is enabled when JP6 is set as shown on the right:



Audio amplifier operates correctly when VDD > 2.2 V and microphone amplifier operates correctly when VDD > 2.7 V.

8.6.2 RS232 and RS485

Communication through RS232 (with Hardware flow control CTS and RTS) and RS485 is supported by D-type 9-pins RS232/RS485 connector CN11, which is connected to USART1 of STM32G081RBT6 on STM32G081B-EVAL Evaluation board. The signal Bootloader_RESET (shared with CTS signal) and Bootloader_BOOT0 (shared with DSR signal) are added on RS232 connector CN11 for ISP support.

By default, PC4 and PC5 are connected as TX and RX signals. PA9 and PA10 are also can be connected as these two signals for bootloader which is NOT supported on PC4 and PC5 by setting of jumpers in [Table 9](#).

Table 9. RS232 and RS485 related jumpers

Jumper	Description
JP14	RS232_RX is connected to RS232 transceiver and RS232 communication is enabled when JP14 is set as shown on the right (default setting):
	RS485_RX is connected to RS485 transceiver and RS485 communication is enabled when JP14 is set as shown on the right:
JP10	PC4 is connected as TX signal without bootloader being supported when JP10 is set as shown on the right (Default setting):
	PA9 is connected as TX signal with bootloader being supported when JP10 is set as shown on the right (CN1 motor control connector is needed to be open in this case):

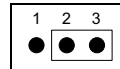
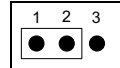
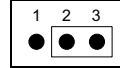
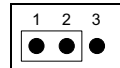
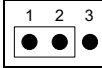
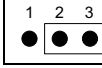


Table 9. RS232 and RS485 related jumpers (continued)

JP8	PC5 is connected as RX signal without bootloader being supported when JP8 is set as shown on the right (default setting):	
	PA10 is connected as RX signal with bootloader being supported when JP8 is set as shown on the right (in this case, CN1 motor control connector must be open):	

The RS485 communication is supported by RS485 transceiver ST3485EBDR which connected to pin4 and pin9 of D-type 9-pins connector CN11 (share same connector with USART1).

Table 10. RS485 related solder bridges

Jumper	Description
SB29,SB31	The external failsafe biasing are enabled when solder bridges SB29 and SB31 was closed Default Setting: Not fitted
SB32	The bus termination is enabled when solder bridge SB32 is closed. Default Setting: Not fitted
SB30	The AC termination is disabled when solder bridge SB30 is closed for high baud rate communication. Default Setting: Not fitted

8.6.3 microSD card

The 8-GB (or more) microSD card connected to SPI1 port (shared with color LCD) of STM32G081RBT6 is available on the board. microSD card detection is managed by standard IO port PC9 and it must be set with internal pull-up.

8.6.4 Analog Input

The two-pin header CN17 and 10K ohm potentiometer RV3 was connected to PB2 of STM32G081RBT6 as analog input. A low pass filter can be implemented by replacing of R111 and C90 with right value of resistor and capacitor as requested by end user's application.

8.6.5 External I2C Connector

The I2C1 bus of the STM32G081RBT6 is connected to CN2 on the STM32G081B-EVAL. The I2C functional daughterboard can be mounted on the CN2 connector and accessed by the microcontroller through the I2C1 bus, it shares same I2C1 bus with Temperature sensor U3 and DDC on HDMI_Source connector CN3 on legacy peripheral daughterboard.

The pull up voltage level of I2C1 bus is automatically decided by the daughterboard (the legacy peripheral daughterboard or the UCPD daughterboard) on CN4 and CN5. If there is

no daughterboard on these connector, pin17 must be closed to pin18 on both CN4 and CN5 by jumpers. Thus I2C pull up voltage and reset pull up voltage on CN2 would be the voltage of VDD.

8.6.6 Motor Control

The STM32G081B-EVAL Evaluation board supports both asynchronous and synchronous three-phase brushless motor control via a 34-pins connector CN1, which provides all required control and feedback signals to and from motor power-driving board.

Available signals on this connector includes emergency stop, motor speed, 3 phase motor current, bus voltage, power heatsink coming from the motor driving board and 6 channels of PWM control signal going to the motor driving circuit.

Daughterboard on CN4 and CN5 must be removed and some jumpers set for motor control application:

- Close JP1, JP2 and JP3.
- Open JP4 and JP6.
- Open pin2-3 of JP8 and JP10.

8.6.7 Display and Input devices

The 2.4" color TFT LCD connected to SPI1 port of STM32G081RBT6 and 4 general purpose color LED's (LD 1,2,3,4) are available as display device. The 4-direction joystick (B3) with selection key which connected to PA0 and supports wakeup feature. Tamper button (B2) are also available as input devices.

Table 11. LCD modules

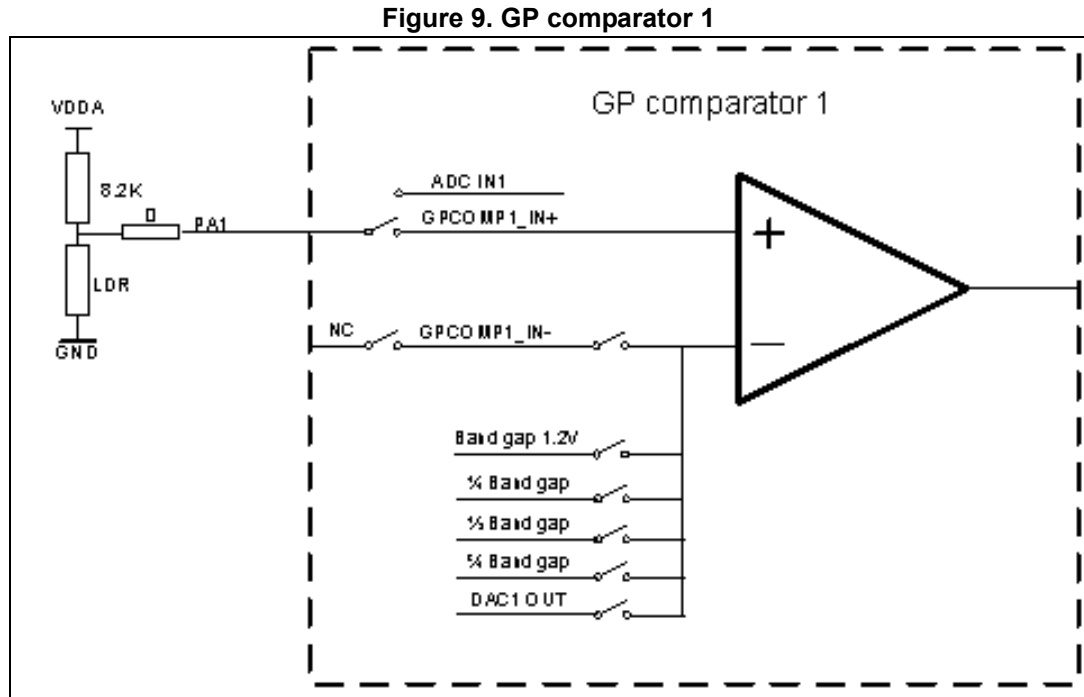
2.4" TFT LCD connector CN14					
Pin	Description	Pin connection	Pin	Description	Pin connection
1	CS	PB8	9	VDD	3.3V
2	SCL	PB3	10	VCI	3.3V
3	SDI	PA7	11	GND	GND
4	RS	-	12	GND	GND
5	WR	-	13	BL_VDD	5V
6	RD	-	14	BL_Control	5V
7	SDO	PB4	15	BL_GND	GND
8	RESET	RESET#	16	BL_GND	GND

Note: The bi-directional voltage translator is implemented on SPI MOSI signal between STM32G081RBT6 and LCD to support 3-wires serial interface of LCD panel only supports 3-wire SPI port. The direction of this voltage translator is controlled by IO PC12 (the IO PA7 is working as MOSI when PC12 is high or as MISO when PC12 is LOW).

8.7 Peripherals on legacy peripheral daughterboard

8.7.1 LDR (Light dependent resistor)

The VDD is divided by resistor bridge of LDR VT9ON1 and 8.2 K resistor and connected to PA1 (COM1_IN+/ADC IN1) as shown [Figure 9](#) on STM32G081B-EVAL Evaluation board.



It's possible to compare LDR output with 1/4 band gap, 1/2 band gap, 3/4 band gap, band gap and DAC1 OUT and to connect LDR output to ADC IN1 for AD conversion.

8.7.2 Temperature sensor

A temperature sensor STLM75M2F is connected to the I2C1 bus of the STM32G081RBT6, and shares same I2C1 bus with EXT I2C connector (on mother board) and DDC on HDMI_Source connector CN3 (on legacy board).

I2C address of temperature sensor is 0b100100(A0), A0 can be 0 or 1 depends on the setting of SB7.

Table 12. Temperature sensor related solder bridge

Solder Bridge	Description
SB7	I2C address A0 is 0 when SB7 is open. (Default setting)
	I2C address A0 is 1 when SB7 is closed.

Note: The temperature result measured from STLM75M2F would be a little higher than the ambient temperature due to the power dissipation of components on the board.

8.7.3 Smartcard

STMicroelectronics smartcard interface chip ST8024L is used on STM32G081B-EVAL Evaluation board for asynchronous 1.8V, 3V and 5V smartcards. It performs all supply protection and control functions based on the connections with STM32G081RBT6 listed in [Table 13](#).

Table 13. Connection between ST8024L and STM32G081RBT6

Signals of ST8024L	Description	Connect to STM32G081RBT6
5V/3V	Smartcard power supply selection pin	PB15
I/OUC	MCU data I/O line	PA2
XTAL1	Crystal or external clock input	PD4
OFF	Detect card presence, Interrupt to MCU	PB12
RSTIN	Card reset input from MCU	PA15
CMDVCC	Start activation sequence input (Active Low)	PB0
1.8V	1.8 V Vcc operation selection. Logic high selects 1.8 V operation and overrides any setting on the 5V/3V pin.	PA3

Smartcard operates correctly when $VDD > 2.7\text{ V}$.

8.7.4 HDMI CEC

Two HDMI connectors CN1 and CN3 are available on STM32G081B-EVAL legacy peripheral daughterboard.

- The connector CN1 is HDMI sink connector with
 - DDC connected to I2C2 of STM32G081RBT6
 - HPD controlled by IO PD2 through transistor T1
 - CEC connected to PB10 through transistor T4
- The connector CN3 is HDMI source connector with
 - DDC connected to I2C1 of STM32G081RBT6 and shared with Temperature sensor and EXT I2C connector
 - HPD controlled by IO PD3
 - CEC connected to PB10 through transistor T4
 - HDMI 5V powered by power switch U1

The signals TDMS D+[0..2], TDMS_CLK+, TDMS D-[0..2], TDMS_CLK- on these two HDMI connectors are connected together.

The CEC injector mode can be enabled by some PCB reworks for debugging purpose only:

- Remove resistors R3, R4, R7, R9, R10, R15 and R22.
- Close solder bridges SB3, SB4, SB5 and SB6.

Note: The I/O PD2 must be set in open-drain output mode by firmware when working as an HPD signal control on the HDMI sink connector CN1.

8.7.5 IR LED and IR receiver

The IR receiver TSOP34836 is connected to PC6 of STM32G081RBT6 and a current around 100mA on IR LED is driven by PB9 through transistors T2 and T3 on the board.

Note: IR LED may be driven by PB9 directly with 20mA current when SB1 is closed and SB2 is open.

8.8 USB Type-C and Power Delivery daughterboard

The UCPD daughterboard is a development platform composed of STM32G081B-EVAL Evaluation board. This daughterboard is used for demonstrating the functionalities of the USB Type-C and USB Power Delivery (USB PD) technologies, facilitating the users to develop their solutions. Refer to [Figure 3](#) for daughterboard structure.

Note: The USB PD reference design on the UCPD daughterboard is used to demonstrate the capability of STM32G081RBT6. This USB PD circuit may not pass all USB PD certifications.

Note: The UCPD daughterboard works with VDD=3.3V. So JP16 pin1-2 must be closed on mother board.

Note: The UCPD daughterboard conflicts with legacy peripheral daughterboard and Motor control on STM32G081B-EVAL Evaluation board.

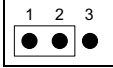
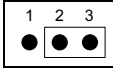
8.8.1 USB Type-C receptacles

Two USB Type-C certified receptacles CN7 and CN5 are present on the UCPD daughterboard, representing respectively the PORT 1 and PORT 2. PORT 1 can be used as DRP (Dual-Role Port), which is eligible to supply another platform plugged by a USB Type-C cable when they are configured as Provider or, otherwise, to be supplied in case of Consumer configuration. PORT 2 can only be used as SINK.

Video signals on display port input connector (CN6) and data signals on USB3.1 Gen1 Type-B connector (CN4) are multiplexed on Type-C PORT 1 thanks to a crosspoint switch IC TUSB546-DCI. These signals on CN6 or on CN4 have to be generated by an external computer or notebook to evaluate the alternate mode (AM) capability of the USB PD technology. The crosspoint switch can be configured through I2C bus, and its I2C address is 0b1000100. The cable which is plugged into CN4 can be detected by PA15.

Same as Type-C PORT1, video signals on display port output connector (CN2) are connected to Type-C PORT 2 through another crosspoint switch IC CBTL08GP053 and DisplayPort Linear Redriver IC SN65DP141. I2C address of CBTL08GP053 is 0b0110000 and SN65DP141's default I2C address is 0b0000000. A Type-A receptacle's (CN1) D+ and D- signals are also connected to Type-C PORT 2 directly. Its VBUS can be set by JP3 in [Table 14](#).

Table 14. VBUS related jumpers

Jumper	Description
JP3	VBUS is connected to VCONN when JP3 is set as shown on the right (default setting). 
	VBUS is connected to D5V through mother board when JP3 is set as shown on the right. 

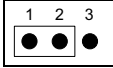
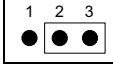
Note: Some week USB charger can not provide power to board immediately from port1 Type-C receptacle when external 19V power adapter is plugged off. If board lose power and reset during such use case, close JP6 may help to solve this problem. JP6 is open by default.

8.8.2 Power Delivery and local power management

The UCPD daughterboard has its own external power jack (CN3, 19V/4A input) to support power delivery function and to provide up to 15V/3A on Type-C port1 (CN7).

The STM32G081B-EVAL Evaluation board can be powered by D5V from the UCPD daughterboard as shown in [Figure 5](#). D5V on the UCPD daughterboard can be generated by three resources, 19V from external power jack, VBUS on Port 1 and VBUS on Port 2. A circuit is implemented on the UCPD daughterboard to automatically select external 19V power supply or VBUS on Port1, because external 19V and VBUS on Port1 are the two power sources for Port1 to D5V. A jumper JP5 is used to select D5V resources in [Table 15](#).

Table 15. Local power related jumpers

Jumper	Description
JP5	D5V from the UCPD daughterboard is generated from external 19V or VBUS on Port1 when JP5 is set as shown on the right (default setting). 
	D5V from the UCPD daughterboard is generated from VBUS on Port2 when JP5 is set as shown on the right. 

8.8.3 VBUS management and discharge mechanism

Type-C port1 (CN7) can be used as DRP (Dual-Role Port), its VBUS can be managed for supplying other platforms as Provider, or to be supplied as Consumer. Two MOSFETs T6 and T7 are set in back-to-back configuration to protect and isolate the VBUS supplying path on both directions.

If the CN7 acts as Provider, the VBUS is on the supply path by mean of the discrete load switch (T6 and T7) driven by the STM32G081RBT6 (GPIO, PD3). For the Consumer case, the same VBUS path is managed by PD3 of STM32G081RBT6 enabling the discrete load switch.

All power profiles are listed in [Table 16](#).

Table 16. VBUS Power Delivery profiles

CN7 role	Solder bridges setting	Power level	Source control signal	Voltage control signal
Provider	SB2, SB3, SB23, SB26 ON SB13, SB14, SB15 OFF	PWM Mode: PWM voltage-3A	PD3 High	PC1-PWM signal
	SB13, SB14, SB15 ON	GPIO Mode: 5V / 9V / 15V- 3A	PD3 High	5V: PC1(VSOURCE-9V) and PA1(VSOURCE-15V) tristate
	SB2, SB3, SB23, SB26 OFF			9V: PC1(VSOURCE-9V) low 15V: PA1 (VSOURCE-15V) low
Consumer	-	Decided by Provider which is connected through Type-C cable	PD3 low	-

Moreover, the VBUS path on PORT1 presents a discharge mechanism implemented by the MOSFET T8 and an RC filter and controlled by PB13, and the VBUS path on PORT2 presents a discharge mechanism implemented by the MOSFET T9 and an RC filter and controlled by PB14.

8.8.4 VBUS voltage-sensing and current-sense stage

Each Type-C port is equipped by a voltage-sensing and a current-sensing stage which are matched with the voltage sensing carried by the STM32G081RBT6 ADC peripherals. Refer to [Table 17](#) for detail. They are able to monitor the right power level applied on the port VBUS.

Table 17. Voltage-sensing and current-sensing ADC

PORT	VSENSE ADC		ISENSE ADC	
PORT 1	PB1	ADC_IN9	PB10	ADC_IN11
PORT 2	PA3	ADC_IN3	PB12	ADC_IN16

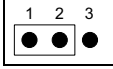
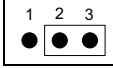
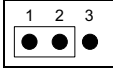
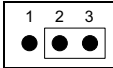
8.8.5 CC management

Dead battery, VCONN output and fast role swap functions are supported on CC signal of Type-C PORT 1.

- Dead battery enable
Dead battery function is supported by OVP chip U17 and U16. And this function also

embedded in STM32G081RBT6. When OVP part U17 is bypassed, dead battery function in STM32G081RBT6 can be enable or disable through enable signals by set JP2 (CC1) or JP1 (CC2). Refer to [Table 18](#) for detail.

Table 18. Dead battery related jumpers

Jumper	Description
JP1	Embed dead battery function is enable when JP1 is set as shown on the right (default setting). 
	Embed dead battery function is disable when JP1 is set as shown on the right. 
JP2	Embed dead battery function is enable when JP2 is set as shown on the right (default setting). 
	Embed dead battery function is disable when JP2 is set as shown on the right. 

2. VCONN output control

When the full-featured cable is connected to PORT 1, the VCONN is directly managed by the STM32G081RBT6 by mean of the PD4 or PB9 and the load switches STMPS2161 U10 and U14.

3. Fast role swap

Type-C PORT 1 can be configure to action fast role swap managed by STM32G081RBT6 through PA2 (CC1) and PB0 (CC2).

9 Connectors

9.1 Connectors on mother board

9.1.1 Motor control connector CN1

Figure 10. Motor Control connector CN1 (top view)

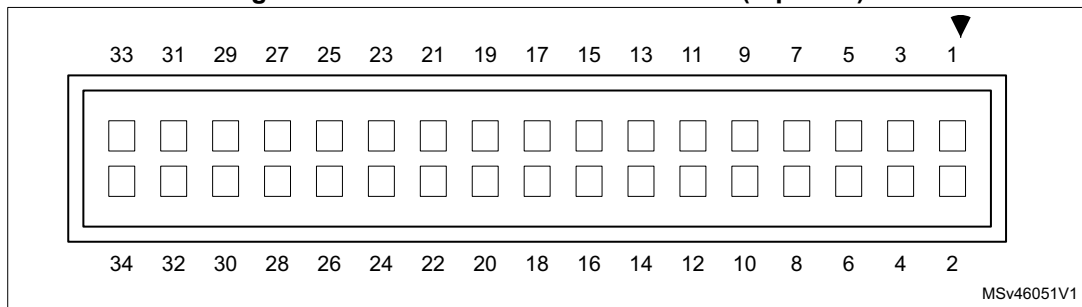


Table 19. Motor control connector CN1

Description	Pin of STM32G081RBT6	Pin number of CN1	Pin number of CN1	Pin of STM32G081RBT6	Description
EmergencySTOP	PB12	1	2	-	GND
PWM-UH	PA8	3	4	-	GND
PWM-UL	PD2	5	6	-	GND
PWM-VH	PA9	7	8	-	GND
PWM-VL	PD3	9	10	-	GND
PWM-WH	PA10	11	12	-	GND
PWM-WL	PD4	13	14	PA1	BUS VOLTAGE
PHASE A CURRENT	PA2	15	16		GND
PHASE B CURRENT	PA6	17	18		GND
PHASE C CURRENT	PB10	19	20	-	GND
NTC BYPASS RELAY	PB9	21	22	-	GND
DISSIPATIVE BRAKE PWM	PB15	23	24	-	GND
+5V power	-	25	26	PA3	Heatsink temperature
PFC SYNC2	PD0	27	28		3.3V power
PFC SYNC1	PC1				
PFC PWM	PB1	29	30	-	GND

Table 19. Motor control connector CN1 (continued)

Description	Pin of STM32G081RBT6	Pin number of CN1	Pin number of CN1	Pin of STM32G081RBT6	Description
Encoder A	PC6	31	32	-	GND
Encoder B	PB5	33	34	PB0	Encoder Index

9.1.2 External I2C connector CN2

Figure 11. I2C EXT connector CN2 (front view)

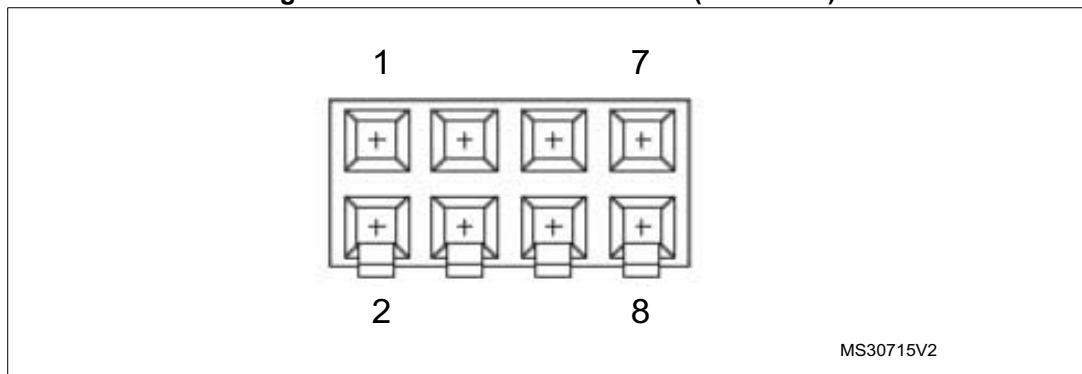


Table 20. RF E2PROM connector CN2

Pin number	Description	Pin number	Description
1	I2C1_SDA (PB7)	5	PWR (Define by daughterboard on CN5, or VDD when short CN5 pin17 and pin18)
2	NC	6	NC
3	I2C1_SCL (PB6)	7	GND
4	EX_RESET(PC0)	8	NC

9.1.3 Daughterboard connector CN4 and CN5

Two 18-pins male headers CN4 and CN5 are designed to connect with the legacy peripheral daughterboard or the UCPD daughterboard to STM32G081B-EVAL Evaluation mother board. All GPIOs are available on CN4, CN5 and extension connector CN9, CN10.

Each pin on CN4 and CN5 can be used by a daughterboard after disconnecting it from the corresponding function block on STM32G081B-EVAL Evaluation board. Please refer to [Table 21](#) and [Table 22](#) for detail.

Table 21. Daughterboard connector CN4

Pin	Signal	Mother board Function	Legacy daughterboard Function (CN5)	UCPD daughterboard Function (CN9)	How to disconnect with function block on mother board
1	PA1	MC_BusVoltage	LDR_OUT	V_CTL2	Keep JP1 open
2	PA15	-	Smartcard RST	USB3_DET	-
3	PB6	I2C1_SCL	I2C1_SCL	I2C1_SCL	-
4	PB7	I2C1_SDA	I2C1_SDA	I2C1_SDA	-
5	GND	-	-	-	-
6	RESET#	-	-	-	-
7	PC6	MC_ENA	IR_IN	Display port HPD_SOURCE	-
8	PB13	-	I2C2_SCL	DISCHARGE 1	-
9	PB14	-	I2C2_SDA	DISCHARGE 2	-
10	PB1	MC_PFCpwm	-	VSENSE 1	-
11	PB10	MC_CurrentC	HDMI_CEC	ISENSE 1	-
12	PA3	MC_heatsinkTemp	Smartcard 1V8	VSENSE 2	Keep JP2 open
13	PB12	MC_EmergencySTOP	Smartcard OFF	ISENSE 2	Keep JP3 open
14	+3V3	-	-	-	-
15	PB11	Daughterboard detection	Daughterboard detection	Daughterboard detection & USB PD output VSENSE	-
16	VDD_ANA	-	-	-	-
17	I2C_PU	I2C pull up power of CN2	-	-	-
18	VDD	-	-	-	-

Table 22. Daughterboard connector CN5

Pin	Signal	Mother board Function	Legacy daughterboard Function (CN4)	UCPD daughterboard Function (CN8)	How to disconnect with function block on mother board
1	PA8	MC_UH	-	PORT1_CC1	-
2	PB15	MC_Dissipative brake	Smartcard 3/5 V	PORT1_CC2	-
3	PA9	MC_VH/USART1_TX_BOOT	-	PORT1_DB1	Keep JP10 pin2-3 open
4	PA10	MC_WH/USART1_RX_BOOT	-	PORT1_DB2	Keep JP8 pin2-3 open
5	GND	-	-	-	-
6	PD4	MC_WL	Smartcard CK	VCONN_EN1	-

Table 22. Daughterboard connector CN5 (continued)

Pin	Signal	Mother board Function	Legacy daughterboard Function (CN4)	UCPD daughterboard Function (CN8)	How to disconnect with function block on mother board
7	PB9	MC_NTC	IR_OUT	VCONN_EN2	-
8	PA2	MC_Current A	Smartcard TX	FRS_TX1	-
9	PB0	MC_ENINDEX	Smartcard CMDVCC	FRS_TX2	-
10	+5V	-	-	-	-
11	PB5	MC_ENB	Temp Sensor INT	Display port HPD_IN	-
12	PC1	MC_PFCsync1	-	V_CTL1	-
13	PD0	MC_PFCsync2	-	PORT2_CC1	-
14	PD2	MC_UL	HDMI_HPDP_SINK	PORT2_CC2	-
15	PD3	MC_VL	HDMI_HPDP_SOURCE	SOURCE_EN	-
16	D5V	-	-	-	-
17	EXT I2C PWR	Power of CN2	5V	VDD	-
18	VDD	-	-	-	-

9.1.4 ST-LINK/V2-1 USB Micro-B connector CN6

The USB Micro-B connector CN6 is used to connect embedded ST-LINK/V2-1 to PC for debugging of board.

Figure 12. USB Micro-B connector CN6 (front view)

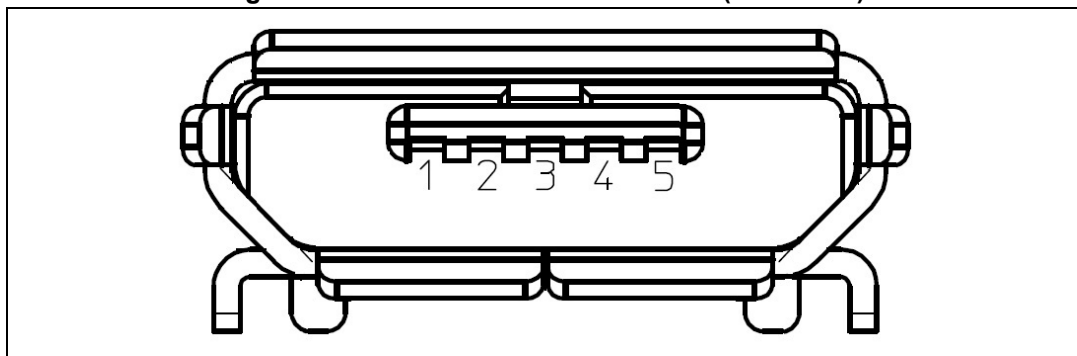


Table 23. USB Micro-B connector CN6

Pin number	Description	Pin number	Description
1	VBUS (power)	4	ID
2	DM	5	GND
3	DP	-	-

9.1.5 ST-LINK/V2-1 programming connector CN7

The connector CN7 is used only for embedded ST-LINK/V2-1 programming during board manufacturing. It is not populated by default and not for end user.

9.1.6 microSD connector CN8

Figure 13. microSD connector CN8 (front view)

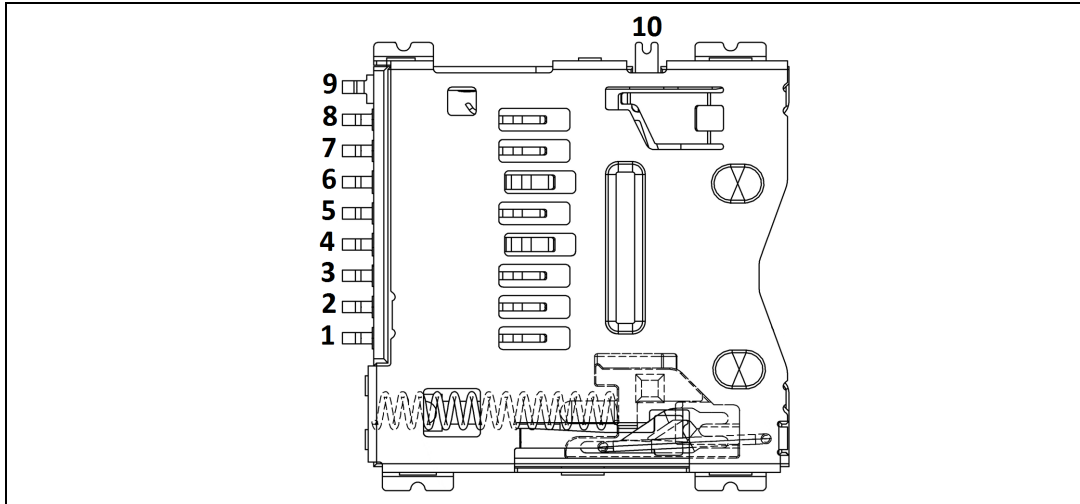


Table 24. microSD connector CN9

Pin number	Description	Pin number	Description
1	NC	5	MicroSDcard_CLK (PB3)
2	MicroSDcard_CS (PD1)	6	Vss/GND
3	MicroSDcard_DIN(PA7)	7	MicroSDcard_DOUT(PB4)
4	+3V3	8	NC
-	-	10	MicroSDcard_detect (PC9)

9.1.7 Extension connector CN9 and CN10

Two 22-pin male headers CN9 and CN10 can be used to connect with daughterboard or standard wrapping board to STM32G081B-EVAL Evaluation board. The standard width between CN9 pin1 and CN10 pin1 is 2700mils (68.58mm). The standard was implemented on the majority of Evaluation boards.

Each pin on CN9 and CN10 can be used by a daughterboard after disconnecting it from the corresponding function block on STM32G081B-EVAL Evaluation board. Please refer to [Table 25](#) and [Table 26](#) for detail.

Table 25. Extension connector CN9

Pin	Description	Alternative Function	How to disconnect with function block on STM32G081B-EVAL board
1	PD8	LED3	Close SB11, Open SB14, SB34
3	PC7	GPIO_JOY_RIGHT	Open SB40
5	PA12	USART_1_RTS	Open SB16
7	PC9	GPIO_SD_DETECT	Open SB8
9	PD5	LED1	Open SB36
11	PD6	LED2	Open SB35
13	PC4	USART_1_TX	Open JP10 pin1-2
15	PC10	VCP_USART_3_TX	Open SB5
17	GND	-	-
19	PC14	OSC32_IN	Remove R43, Close SB18
21	PC13	Button (Tamp, Wakeup2)	Open SB42
2	PD9	LED4	Close SB10, Open SB13, SB33
4	PA11	USART_1_CTS	Open SB28
6	PC8	GPIO_JOY_LEFT	Open SB39
8	PD1	GPIO_SD_CS	Open SB9
10	GND	-	-
12	PC5	USART_1_RX	Open JP8 pin1-2
14	PB4	LCD/SD1_MISO	Open SB12
16	PC11	VCP_USART_3_RX	Open JP7
18	PC15	OSC32_OUT	Remove R44, Close SB19
20	D5V	-	-
22	+3V3	-	-

Table 26. Extension connector CN10

Pin	Description	Alternative Function	How to disconnect with function block on STM32G081B-EVAL board
1	PA7	LCD/SD1_MOSI	Open SB24
3	PA5	AUDIO_OUT_DAC1_OUT2	Open JP6 pin2-3
5	PA13	SWDIO	Open SB4, Remove R48
7	PB8	GPIO_LCD_CS	Open SB27
9	PA0	JOY_SEL_TAMP_WKUP1	Open SB38
11	PC2	GPIO_JOY_UP	Open SB41
13	PF1	OSC_OUT	Remove R46, Close SB21
15	PF0	OSC_IN	Remove R45, Close SB20

Table 26. Extension connector CN10 (continued)

Pin	Description	Alternative Function	How to disconnect with function block on STM32G081B-EVAL board
17	GND	-	-
19	PA14-BOOT	SWCLK BOOT0	Open JP9 pin1-2
21	VDD	-	-
2	PB2	POTENTIOMETER_ADC_IN10	Open SB43
4	PA6	AUDIO_IN_ADC_IN6/ MC_CurrentB	Open JP4, Keep CN1 disconnected
6	PA4	AUDIO_OUT_DAC1_OUT1	Open JP6 pin1-2, JP19
8	PB3	LCD/SD1_SCK	Open SB25
10	GND	-	-
12	PC0	GPIO_EXT_RST	Remove R12, Keep CN2 disconnected
14	PC3	GPIO_JOY_DOWN	Open SB37
16	PC12	GPIO_LCD/SD_MOSI_DIR	Open SB26
18	PF2-NRST	RESET	Open SB23
20	PF3-VBAT	VBAT	Open JP15
22	PF4-VREF+	VREF+	Open SB17, SB22

9.1.8 RS232 and RS485 connector CN11

Figure 14. RS232 and RS485 connector CN11 (front view)

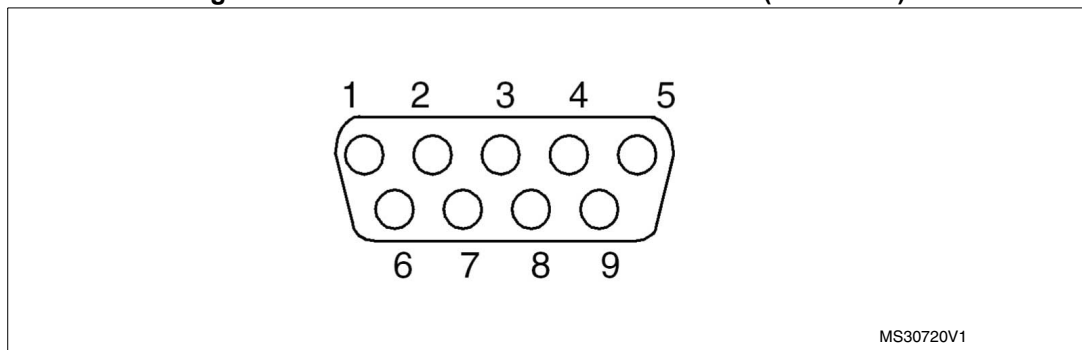


Table 27. RS232 & RS485 connector CN11

Pin number	Description	Pin number	Description
1	NC	6	Bootloader_BOOT0
2	RS232_RX (PC5 or PA10)	7	RS232_RTS(PA12)
3	RS232_TX (PC4 or PA9)	8	RS232_CTS(PA11) / Bootloader_RESET

Table 27. RS232 & RS485 connector CN11 (continued)

Pin number	Description	Pin number	Description
4	RS485_A	9	RS485_B
5	GND	-	-

9.1.9 Standard SWD connector CN12

Figure 15. Standard SWD debugging connector CN12 (top view)

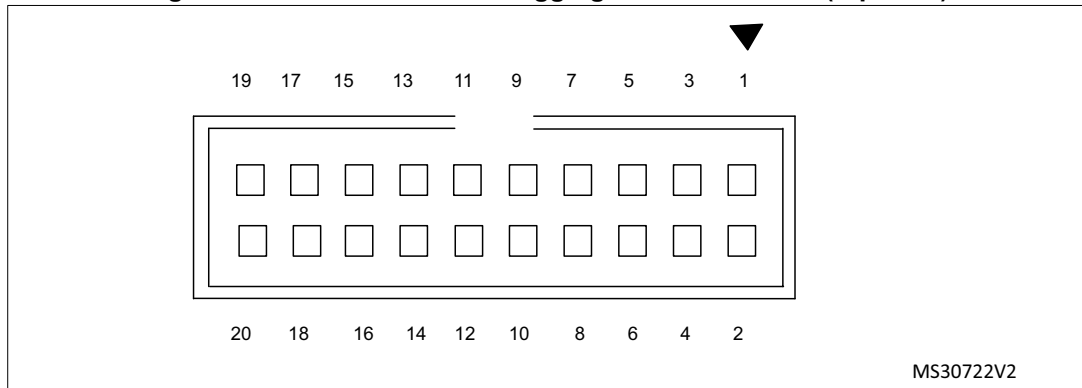


Table 28. Standard SWD debugging connector CN12

Pin number	Description	Pin number	Description
1	VDD	2	VDD
3	NC	4	GND
5	NC	6	GND
7	SWDAT(PA13)	8	GND
9	SWCLK(PA14)	10	GND
11	10K pull-down	12	GND
13	NC	14	GND
15	RESET#	16	GND
17	10K pull-down	18	GND
19	10K pull-down	20	GND

9.1.10 High density SWD connector CN13

Figure 16. High density SWD debugging connector CN13 (top view)

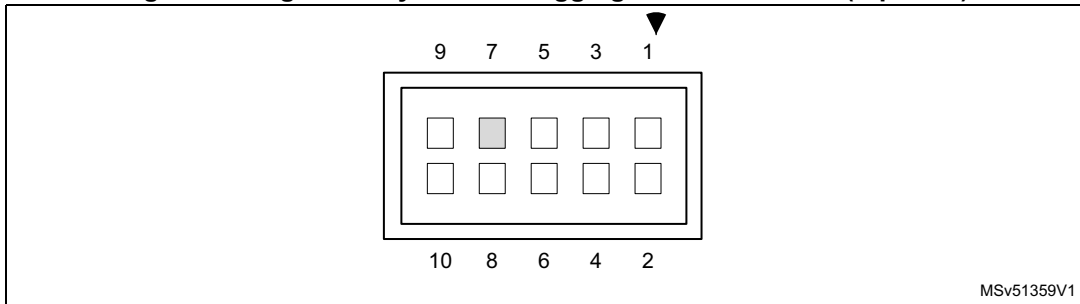


Table 29. High density SWD debugging connector CN13

Pin number	Description	Pin number	Description
1	VDD	2	SWDAT(PA13)
3	GND	4	SWCLK(PA14)
5	GND	6	NC
7	KEY	8	NC
9	GND	10	RESET#

9.1.11 TFT LCD connector CN14

A TFT color LCD board is mounted on CN14. Please refer to Section 1.6.7 for detail.

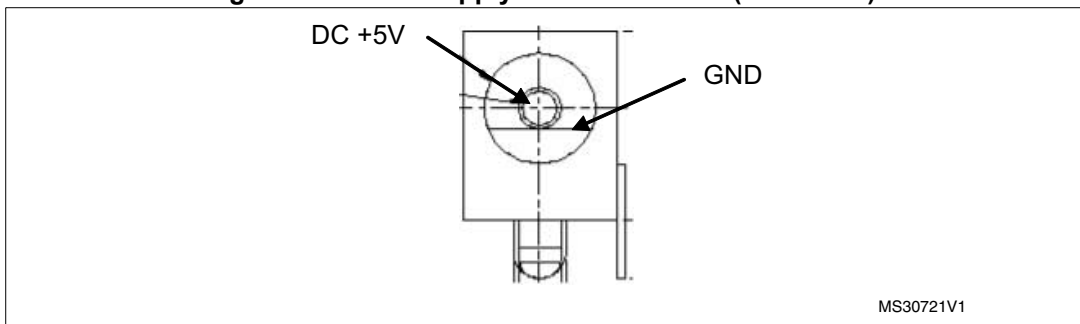
9.1.12 Audio jack CN15

A 3.5mm Stereo audio jack CN15 connected to audio DAC and ADC is available on STM32G081B-EVAL board.

9.1.13 5 V Power connector CN16

STM32G081B-EVAL Evaluation mother board can be powered from a DC 5V power supply via the external power supply jack (CN16) shown in *Figure 17*. The central pin of CN16 must be positive.

Figure 17. Power-supply connector CN16 (front view)



9.1.14 Analog input connector CN17

Figure 18. Analog input-output connector CN17 (top view)

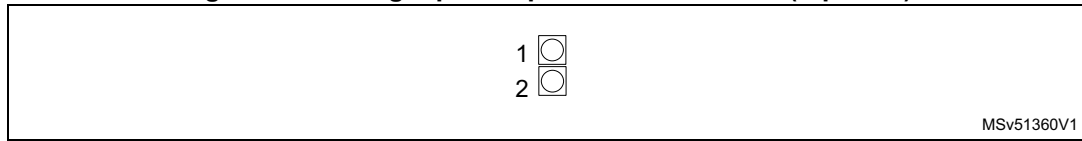


Table 30. Analog input-output connector CN17

Pin number	Description	Pin number	Description
1	Analog input-output PB2	2	GND

9.2 Connectors on legacy peripheral daughterboard

9.2.1 HDMI sink connector CN1

Figure 19. HDMI sink connector CN1 (front view)

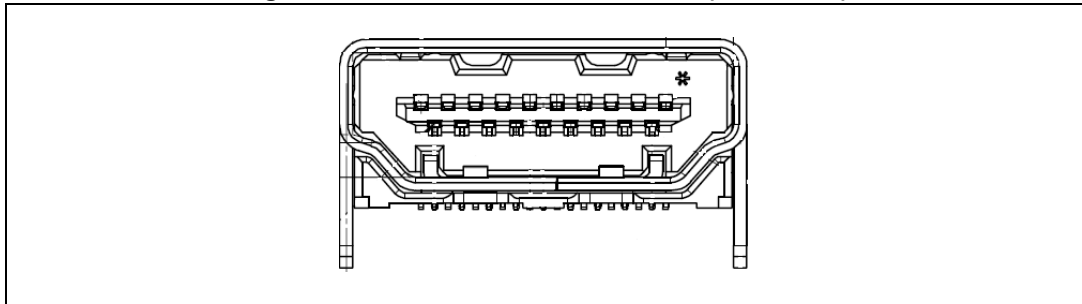


Table 31. HDMI sink connector CN1

Pin number	Description	Pin number	Description
1,3,4,6,7,9,10,12	TMDS differential signal pair connected to CN3	16	I2C2_SDA (PB14)
13	CEC (PB10)	2,5,8,11,17	GND
14	NC	18	HDMI_5V_Sink
15	I2C2_SCL (PB13)	19	HPD (PD2 through transistor)

9.2.2 Smartcard connector CN2

Figure 20. Smartcard connector CN2 (top view)

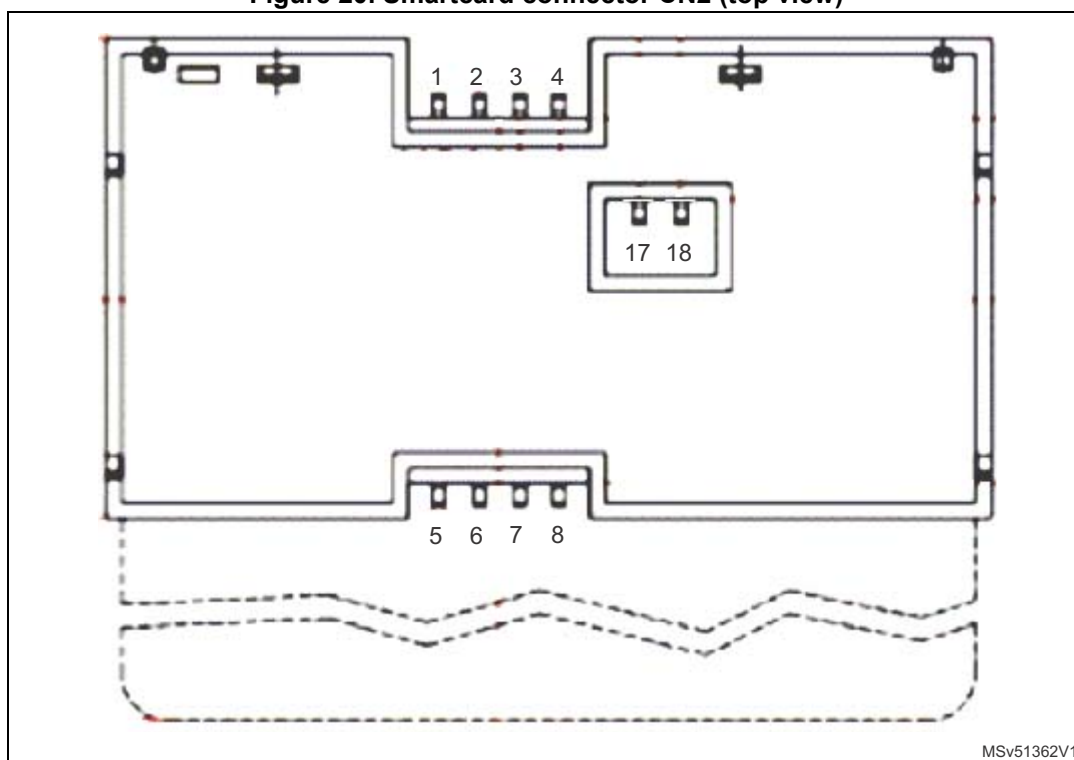


Table 32. Smartcard connector CN2

Pin number	Description	Pin number	Description
1	VCC	5	GND
2	RST	6	NC
3	CLK	7	I/O
4	NC	8	NC
17	Card presence detection pin	18	Card presence detection pin

9.2.3 HDMI source connector CN3

Figure 21. HDMI source connector CN3 (front view)

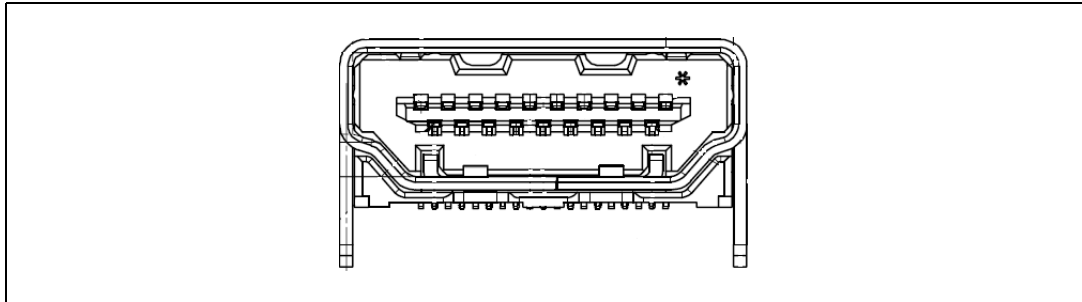


Table 33. HDMI source connector CN3

Pin number	Description	Pin number	Description
1,3,4,6,7,9,10,12	TMDS differential signal pair connected to CN1	16	I2C1_SDA (PB7)
13	CEC (PB10)	2,5,8,11,17	GND
14	NC	18	HDMI_5V_Source from power switch U3
15	I2C1_SCL (PB6)	19	HPD (PD3)

9.2.4 Daughterboard female connector CN4 and CN5

Two female connectors CN4 and CN5 are used to implement the legacy peripheral daughterboard on the mother board. CN4 on legacy daughterboard is connected to CN5 on mother board, and CN5 on legacy daughterboard is connected to CN4 on mother board. Please refer to [Section 9.1.3](#) for detail signal definition of these connectors.

9.3 Connectors on UCPD daughterboard

9.3.1 USB Type A connector CN1

Figure 22. USB Type A connector CN1 (front view)

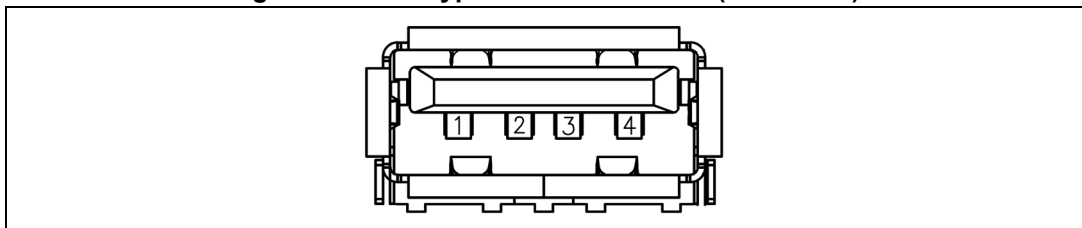


Table 34. USB Type A connector CN1

Pin number	Description	Pin number	Description
1	VBUS (power)	3	D+
2	D-	4	GND

9.3.2 DisplayPort source connector CN2

Figure 23. DisplayPort source connector CN2 (front view)

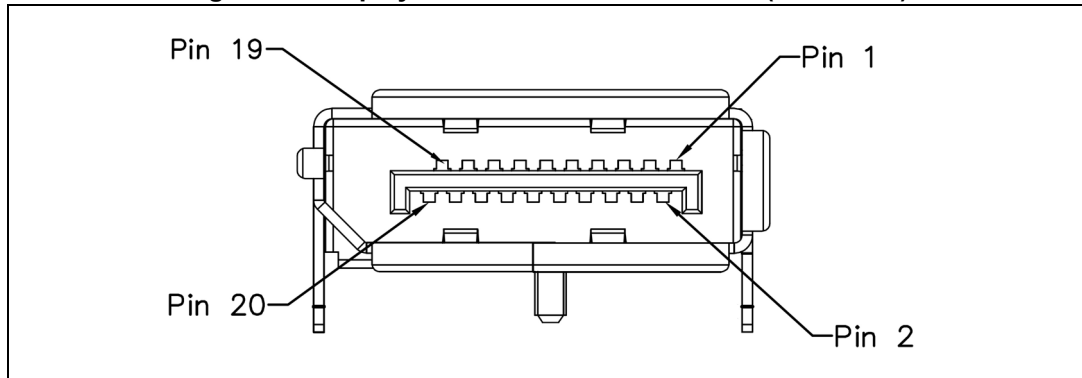


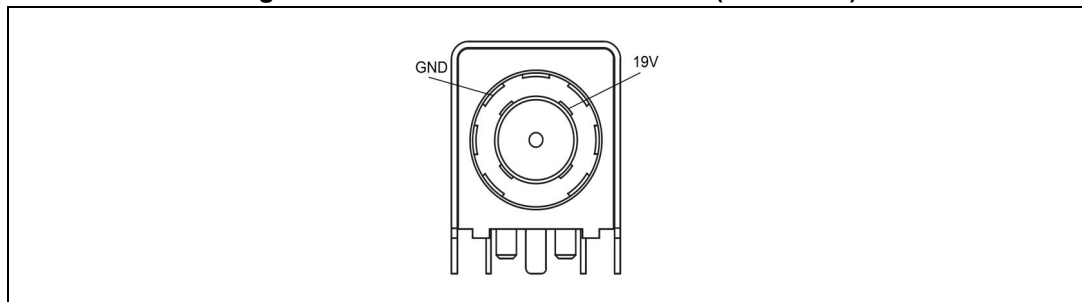
Table 35. DisplayPort source connector CN2

Pin number	Description	Pin number	Description
1	LANE0_P	13	CONFIG1
3	LANE0_N	14	CONFIG2
4	LANE1_P	15	AUX_CH_P
6	LANE1_N	17	AUX_CH_N
7	LANE2_P	18	HPD (PC6)
9	LANE2_N	19	RETURN
10	LANE3_P	20	DP_PWR
12	LANE3_N	2,5,8,11,16	GND

9.3.3 19 V Power connector CN3

The UCPD daughterboard can be powered from a DC 19 V power supply via the external power supply jack (CN3) shown in [Figure 24](#). And it is used for USB PD.

Figure 24. 19 V Power connector CN3 (front view)



9.3.4 USB3.1 Gen1 Type B connector CN4

Figure 25. USB3.1 Gen1 Type B connector CN4 (front view)

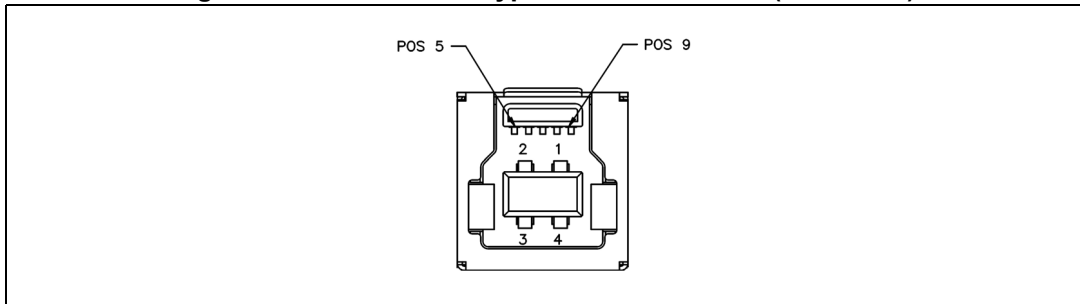


Table 36. USB3.1 Gen1 Type B connector CN4

Pin number	Description	Pin number	Description
1	VBUS (power)	5	SSTX-
2	D-	6	SSTX+
3	D+	7	GND_DRAIN
4	GND	8	SSRX-
-	-	9	SSRX+

9.3.5 USB Type-C connector PORT2 CN5

Figure 26. USB Type-C connector PORT2 CN5 (front view)

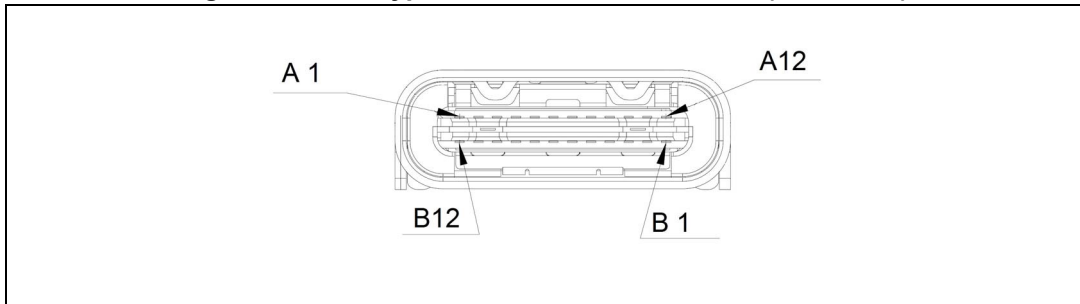


Table 37. USB Type-C connector PORT2 CN5

Pin number	Description	Pin number	Description
A1	GND	B1	GND
A2	TX1+	B2	TX2+
A3	TX1-	B3	TX2-
A4	VBUS	B4	VBUS
A5	CC1 (PD0)	B5	CC2 (PD2)
A6	D+	B6	D+
A7	D-	B7	D-

Table 37. USB Type-C connector PORT2 CN5 (continued)

Pin number	Description	Pin number	Description
A8	SBU1	B8	SBU2
A9	VBUS	B9	VBUS
A10	RX2-	B10	RX1-
A11	RX2+	B11	RX1+
A12	GND	B12	GND

9.3.6 Display port sink connector CN6

Figure 27. DisplayPort sink connector CN6 (front view)

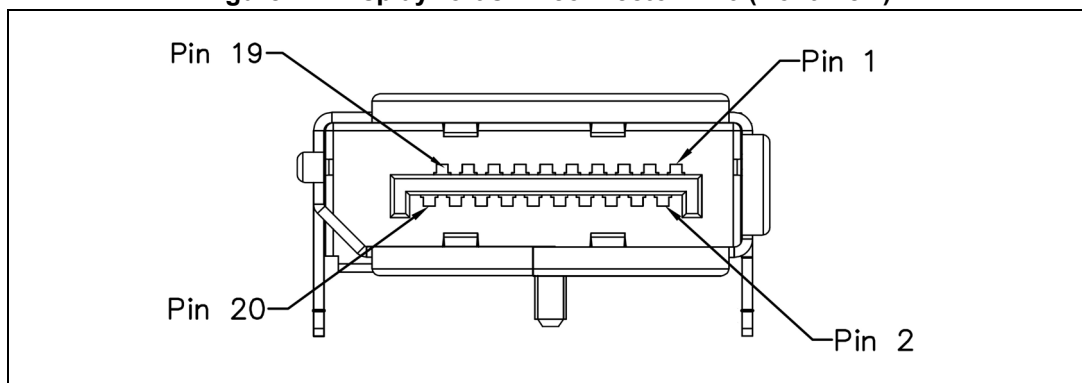


Table 38. DisplayPort sink connector CN6

Pin number	Description	Pin number	Description
1	LANE3_N	13	CONFIG1
3	LANE3_P	14	CONFIG2
4	LANE2_N	15	AUX_CH_P
6	LANE2_P	17	AUX_CH_N
7	LANE1_N	18	HPD (PB5)
9	LANE1_P	19	RETURN
10	LANE0_N	20	DP_PWR
12	LANE0_P	2,5,8,11,16	GND

9.3.7 USB Type-C connector PORT1 CN7

Figure 28. USB Type-C connector PORT1 CN7 (front view)

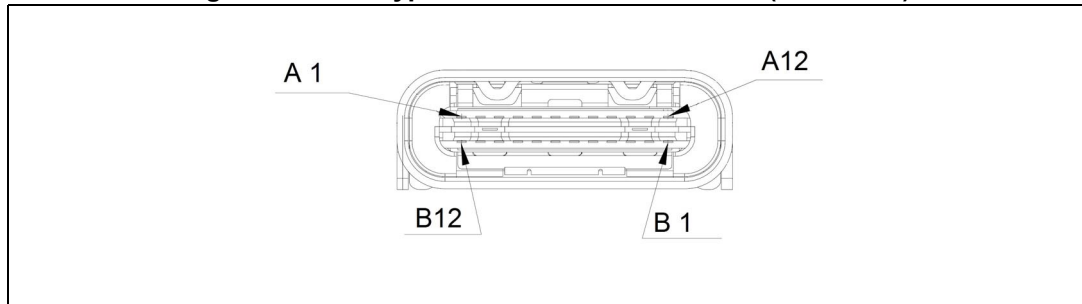


Table 39. USB Type-C connector PORT1 CN7

Pin number	Description	Pin number	Description
A1	GND	B1	GND
A2	TX1+	B2	TX2+
A3	TX1-	B3	TX2-
A4	VBUS	B4	VBUS
A5	CC1 (PA8)	B5	CC2 (PB15)
A6	D+	B6	D+
A7	D-	B7	D-
A8	SBU1	B8	SBU2
A9	VBUS	B9	VBUS
A10	RX2-	B10	RX1-
A11	RX2+	B11	RX1+
A12	GND	B12	GND

9.3.8 Daughterboard female connector CN8 and CN9

Two female connectors CN8 and CN9 are used to implement the UCPD daughterboard on mother board. CN8 on UCPD the daughterboard is connected to CN5 on the mother board, and CN9 on the UCPD daughterboard is connected to CN4 on the mother board. Please refer to [Section 9.1.3](#) for detail signal definition of these connectors.

Appendix A Electrical schematics

This chapter provides design schematics for the STM32G081B-EVAL key features to help users to implement these features in application designs:

- [Figure 29: STM32G081B-EVAL mother board top on page 48](#)
- [Figure 30: STM32G081B-EVAL MCU on page 49](#)
- [Figure 31: STM32G081B-EVAL power on page 50](#)
- [Figure 32: STM32G081B-EVAL audio on page 51](#)
- [Figure 33: STM32G081B-EVAL LCD microSD on page 52](#)
- [Figure 34: STM32G081B-EVAL motor-control on page 53](#)
- [Figure 35: STM32G081B-EVAL peripherals on page 54](#)
- [Figure 36: STM32G081B-EVAL RS232 and RS485 on page 55](#)
- [Figure 37: STM32G081B-EVAL extension connectors on page 56](#)
- [Figure 38: STM32G081B-EVAL ST-LINK V2-1 on page 57](#)
- [Figure 39: STM32G081B-EVAL SWD on page 58](#)
- [Figure 40: STM32G081B-EVAL legacy peripheral daughterboard on page 59](#)
- [Figure 41: STM32G081B-EVAL legacy peripheral daughterboard HDMI and CEC on page 60](#)
- [Figure 42: STM32G081B-EVAL legacy peripheral daughterboard Smartcard and IR on page 61](#)
- [Figure 43: STM32G081B-EVAL legacy peripheral daughterboard temperature sensor and LDR on page 62](#)
- [Figure 44: STM32G081B-EVAL UCPD daughterboard top on page 63](#)
- [Figure 45: STM32G081B-EVAL UCPD daughterboard CC and VCONN on page 64](#)
- [Figure 46: STM32G081B-EVAL UCPD daughterboard port1 DP USB3 on page 65](#)
- [Figure 47: STM32G081B-EVAL UCPD daughterboard Type-C source con on page 66](#)
- [Figure 48: STM32G081B-EVAL UCPD daughterboard port2 DP on page 67](#)
- [Figure 49: STM32G081B-EVAL UCPD daughterboard Type-C sink con on page 68](#)
- [Figure 49: STM32G081B-EVAL UCPD daughterboard Type-C sink con on page 68](#)
- [Figure 50: STM32G081B-EVAL UCPD daughterboard USB PD on page 69](#)
- [Figure 51: STM32G081B-EVAL UCPD daughterboard power on page 70](#)
- [Figure 52: STM32G081B-EVAL UCPD daughterboard source power on page 71](#)

Figure 29. STM32G081B-EVAL mother board top

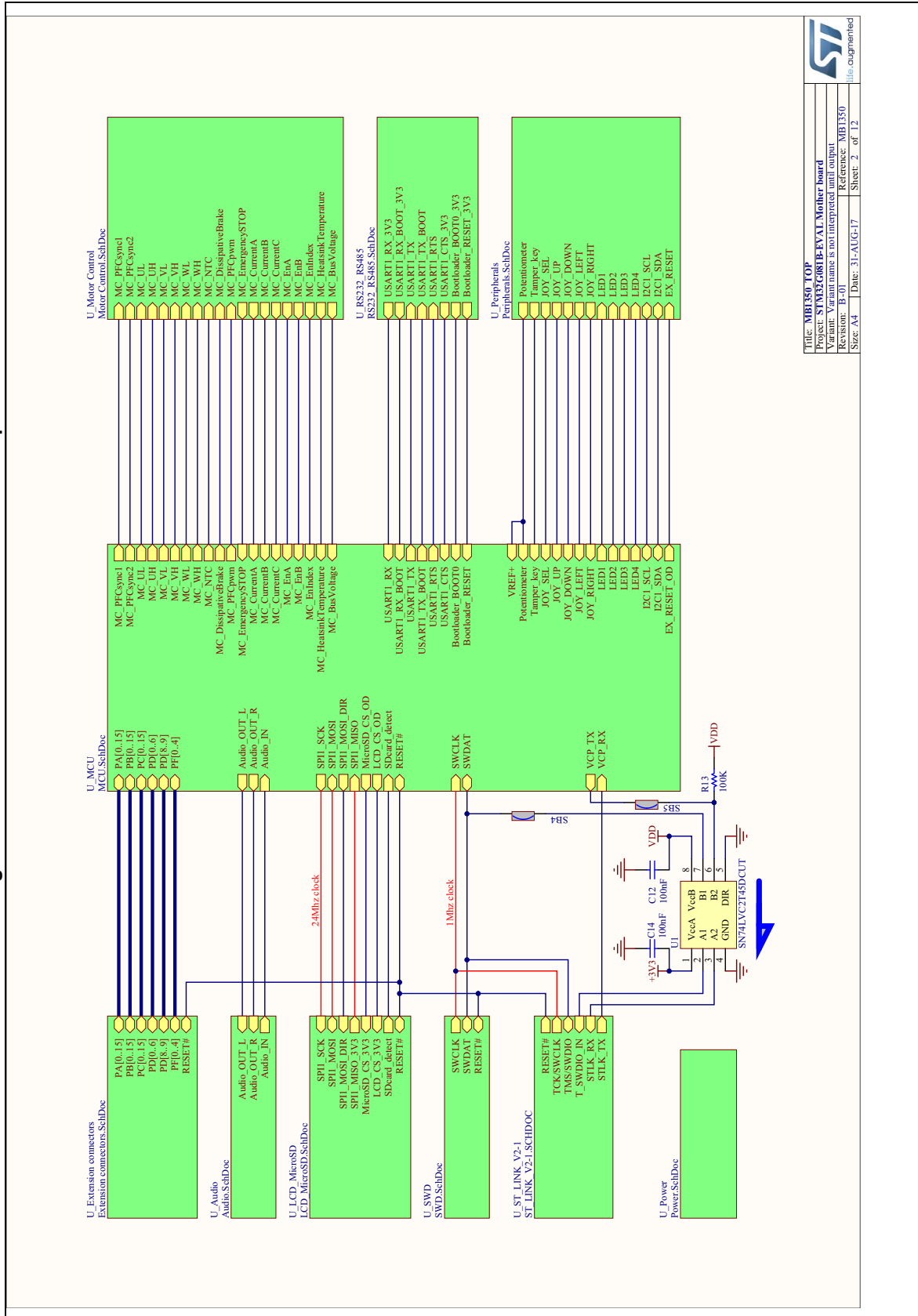
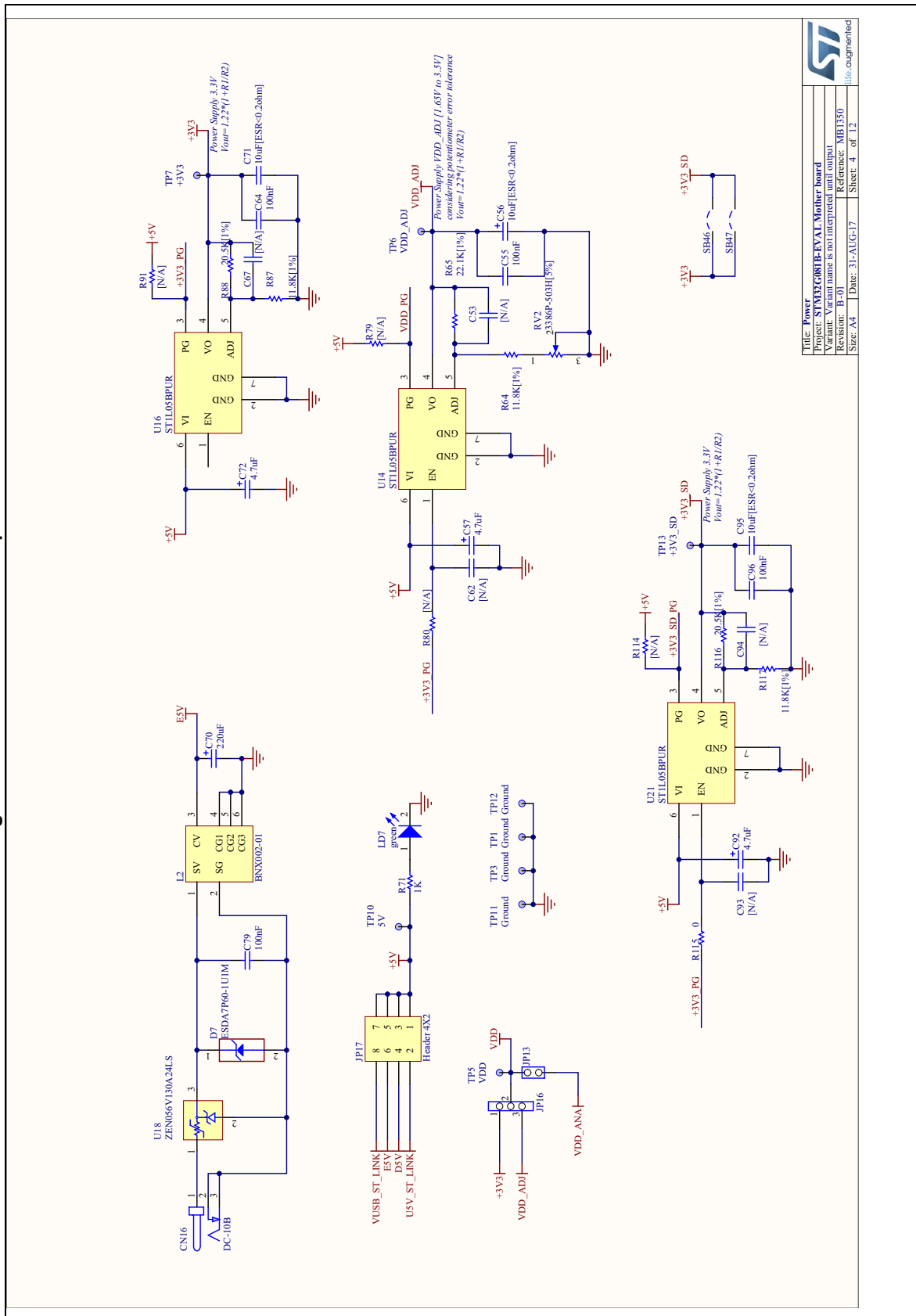


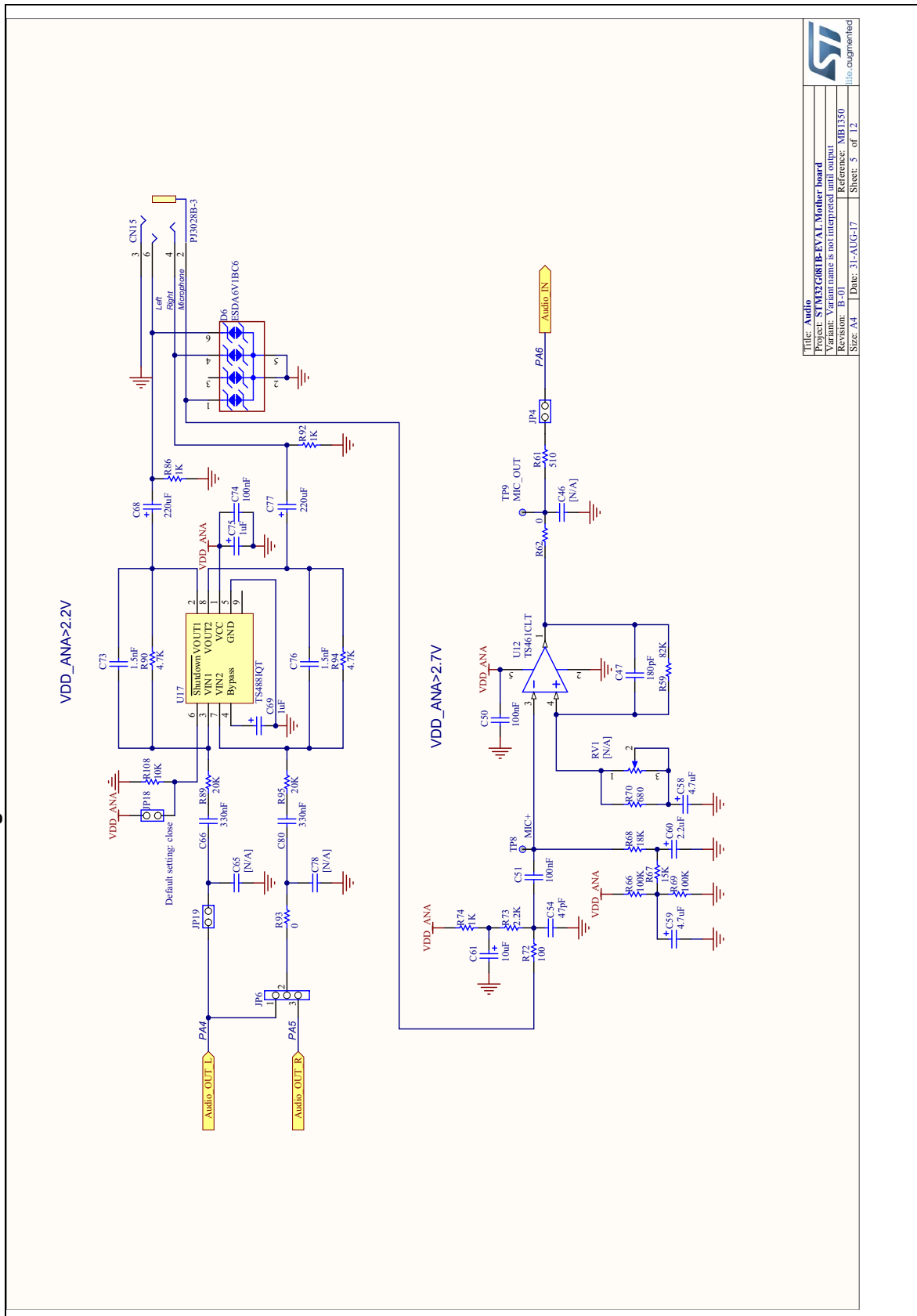
Figure 31. STM32G081B-EVAL power



Title: Power	
Project: STM32G081B-EVAL_Mother board	
Variant: Variant name is not interpreted until output	
Revision: B-01	Reference: MB1350
Size: A4	Date: 31-AUG-17
	Sheet: 4 of 12



Figure 32. STM32G081B-EVAL audio




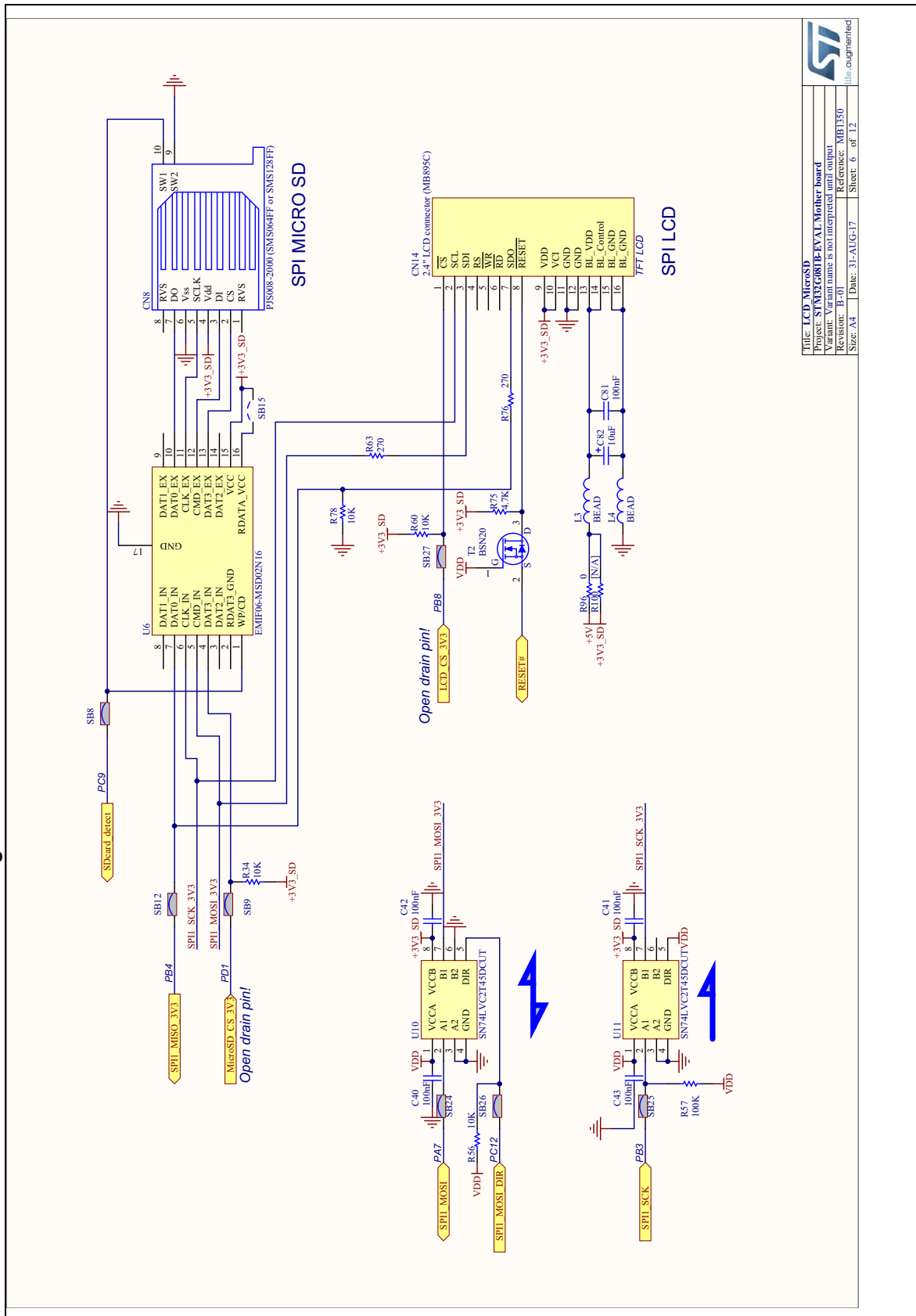
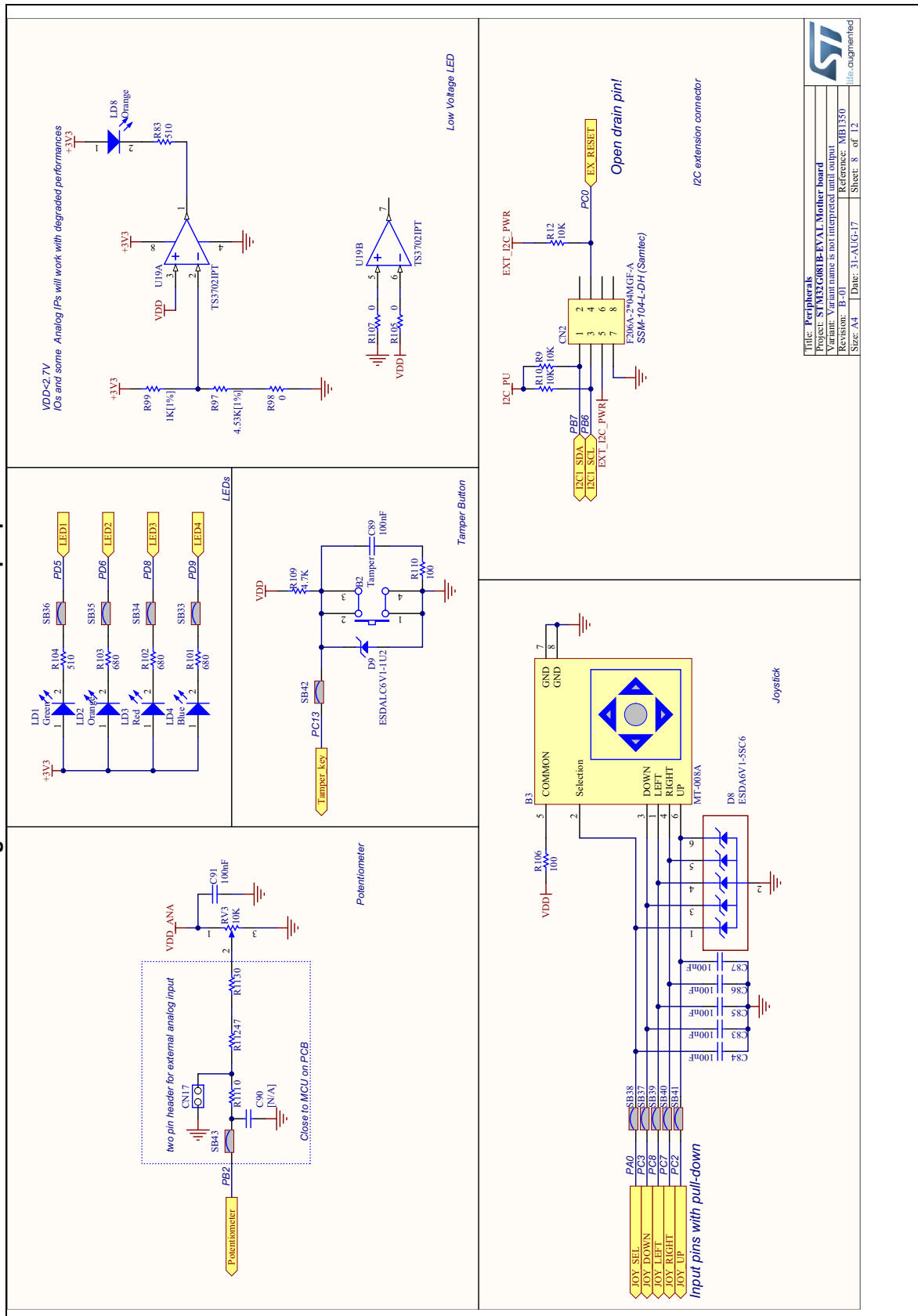
	
Title: Audio	Reference: MB1350
Project: STM32G081B-EVAL Mother board	Sheet: 5 of 12
Variant: Variant name is not interpreted until output	
Revision: B-01	
Size: A4	Date: 31-AUG-17
	File: aqmpnefied

Figure 33. STM32G081B-EVAL LCD microSD



	
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Project: STM32G081B-EVAL_Mother_board	
Variant: Variant name is not interpreted until output	
Revision: B-01	Reference: MB1350
Size: A4	Date: 31-AUG-17
Sheet: 6 of 12	

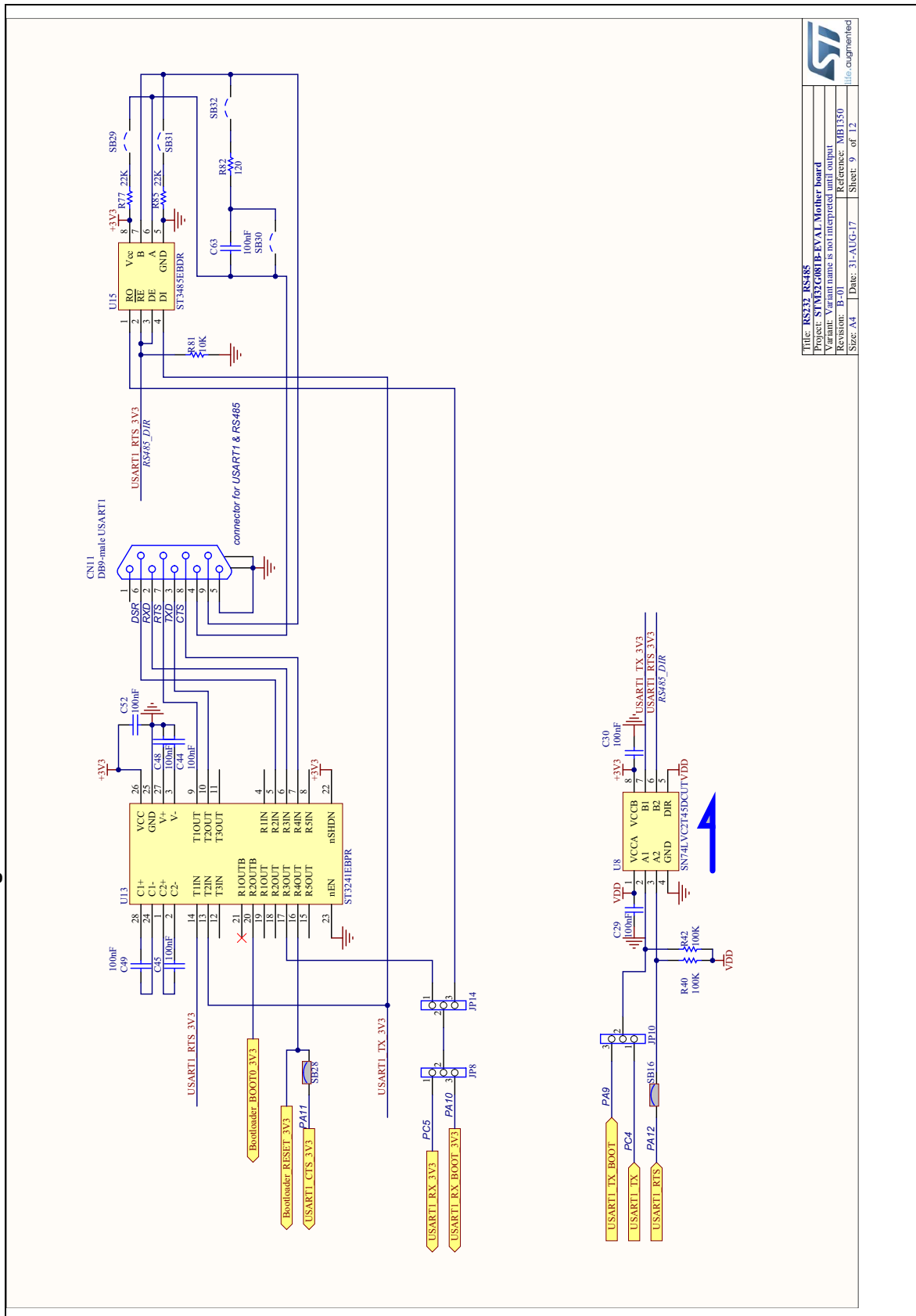
Figure 35. STM32G081B-EVAL peripherals



Peripherals	
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Variant:	Variant name is not interpreted until output
Revision:	B-01
Reference:	MB1350
Size:	A4
Date:	31-AUG-17
Sheet:	8 of 12



Figure 36. STM32G081B-EVAL RS232 and RS485



	
Title: RS232_RS485	Project: STM32G081B-EVAL Mother board
Variant: Variant name is not interpreted until output	Reference: MB1350
Revision: B-01	Size: A4
Date: 31-AUG-17	Sheet: 9 of 12

Figure 37. STM32G081B-EVAL extension connectors

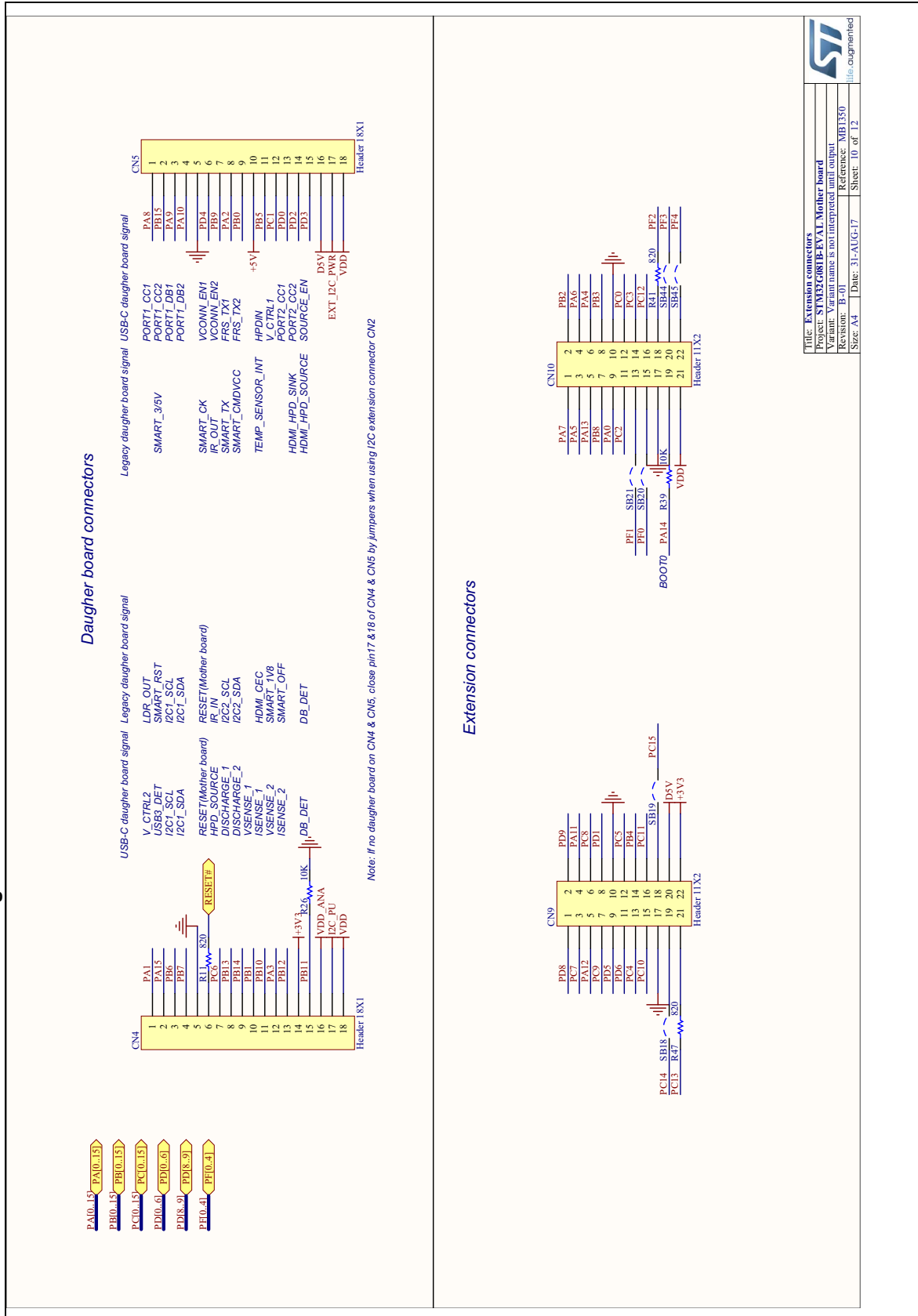
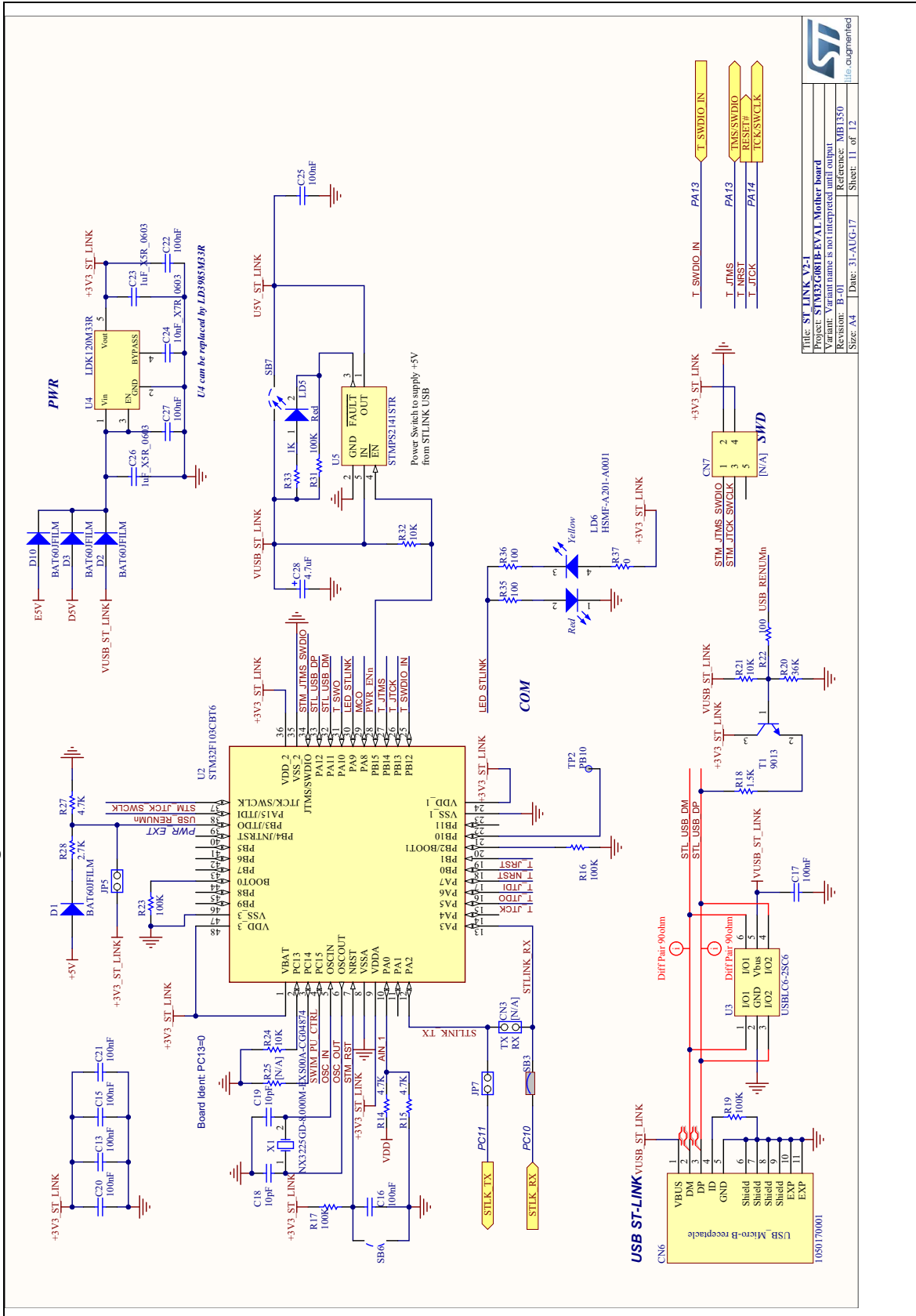


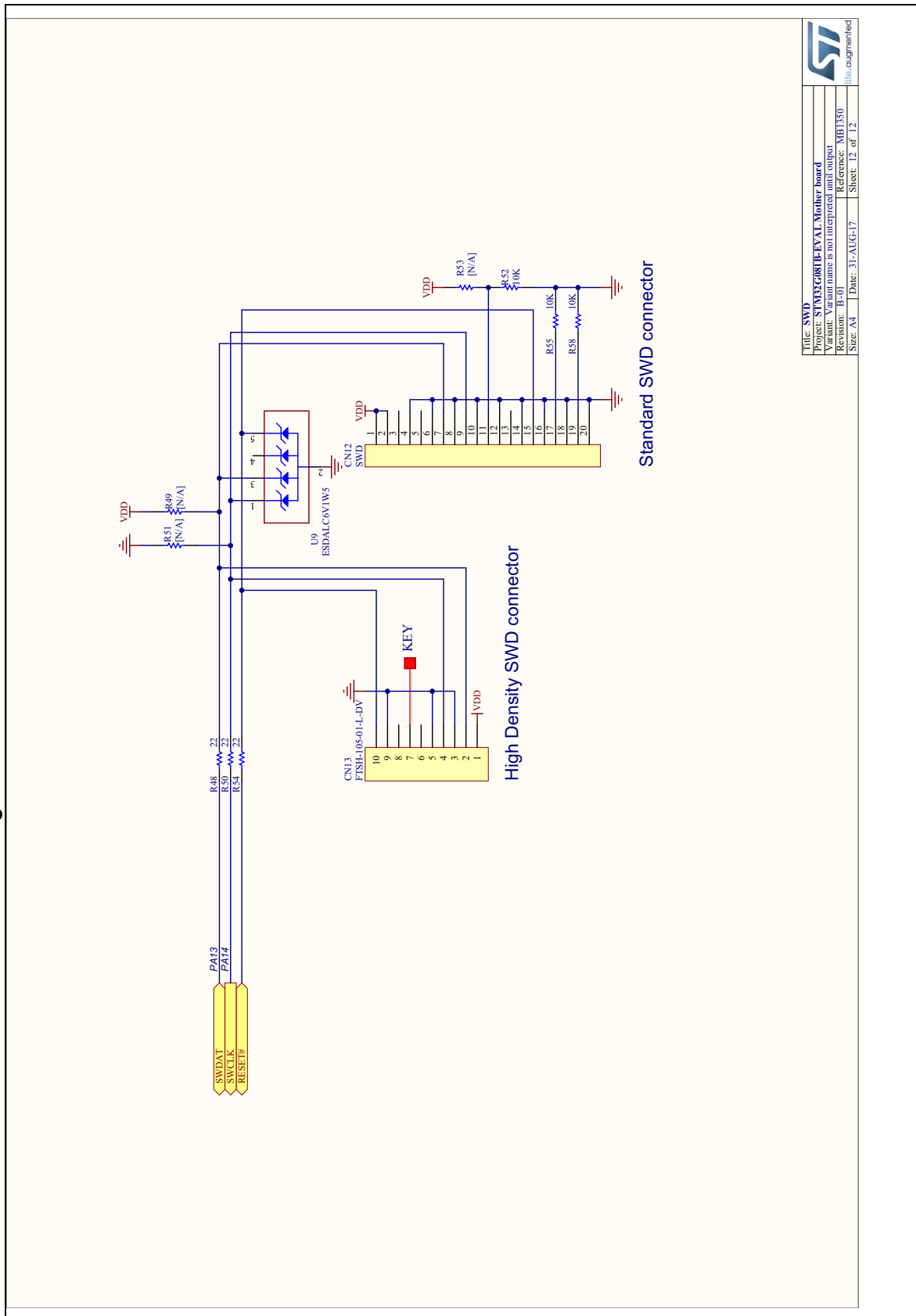
Figure 38. STM32G081B-EVAL ST-LINK V2-1



Title: ST-LINK V2-1			
Project: STM32G081B-EVAL Mother board			
Variant: Variant name is not interpreted until output			
Revision: B-01	Date: 31-AUG-17	Reference: MB1350	Sheet: 11 of 12
Size: A4			



Figure 39. STM32G081B-EVAL SWD



Title: SWD	
Project: STM32G081B-EVAL Mother board	
Variant: Variant name is not interpreted until output	
Revision: B-01	Reference: MB1350
Size: A4	Date: 31-AUG-17
Sheet: 12 of 12	

Figure 40. STM32G081B-EVAL legacy peripheral daughterboard

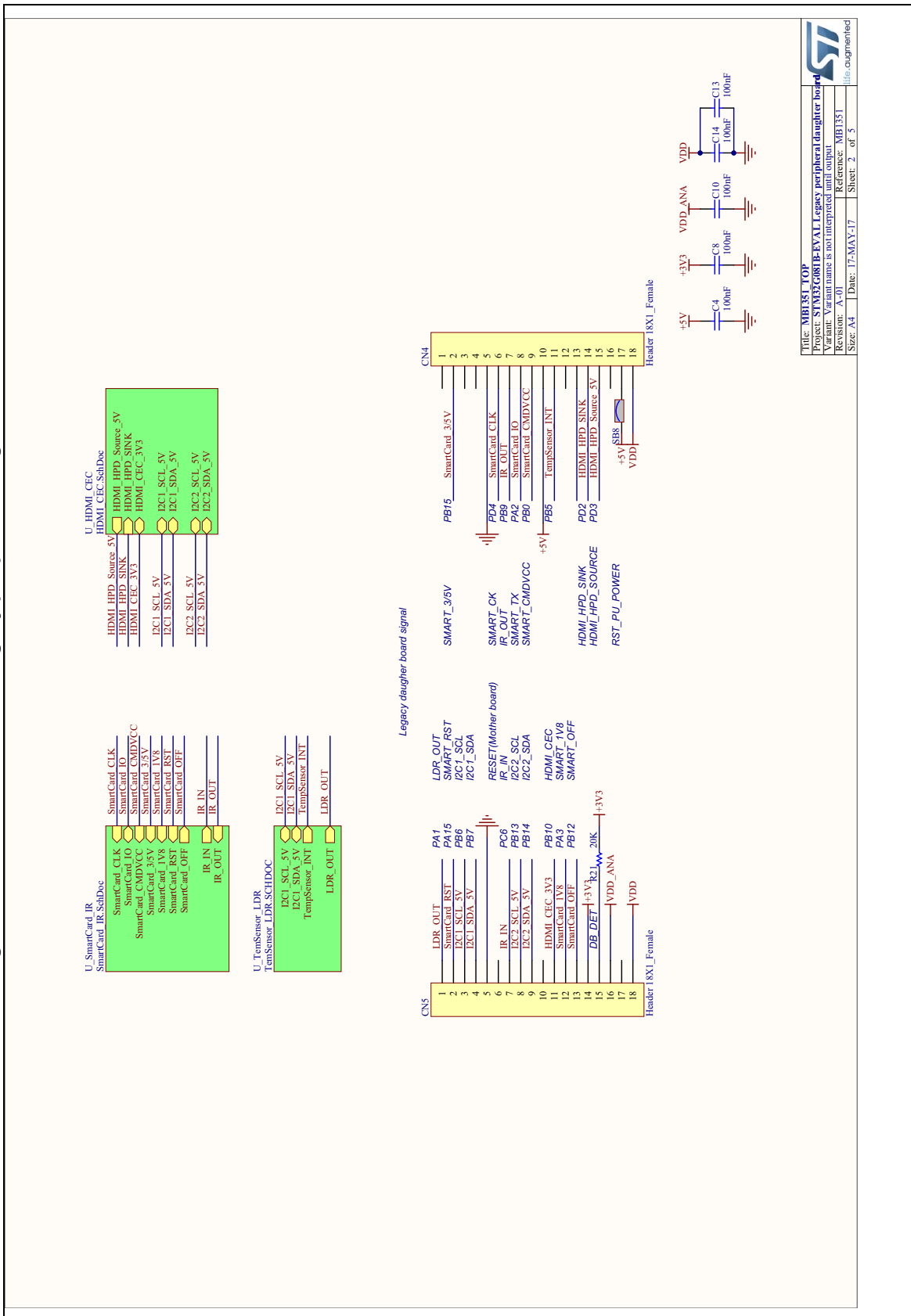
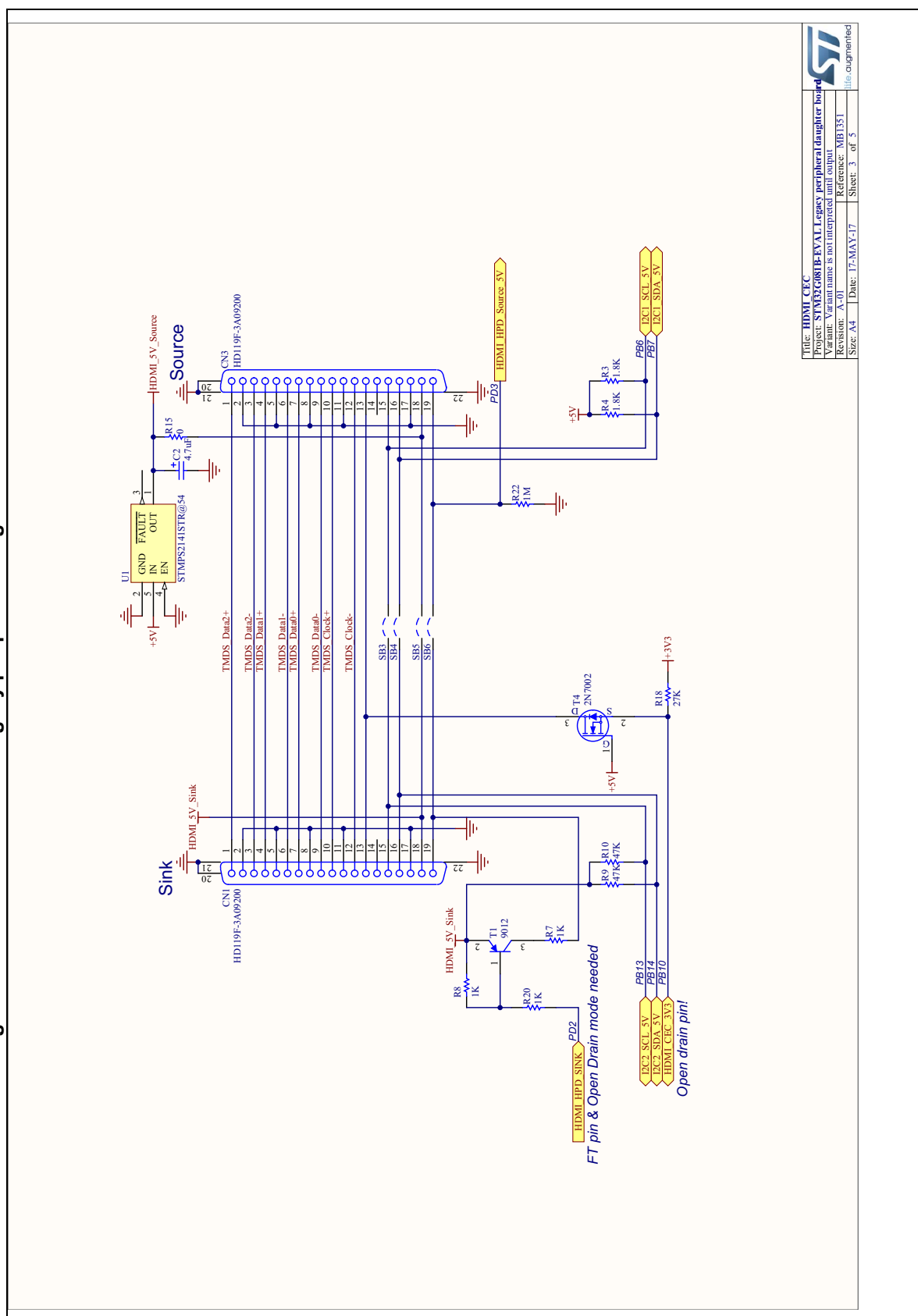


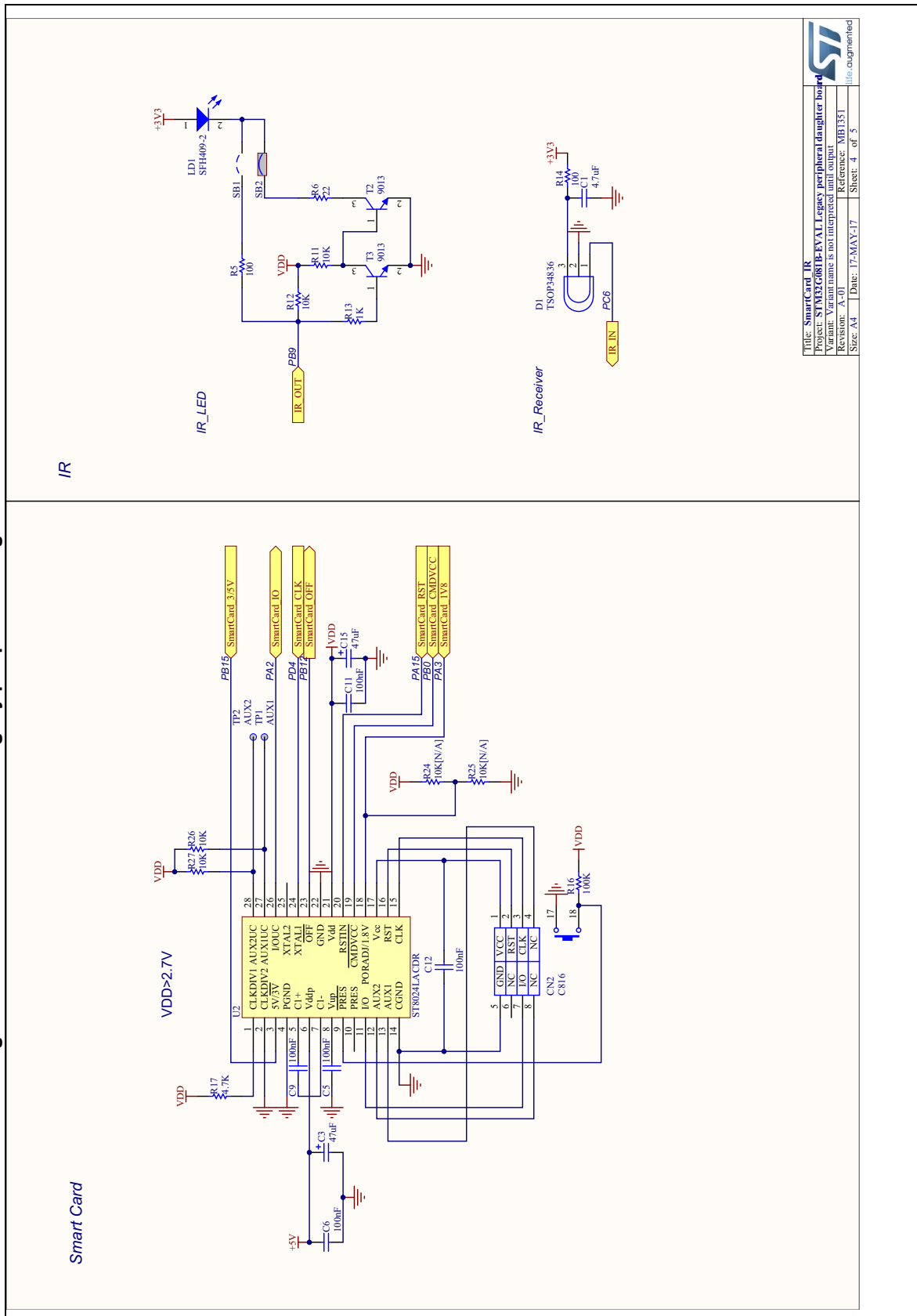
Figure 41. STM32G081B-EVAL legacy peripheral daughterboard HDMI and CEC



	
Title:	HDMI_CEC
Project:	STM32G081B-EVAL Legacy peripheral daughter board
Variant:	Variant name is not interpreted until output
Revision:	A-01
Reference:	MB1351
Size:	A4
Date:	17-MAY-17
Sheet:	3 of 5



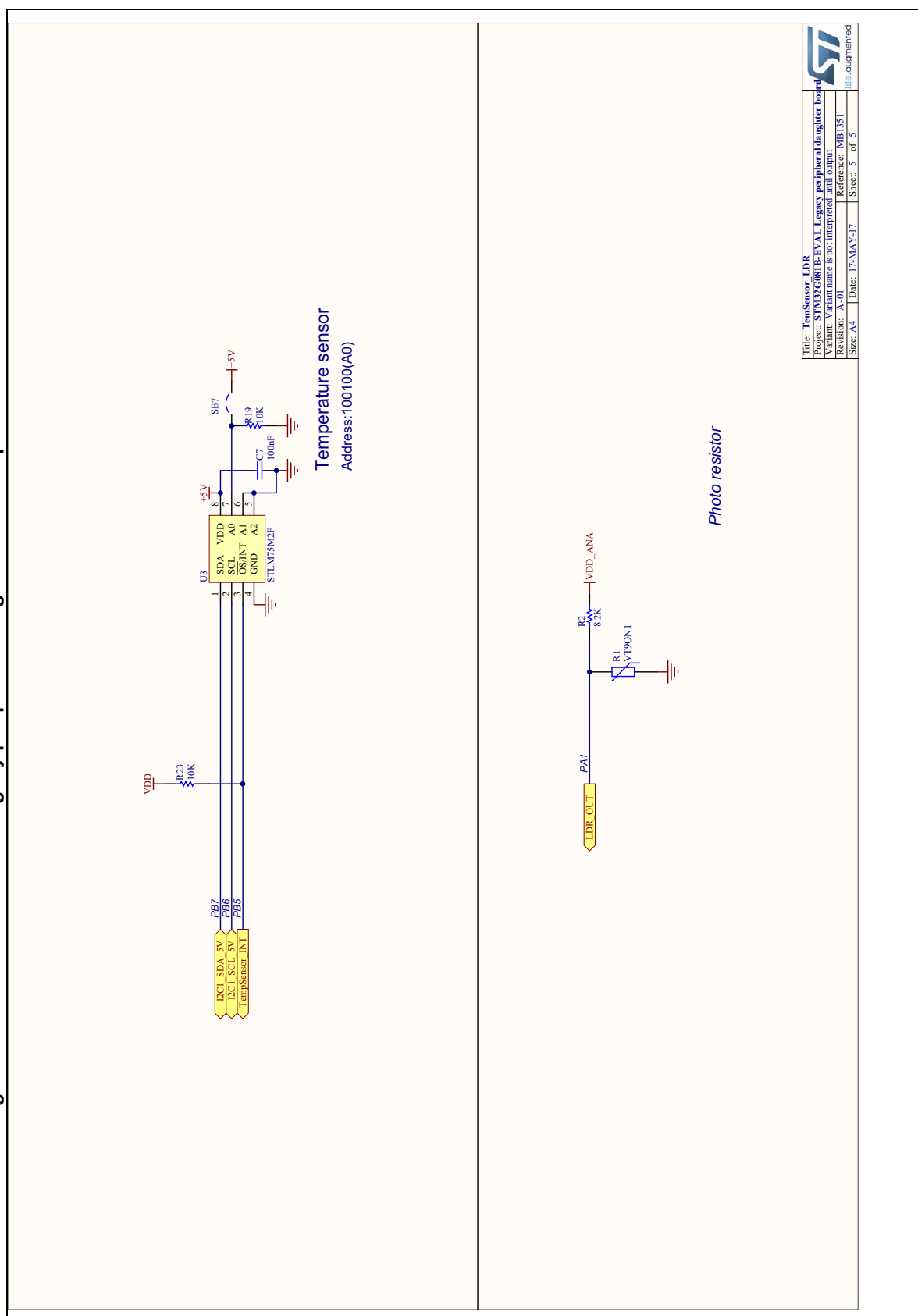
Figure 42. STM32G081B-EVAL legacy peripheral daughterboard Smartcard and IR



Title: SmartCard_IR	
Project: STM32G081B-EVAL legacy peripheral daughter board	
Variant: Variant name is not interpreted until output	
Revision: A-01	Reference: MB1351
Size: A4	Date: 17-MAY-17
Sheet: 4 of 5	



Figure 43. STM32G081B-EVAL legacy peripheral daughterboard temperature sensor and LDR



Title:	TempSensor_LDR
Project:	STM32G081B-EVAL legacy peripheral daughter board
Variant:	Variant name is not interpreted until output
Revision:	A-01
Reference:	MB1351
Size:	A4
Date:	17-MAY-17
Sheet:	5 of 5



Figure 45. STM32G081B-EVAL UCPD daughterboard CC and VCONN

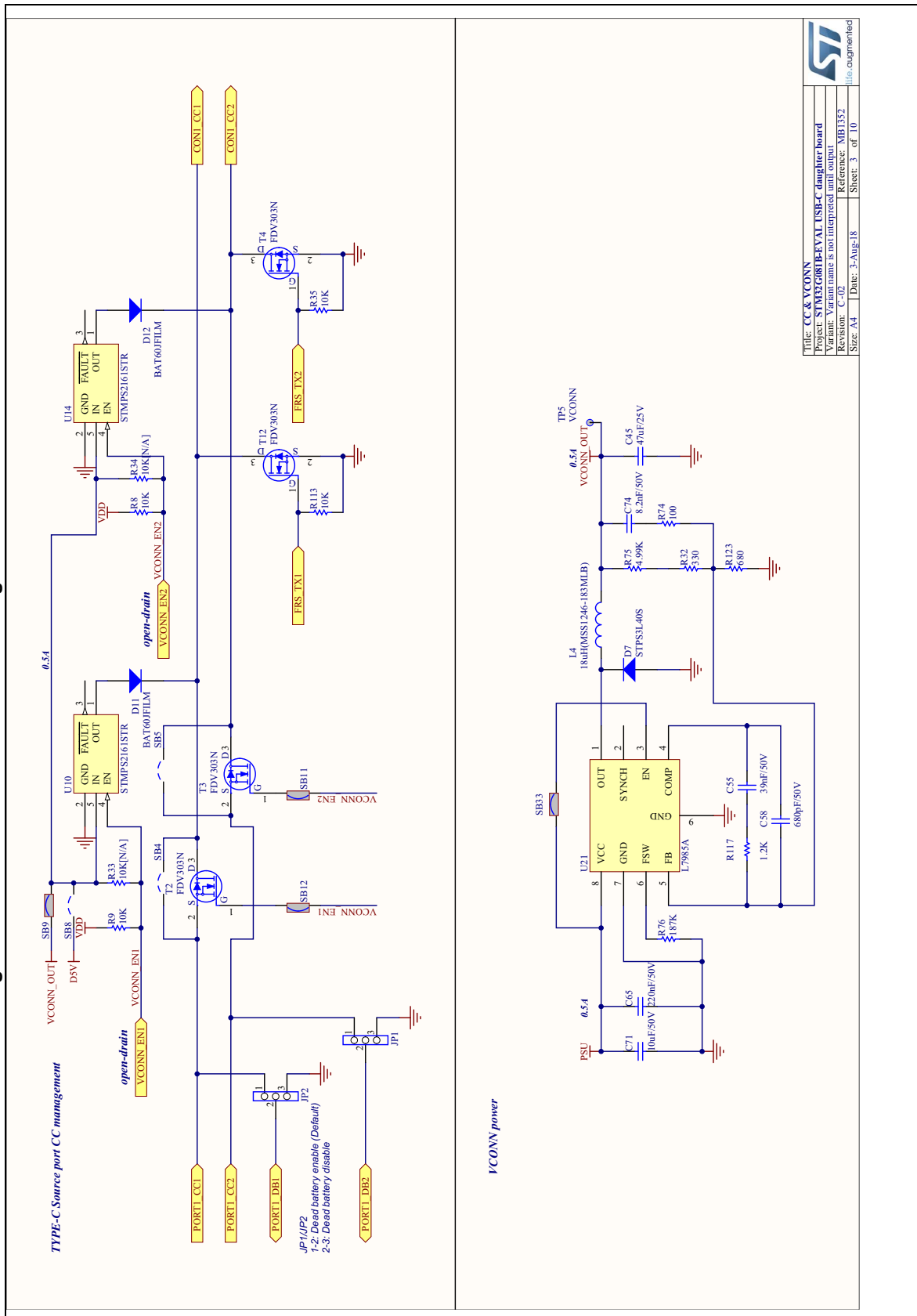


Figure 48. STM32G081B-EVAL UCPCD daughterboard port2 DP

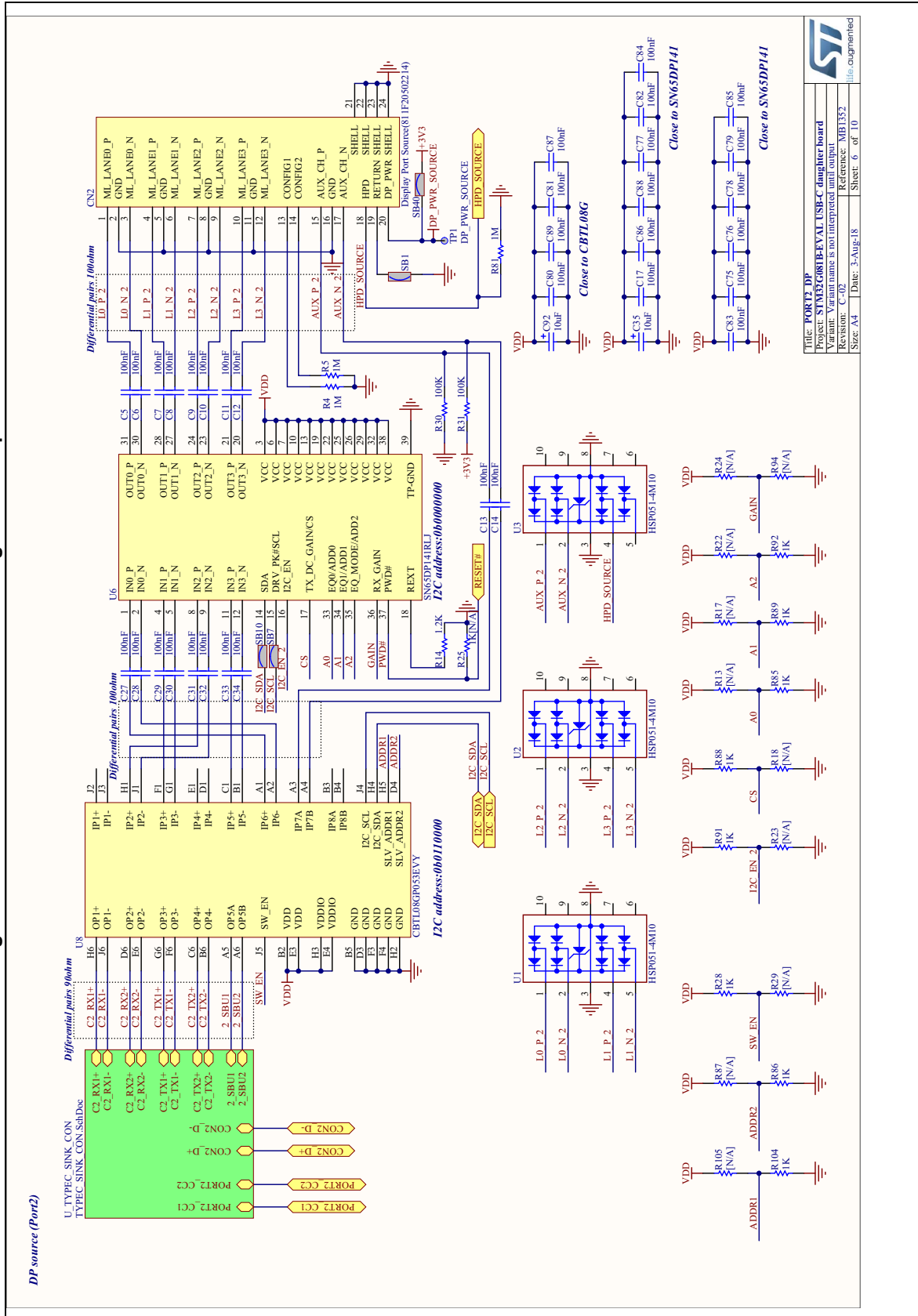
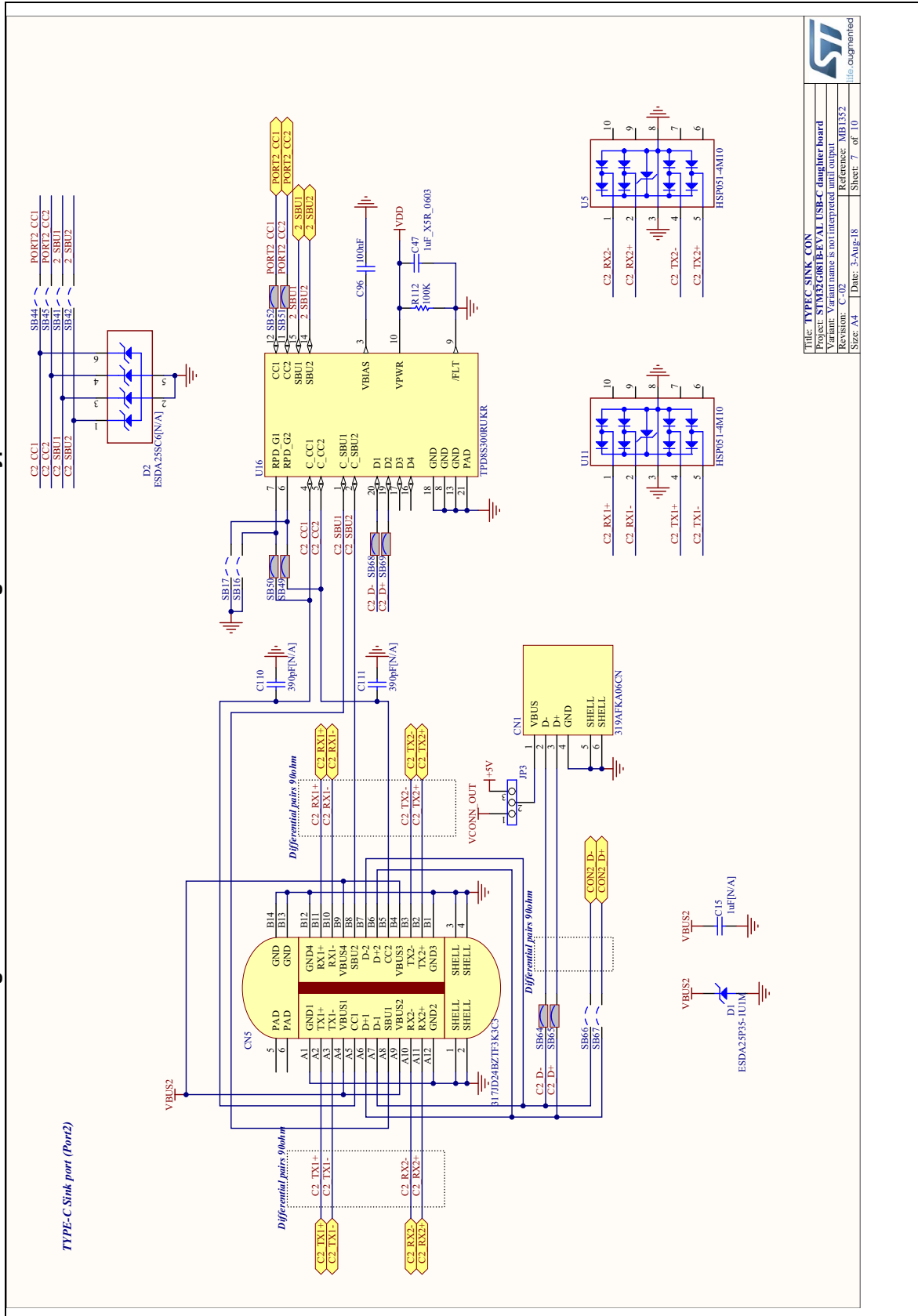


Figure 49. STM32G081B-EVAL UCPD daughterboard Type-C sink con




	
Title: TYPE-C SINK_CON	
Project: STM32G081B-EVAL USB-C daughter board	
Variant: Variant name is not interpreted until output	
Revision: C-02	
Reference: MB1352	Sheet: 7 of 10
Size: A4	Date: 3-Aug-18

Figure 50. STM32G081B-EVAL UCPCD daughterboard USB PD

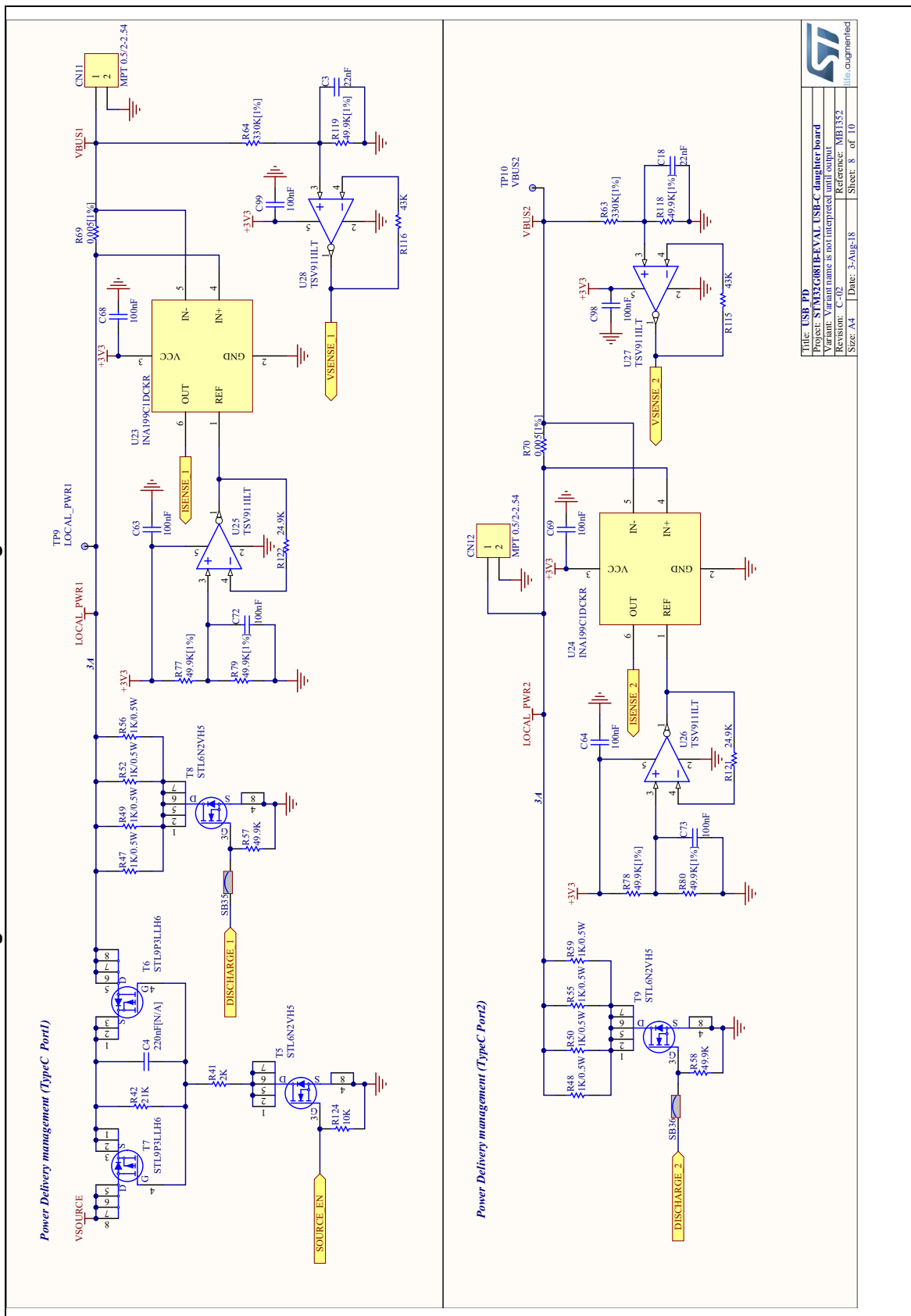
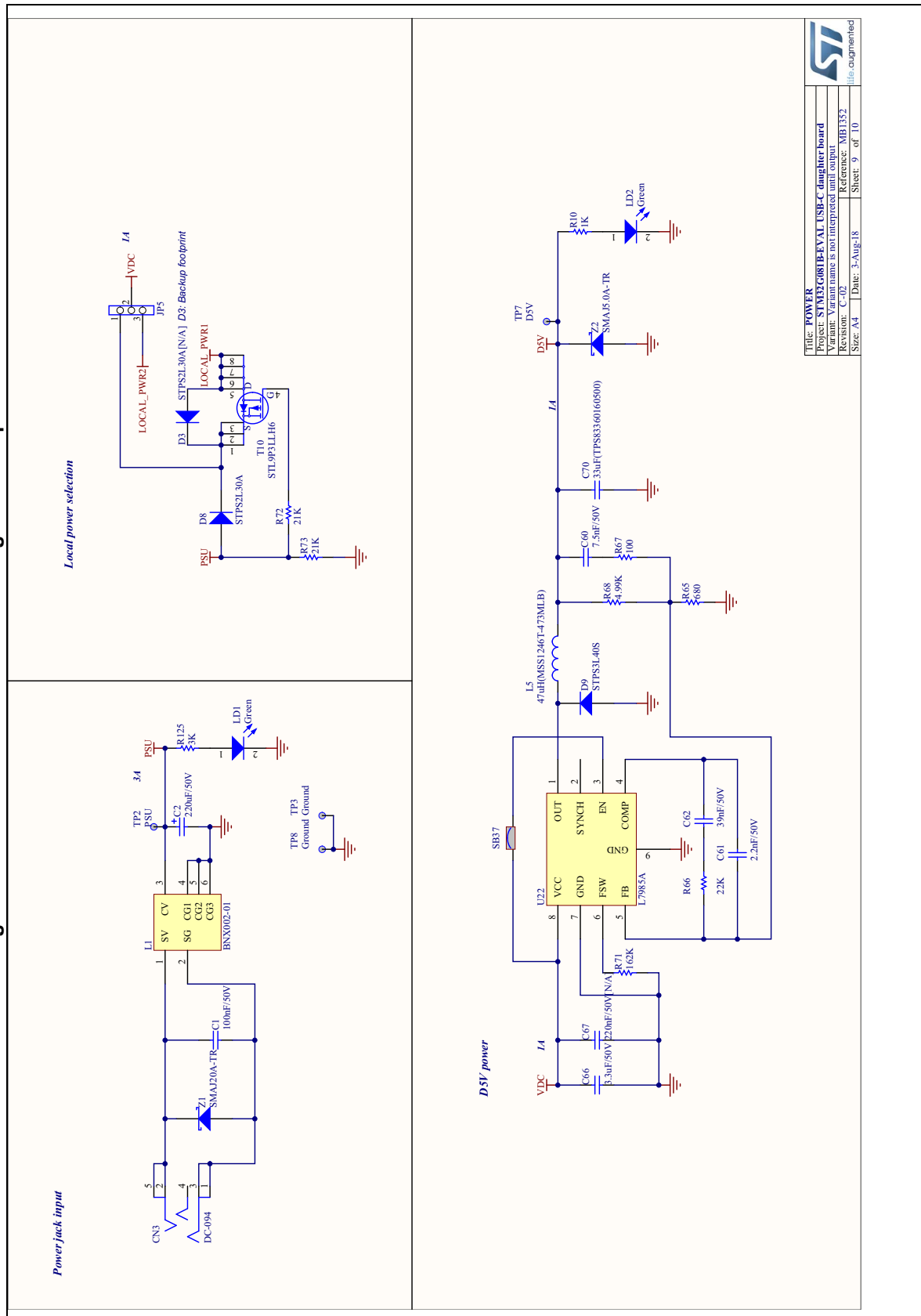


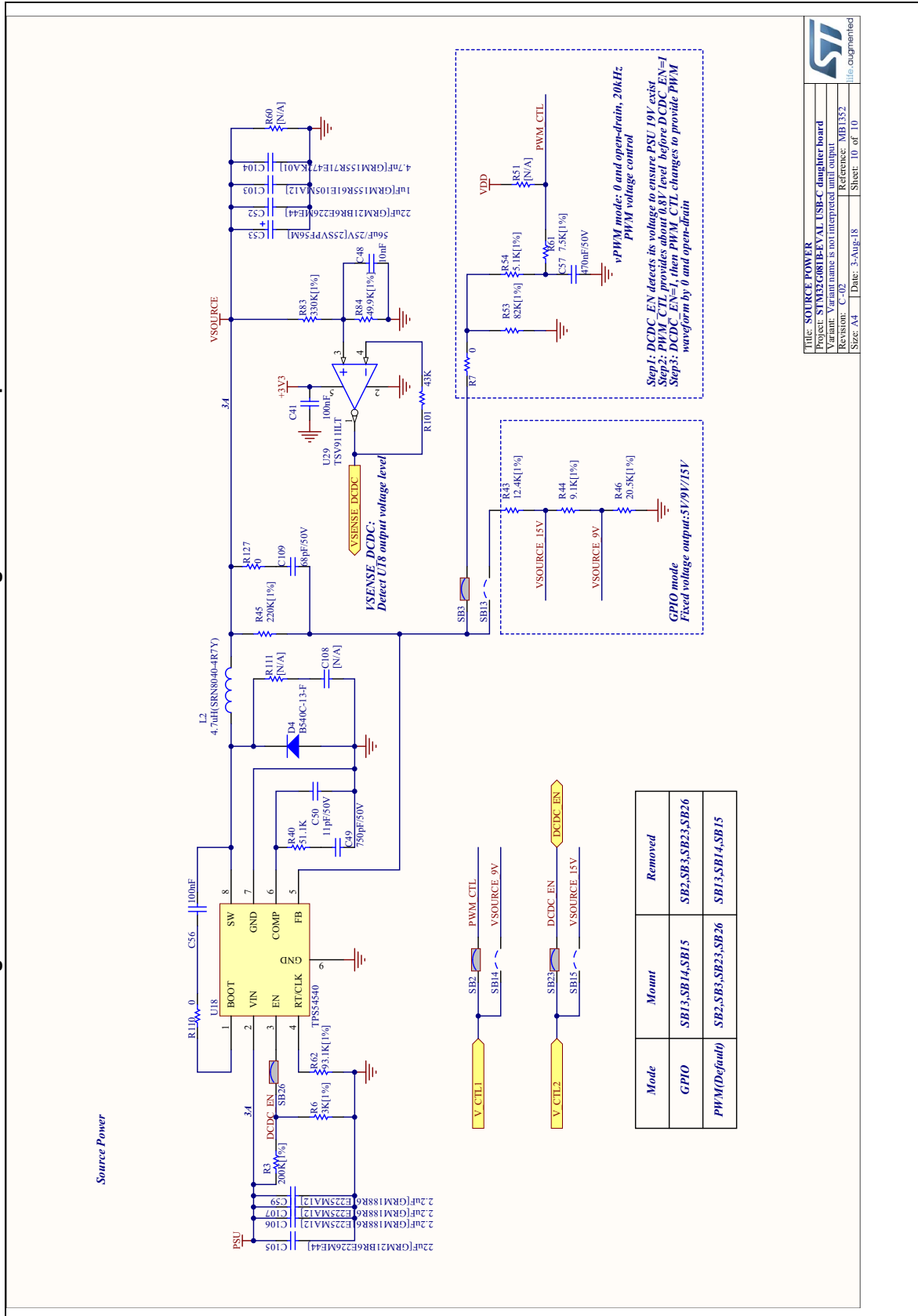
Figure 51. STM32G081B-EVAL UCPD daughterboard power



SI	
Title: POWER	
Project: STM32G081B-EVAL USB-C daughter board	
Variant: Variant name is not interpreted until output	
Revision: C-02	
Reference: MB1352	
Size: A4	Sheet: 9 of 10
Date: 3-Aug-18	Updated



Figure 52. STM32G081B-EVAL UCPCD daughterboard source power



Title: SOURCE POWER
Project: STM32G081B-EVAL USB-C daughter board
 Variant: Variant name is not interpreted until output
 Revision: C-02 Reference: MB1352
 Size: A4 Date: 3-Aug-18 Sheet: 10 of 10

Appendix B STM32G081B-EVAL IO Assignment

Table 40. STM32G081B-EVAL IO Assignment

Pin No.	Pin Name	IO Assignment on mother board	IO Assignment on legacy daughterboard	IO Assignment on UCPD daughterboard
1	PC11	VCP_USART_3_RX	-	-
2	PC12	GPIO_LCD / SD_MOSI_DIR	-	-
3	PC13	KEY_TAMP_IN1, RTC_TS, RTC_OUT1, WKUP2	-	-
4	PC14 - OSC32_IN	OSC32_IN	-	-
5	PC15 - OSC32_OUT	OSC32_OUT	-	-
6	PF3 - VBAT	VBAT	-	-
7	PF4 - VREF+	VREF+	-	-
8	VDD_1	VDD	-	-
9	VSS_1	VSS	-	-
10	PF0 - OSC_IN	OSC_IN	-	-
11	PF1 - OSC_OUT	OSC_OUT	-	-
12	PF2 - NRST	NRST, (WKUP8)	-	-
13	PC0	GPIO_EXT_RST	-	-
14	PC1	MC_IO_(PFC_sync1)	-	GPIO_9V_EN_LPTIM1_OUT
15	PC2	GPIO_JOY_UP	-	-
16	PC3	GPIO_JOY_DOWN	-	-
17	PA0	JOY_SEL_TAMP_IN2, WKUP1	-	-
18	PA1	MC_AIN1_COMP_1_INP (Bus voltage)	LDR_OUT_COMP_1_INP_ADC_IN1	GPIO_DP1_DET
19	PA2	MC_ADC_IN2(CurrentA)	SMART_2_TX	TYPE-C_1_FRSTX
20	PA3	MC_ADC_IN3(Heatsink temp)	GPIO_SMART_1V8	TYPE-C_2_V_ADC_IN3
21	PA4	AUDIO_OUT_DAC1_OUT1	-	-
22	PA5	AUDIO_OUT_DAC1_OUT2	-	-
23	PA6	AUDIO_IN_ADC_IN6 / MC_ADC_IN6(CurrentB)	-	-

Table 40. STM32G081B-EVAL IO Assignment (continued)

Pin No.	Pin Name	IO Assignment on mother board	IO Assignment on legacy daughterboard	IO Assignment on UCPD daughterboard
24	PA7	LCD/SD1_MOSI	-	-
25	PC4	USART_1_TX	-	-
26	PC5	USART_1_RX	-	-
27	PB0	MC_TIM_3_CH3(Encoder index)	GPIO_SMART_CMDVCC	TYPE-C_1_FRSTX
28	PB1	MC_TIM_3_CH4(PFC_PWM)	-	TYPE-C_1_V_ADC_IN9
29	PB2	POT_ADC_IN10	-	-
30	PB10	MC_ADC_IN11(CurrentC)	HDMI_CEC	TYPE-C_1_I_ADC_IN11
31	PB11	BOARD_DET_ADC_IN15	BOARD_DET_ADC_IN15	BOARD_DET_ADC_IN15
32	PB12	MC_TIM_1_BK(EmergencyS TOP)	GPIO_SMART_OFF	TYPE-C_2_I_ADC_IN16
33	PB13	-	I2C2_SCL (HDMI_SINK)	GPIO_DISCHARGE_1
34	PB14	-	I2C2_SDA (HDMI_SINK)	GPIO_DISCHARGE_2
35	PB15	MC_IO_ (Dissipative brake)	GPIO_SMART_3/5V	TYPE-C_1_CC2
36	PA8	MC_TIM_1_CH1(UH)	-	TYPE-C_1_CC1
37	PA9	USART_BOOT_1_TX / MC_TIM_1_CH2(VH)	-	TYPE-C_1_DBCC1
38	PC6	MC_TIM_3_CH1 (EncoderA)	IR_IN_TIM3_CH1	GPIO_DP2_HPDP
39	PC7	GPIO_JOY_RIGHT	-	-
40	PD8	LED3	-	-
41	PD9	LED4	-	-
42	PA10	USART_BOOT_1_RX / MC_TIM_1_CH3(WH)	-	TYPE-C_1_DBCC2
43	PA11 [PA9]	USART_1_CTS	-	-
44	PA12 [PA10]	USART_1_RTS_DE_CK	-	-
45	PA13	SWDIO	-	-
46	PA14 - BOOT0	SWCLK / BOOT0	-	-
47	PA15	-	GPIO_SMART_RST	GPIO_USB3_DET
48	PC8	GPIO_JOY_LEFT	-	-
49	PC9	GPIO_SD_DETECT	-	-
50	PD0	MC_TIM_16_CH1(PFC_sync 2)	-	TYPE-C_2_CC1

Table 40. STM32G081B-EVAL IO Assignment (continued)

Pin No.	Pin Name	IO Assignment on mother board	IO Assignment on legacy daughterboard	IO Assignment on UCPD daughterboard
51	PD1	GPIO_SD_CS	-	-
52	PD2	MC_TIM_1_CH1N(UL)	GPIO_HDMI_HPD_SINK	TYPE-C_2_CC2
53	PD3	MC_TIM_1_CH2N(VL)	GPIO_HDMI_HPD_SOURCE	GPIO_SOURCE_EN
54	PD4	MC_TIM_1_CH3N(WL)	SMART_2_RTS_DECK	GPIO_VCONN_EN_1_1
55	PD5	LED1	-	-
56	PD6	LED2	-	-
57	PB3	LCD/SD1_SCK	-	-
58	PB4	LCD/SD1_MISO	-	-
59	PB5	MC_TIM_3_CH2(EncoderB)	TEMP_SENSOR_INT_WKUP6	GPIO_15V_EN
60	PB6	I2C1_SCL	HDMI_SOURCE_I2C1_SCL	MUX_I2C1_SCL
61	PB7	I2C1_SDA	HDMI_SOURCE_I2C1_SDA	MUX_I2C1_SDA
62	PB8	GPIO_LCD_CS	-	-
63	PB9	MC_IO_(NTC_bypass)	IR_OUT	GPIO_VCONN_EN_1_2
64	PC10	VCP_USART_3_TX	-	-

Appendix C Federal Communications Commission (FCC) and Industry Canada (IC) Compliance Statements

C.1 FCC Compliance Statement

C.1.1 Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

C.1.2 Part 15.105

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

C.1.3 Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

C.2 IC Compliance Statement

C.2.1 Compliance Statement

Industry Canada ICES-003 Compliance Label: CAN ICES-3 (A)/NMB-3(A).

C.3 Déclaration de conformité

Étiquette de conformité à la NMB-003 d'Industrie Canada: CAN ICES-3 (A)/NMB-3(A).

Appendix D Mechanical dimensions

Figure 53. Mechanical dimensions

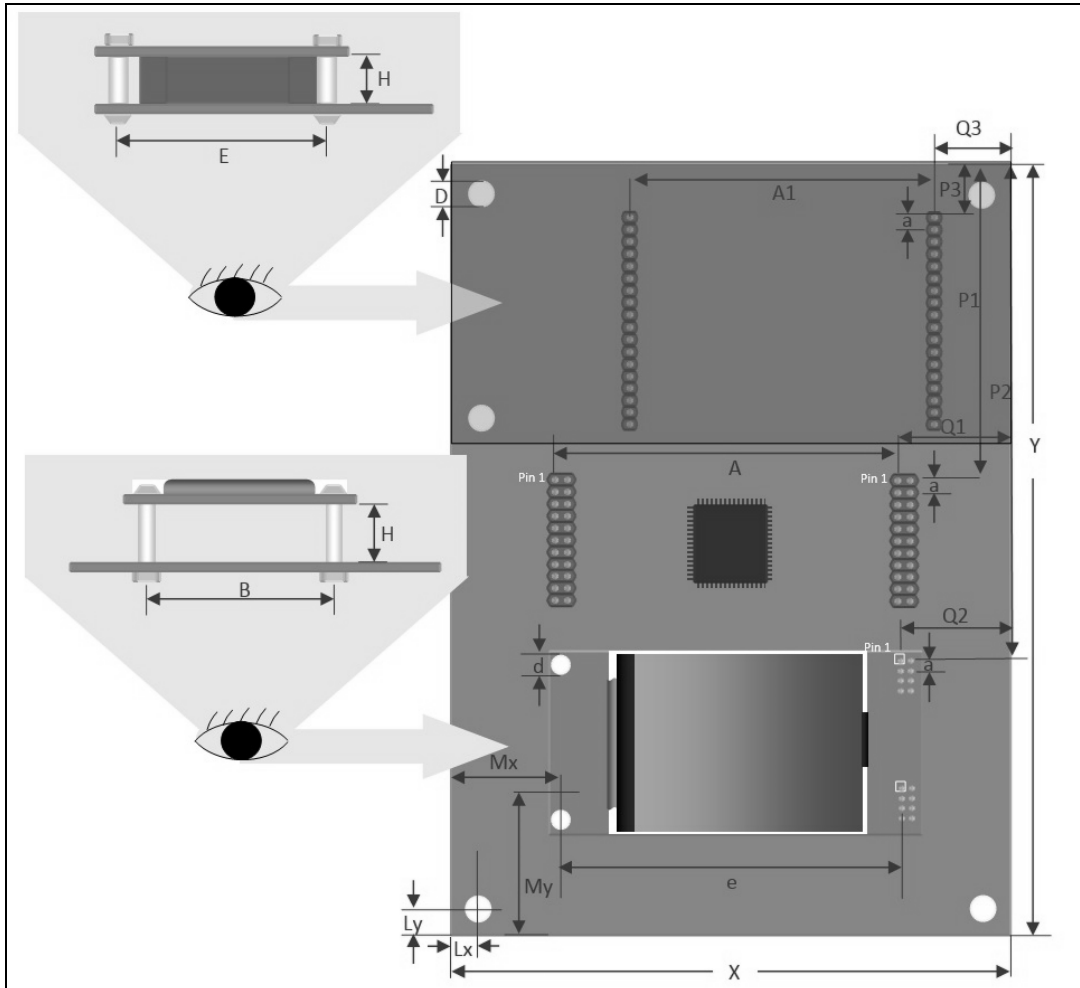


Table 41. Mechanical dimensions

Symbol	Size (mm)	Symbol	Size (mm)	Symbol	Size (mm)
A	68.58	e	77.44	P2	111.76
A1	61.97	H	11	P3	10.41
a	2.54	Lx	5.715	Q1	24.12
B	36	Ly	5.715	Q2	17.70
D	3.5	Mx	19.08	Q3	16
d	3.2	My	23.81	X	114.3
E	47	P1	65.78	Y	172.72

Revision history

Table 42. Document revision history

Date	Revision	Changes
7-Nov-2018	1	Initial version

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