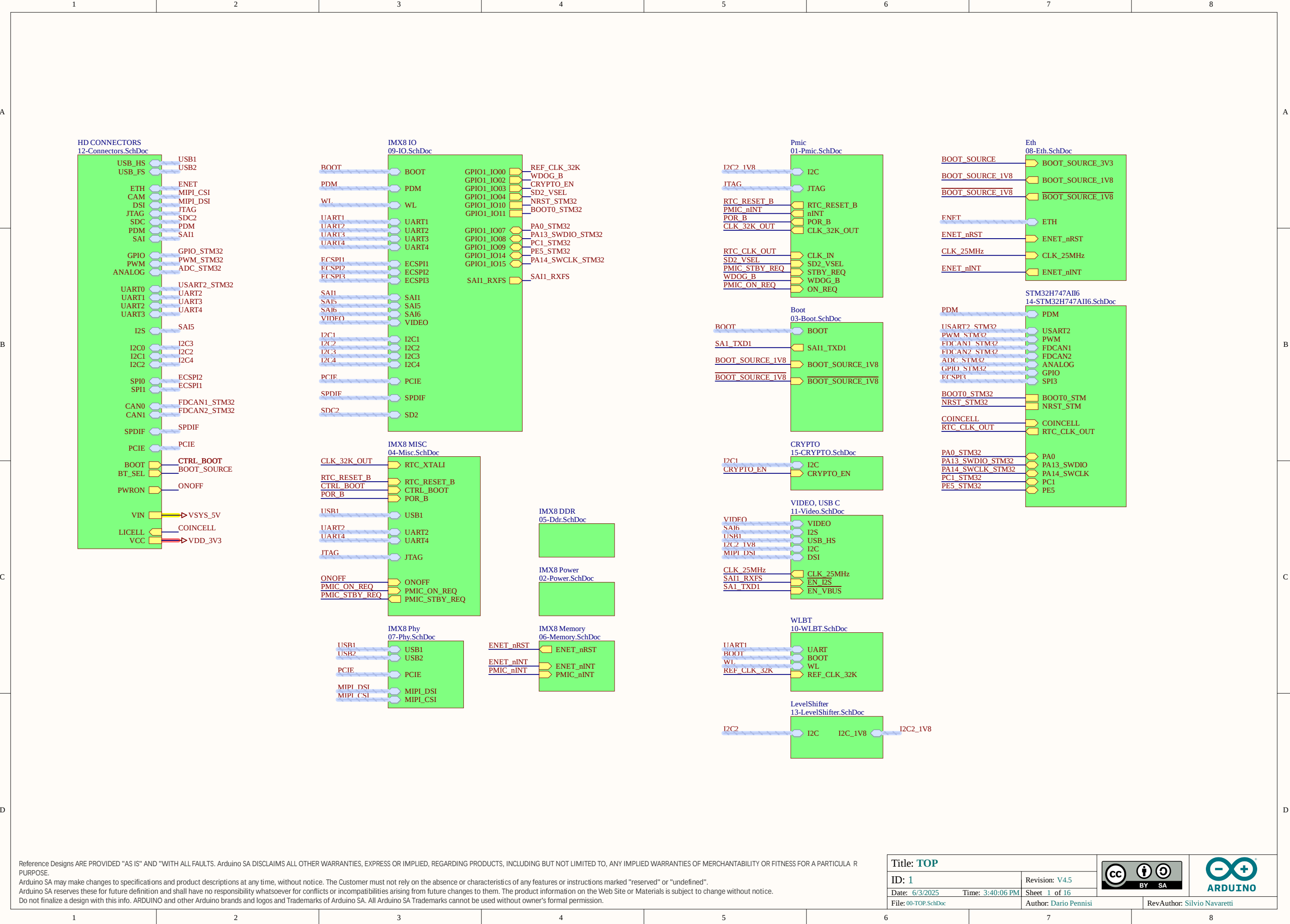




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Title: **TOP**

ID: **1**

Date: **6/3/2025**

File: 00-TOP.SchDoc

Revision: **V4.5**

Time: **3:40:06 PM**

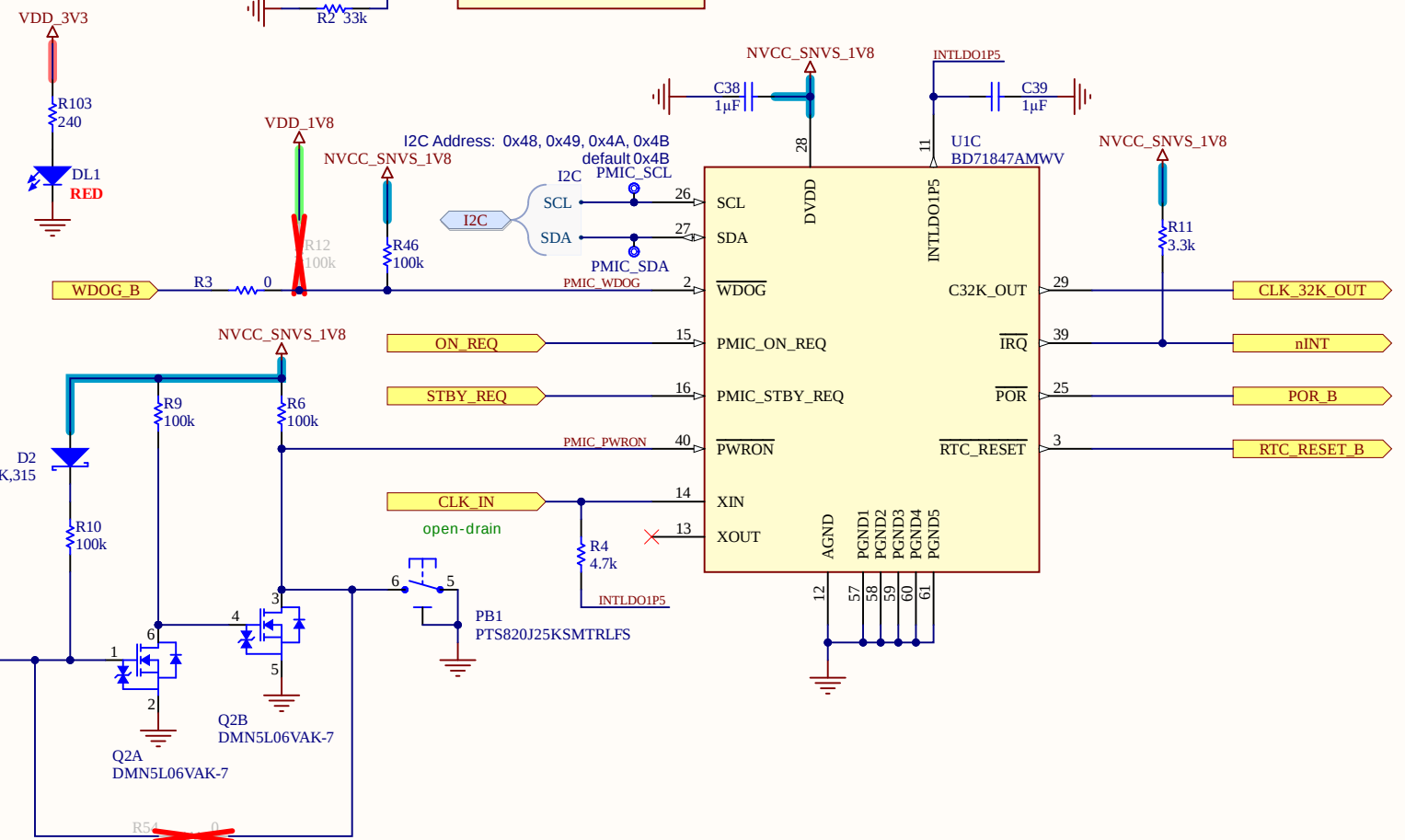
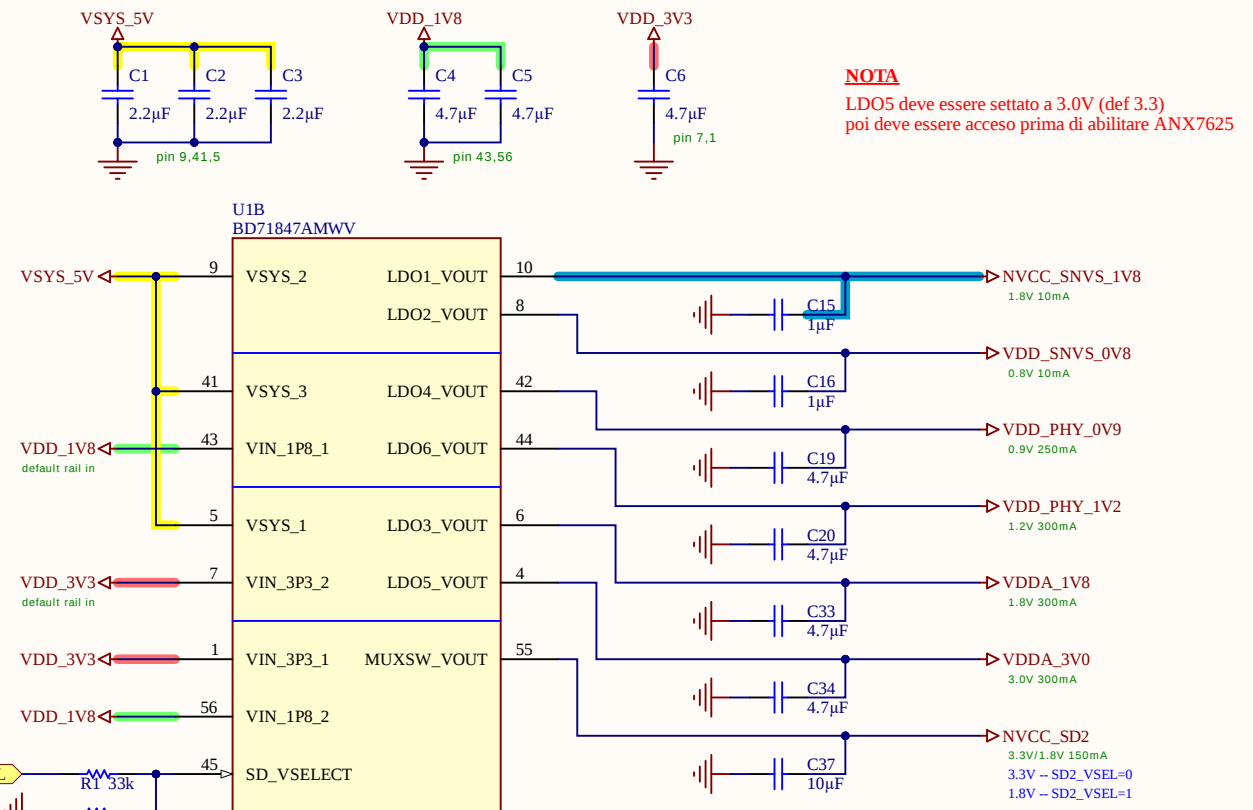
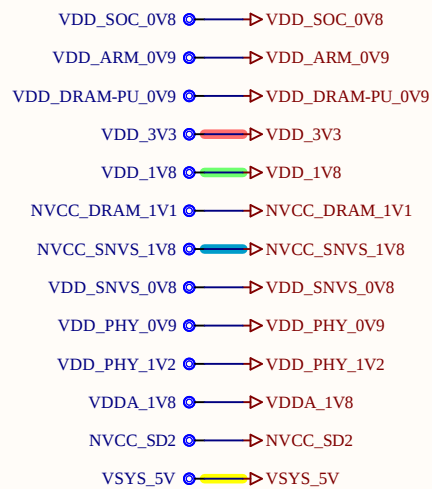
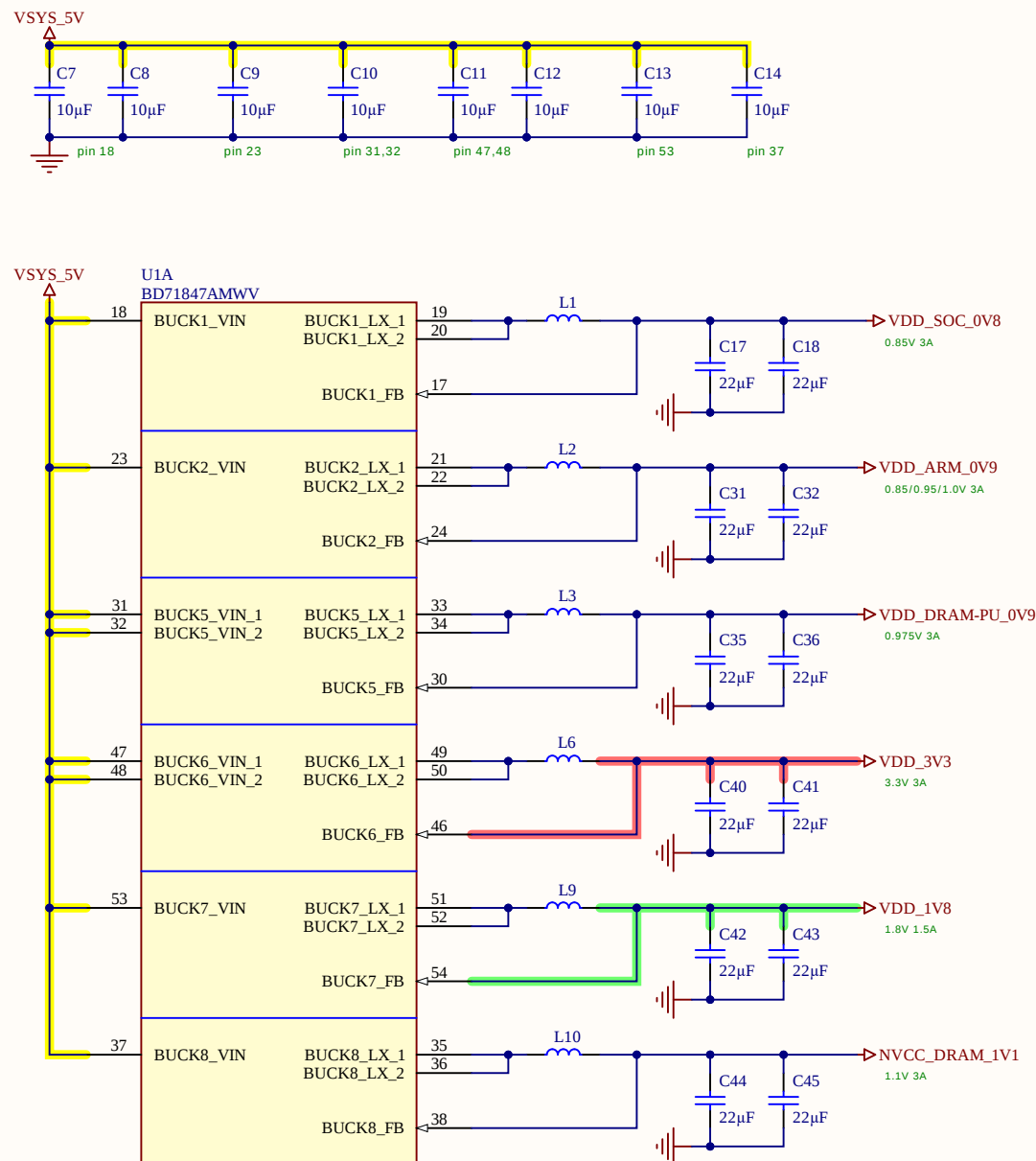
Sheet **1** of **16**

Author: **Dario Pennisi**

RevAuthor: **Silvio Navaretti**



IMX8Mmini PMIC



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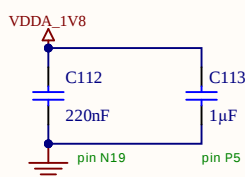
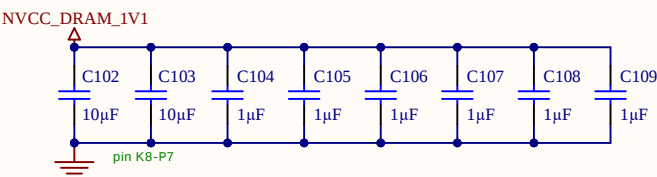
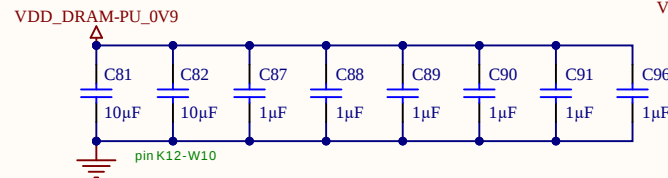
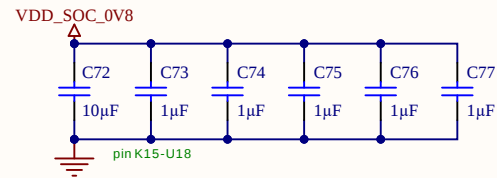
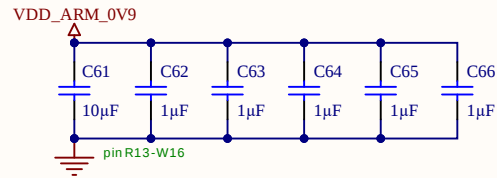
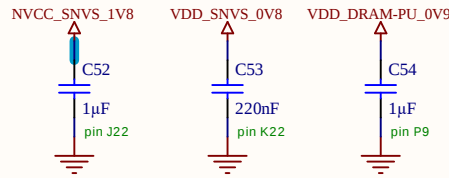
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Title: PMIC				
ID: 2	Revision: V4.5			
Date: 6/3/2025	Time: 3:40:07 PM	Sheet 2 of 16		
File: 01-Pmic.SchDoc		Author: Dario Pennisi	RevAuthor: Silvio Navaretti	

IMX8Mmini POWER



NVCC_SNVS_1V8

VDD_SNVS_0V8

VDDA_1V8

VDD_ARM_0V9

VDD_SOC_0V8

VDD_DRAM-PU_0V9

NVCC_DRAM_1V1

NVCC_DRAM_1V1

VDDA_1V8

VDD_DRAM-PU_0V9

U2M
MIMX8MM6CVTKZAA
i.MX8M Mini - POWER

NVCC_SNVS_1P8

VDD_SNVS_0P8

VDD_24M_XTAL_1P8

VDD_ARM1

VDD_ARM2

VDD_ARM3

VDD_ARM4

VDD_ARM5

VDD_ARM6

VDD_ARM7

VDD_ARM8

VDD_ARM9

VDD_ARM10

VDD_ARM11

VDD_ARM12

VDD_ARM13

VDD_ARM14

VDD_SOC1

VDD_SOC2

VDD_SOC3

VDD_SOC4

VDD_SOC5

VDD_SOC6

VDD_SOC7

VDD_SOC8

VDD_SOC9

VDD_SOC10

VDD_SOC11

VDD_SOC12

VDD_VPU1

VDD_VPU2

VDD_VPU3

VDD_VPU4

VDD_VPU5

VDD_VPU6

VDD_VPU7

VDD_GPU1

VDD_GPU2

VDD_GPU3

VDD_GPU4

VDD_GPU5

VDD_DRAM1

VDD_DRAM2

VDD_DRAM3

VDD_DRAM4

VDD_DRAM5

VDD_DRAM6

NVCC_DRAM1

NVCC_DRAM2

NVCC_DRAM3

NVCC_DRAM4

NVCC_DRAM5

NVCC_DRAM6

NVCC_DRAM7

NVCC_DRAM8

NVCC_DRAM9

NVCC_DRAM10

NVCC_DRAM11

NVCC_DRAM12

NVCC_DRAM13

VDD_DRAM_PLL_1P8

VDD_DRAM_PLL_0P8

NVCC_JTAG

NVCC_NAND

NVCC_SAI1

NVCC_SAI2

NVCC_SAI3

NVCC_SAI5

NVCC_GPIO1

NVCC_I2C

NVCC_UART

NVCC_ECSPi

NVCC_ENET

NVCC_SD1

NVCC_SD2

NVCC_CLK

VDD_USB_3P3

PVCC0_1P8

PVCC1_1P8

PVCC2_1P8

VDD_ARM_PLL_1P8

VDD_ANA0_1P8_0

VDD_ANA0_1P8_1

VDD_ANA1_1P8_0

VDD_ANA1_1P8_1

VDD_ARM_PLL_0P8

VDD_ANA_0P8_0

VDD_ANA_0P8_1

VDD_USB_0P8

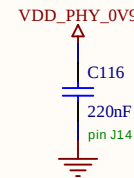
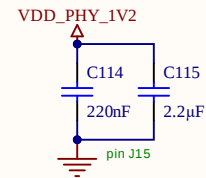
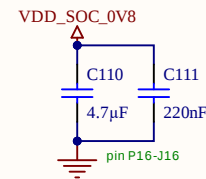
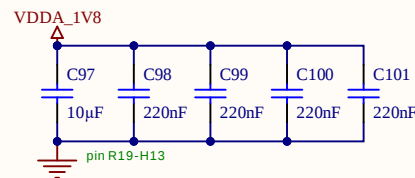
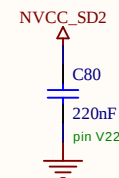
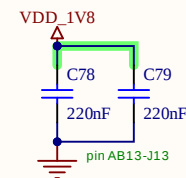
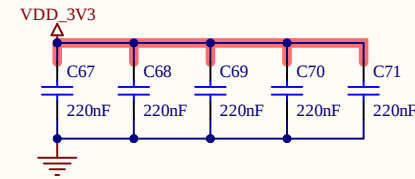
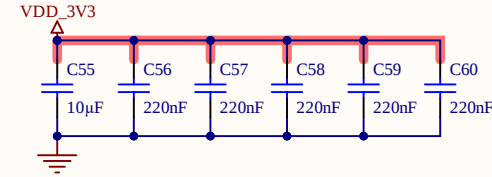
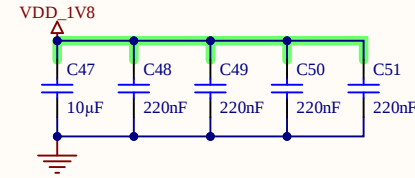
VDD_PCI_0P8

VDD_MIPI_1P2

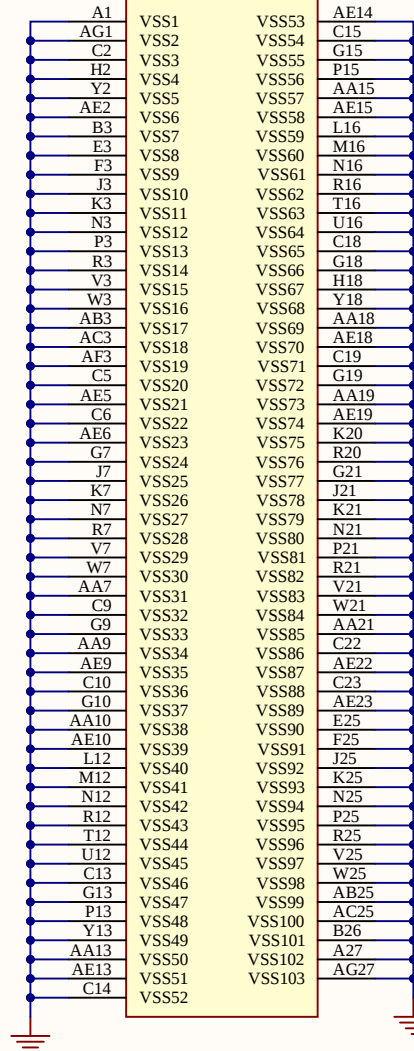
VDD_MIPI_0P9

MIPI_VREG_CAP

NC1



U2N
MIMX8MM6CVTKZAA
i.MX8M Mini - GND



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Title: **POWER**

ID: 3

Date: 6/3/2025

Time: 3:40:09 PM

File: 02-Power.SchDoc

Revision: V4.5

Sheet 3 of 16

Author: Dario Pennisi

RevAuthor: Silvio Navaretti



IMX8Mmini BOOT

Boot Pins:

BOOT_MODE0
BOOT_MODE1

SAI1_TXD7	BT0_CFG15	SAI1_RXD7	BT0_CFG07
SAI1_TXD6	BT0_CFG14	SAI1_RXD6	BT0_CFG06
SAI1_TXD5	BT0_CFG13	SAI1_RXD5	BT0_CFG05
SAI1_TXD4	BT0_CFG12	SAI1_RXD4	BT0_CFG04
SAI1_TXD3	BT0_CFG11	SAI1_RXD3	BT0_CFG03
SAI1_TXD2	BT0_CFG10	SAI1_RXD2	BT0_CFG02
SAI1_TXD1	BT0_CFG09	SAI1_RXD1	BT0_CFG01
SAI1_TXD0	BT0_CFG08	SAI1_RXD0	BT0_CFG00

default -->

0		0		1		0		1		0	
BT_CFG15		BT_CFG14		BT_CFG13		BT_CFG12		BT_CFG11		BT_CFG10	
Infini-Loop 0 - Disable 1 - Enable		Boot device type 001 - SD/eSD 010 - MMC/eMMC						Port Select: 00 - uSDHC1 01 - uSDHC2 10 - uSDHC3		Power Cycle Enable '0' - No power cycle '1' - Enabled	
										SD Loopback Clock Source Sel (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct	

default -->

	0	0	0	1	0	0	1	1
	BT_CFG7	BT_CFG6	BT_CFG5	BT_CFG4	BT_CFG3	BT_CFG2	BT_CFG1	BT_CFG0
SD	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50			Reserved
MMC		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4)			Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC IO VOLTAGE SELECTION For Normal Boot Mode 0 - 3.3V 1 - 1.8V	USDHC IO VOLTAGE SELECTION For Manufacture Mode 0 - 3.3V 1 - 1.8V

Default boot device: eMMC/SDHC3 - BT_CFG[15:0] = 0 010 10 10 0 010 00 1 1

Alternative boot device: uSD/SDHC2 - BT_CFG[15:0] = 0 001 01 10 0 001 00 1 1

BT_CFG13
BT_CFG12
BT_CFG11
BT_CFG10
BT_CFG5
BT_CFG4

BOOT

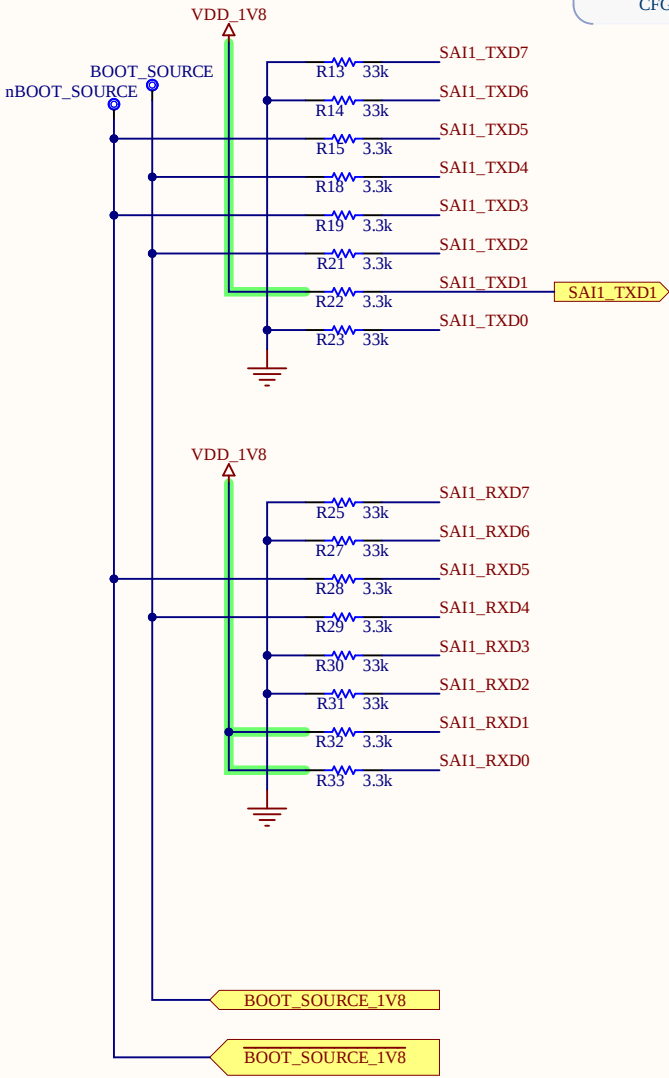
DEV_WAKE	SD1_DATA5
HOST_WAKE	SD1_DATA6
REG_ON	SD1_DATA4
CFG_0	SAI1_RXD0
CFG_1	SAI1_RXD1
CFG_2	SAI1_RXD2
CFG_3	SAI1_RXD3
CFG_4	SAI1_RXD4
CFG_5	SAI1_RXD5
CFG_6	SAI1_RXD6
CFG_7	SAI1_RXD7

BOOT

CFG_8	SAI1_TXD0
CFG_9	SAI1_TXD1
CFG_10	SAI1_TXD2
CFG_11	SAI1_TXD3
CFG_12	SAI1_TXD4
CFG_13	SAI1_TXD5
CFG_14	SAI1_TXD6
CFG_15	SAI1_TXD7

BOOT_MODE1:01

00 - Boot from fuses
01 - Serial Downloader
10 - Internal Boot
11 - Reserved



Title: **BOOT**

ID: 4

Revision: V4.5

Date: 6/3/2025 Time: 3:40:11 PM

Sheet 4 of 16

File: 03-Boot.SchDoc

Author: Dario Pennisi

RevAuthor: Silvio Navaretti



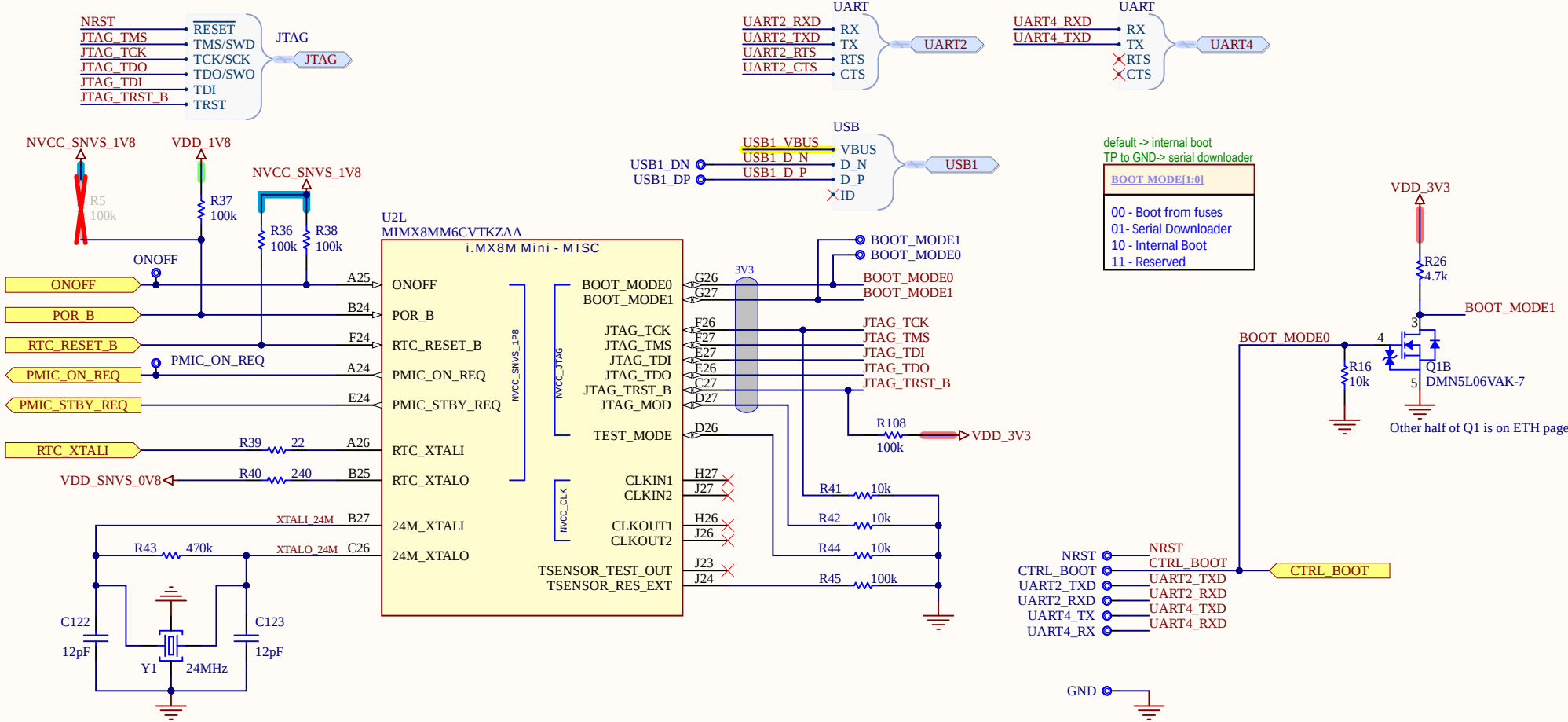
IMX8Mmini MISC

A

B

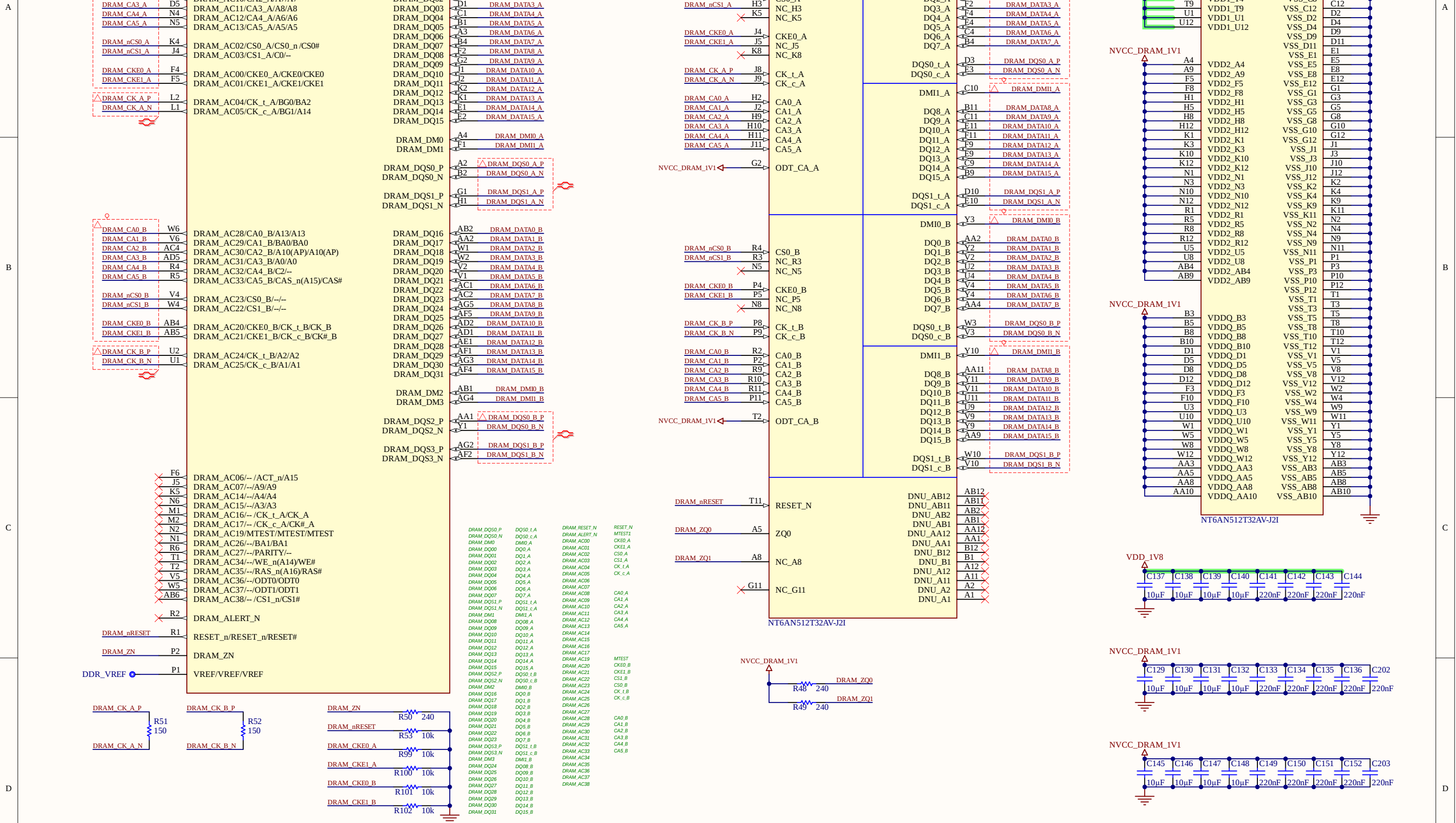
C

D



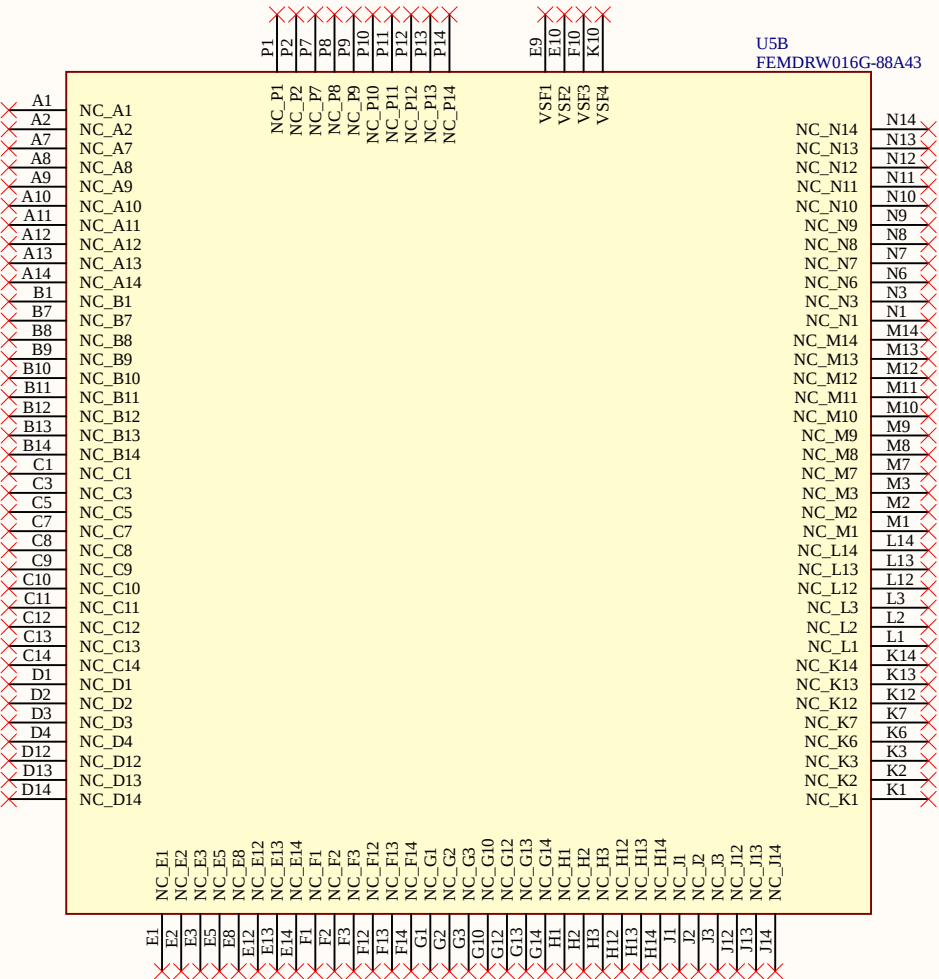
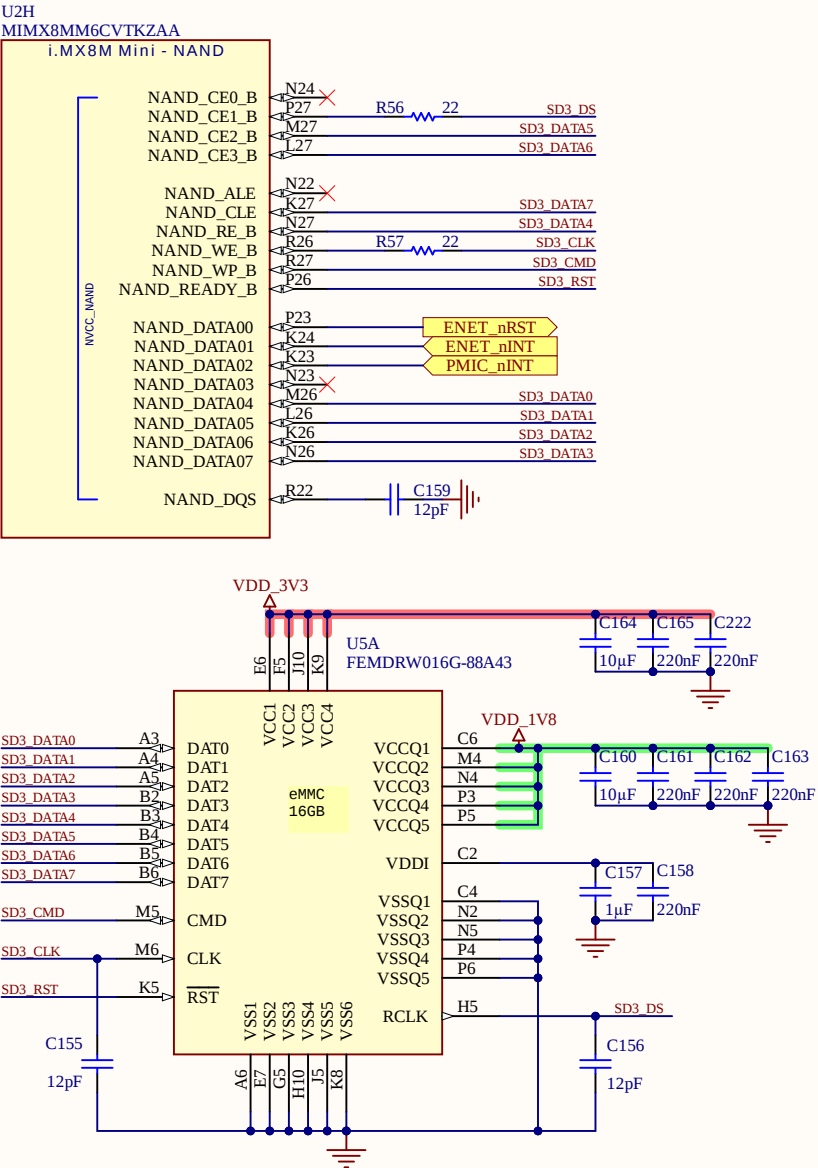
Mfg Tool

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ID: 6		Revision: V4.5				
Date: 6/3/2025 Time: 3:40:15 PM		Sheet 6 of 16				
File: 05-Ddr SchDoc		Author: Dario Pennisi		Rev Author: Silvio Navaretti		

IMX8Mmini Memory



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Title: **MEMORY**

ID: **7**

Date: **6/3/2025** Time: **3:40:17 PM** Sheet **7** of **16**

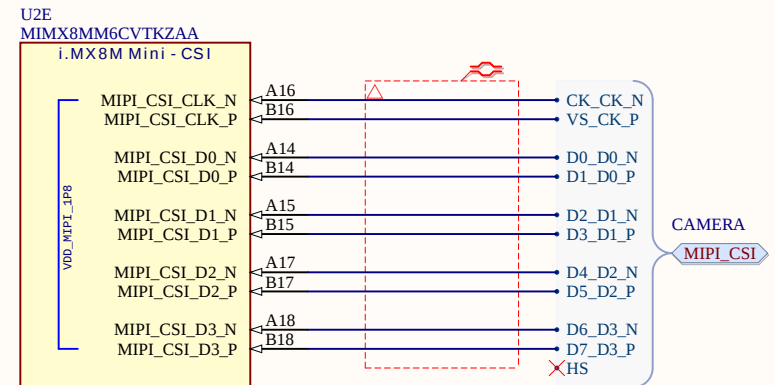
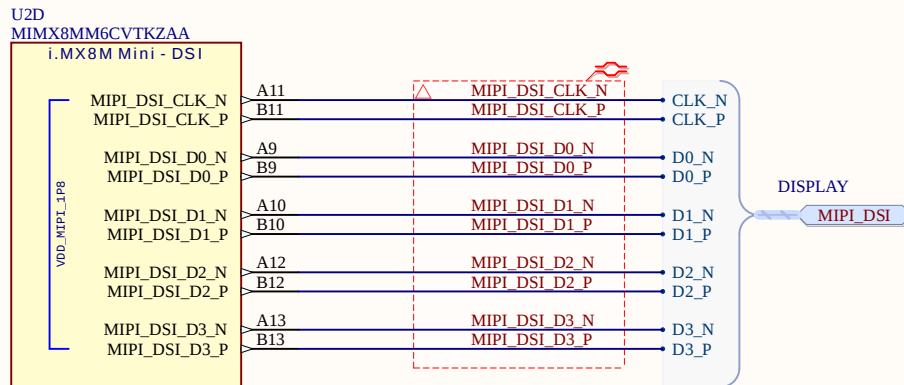
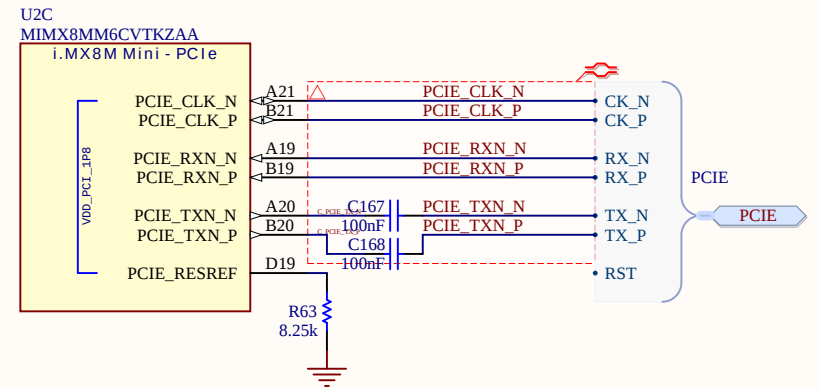
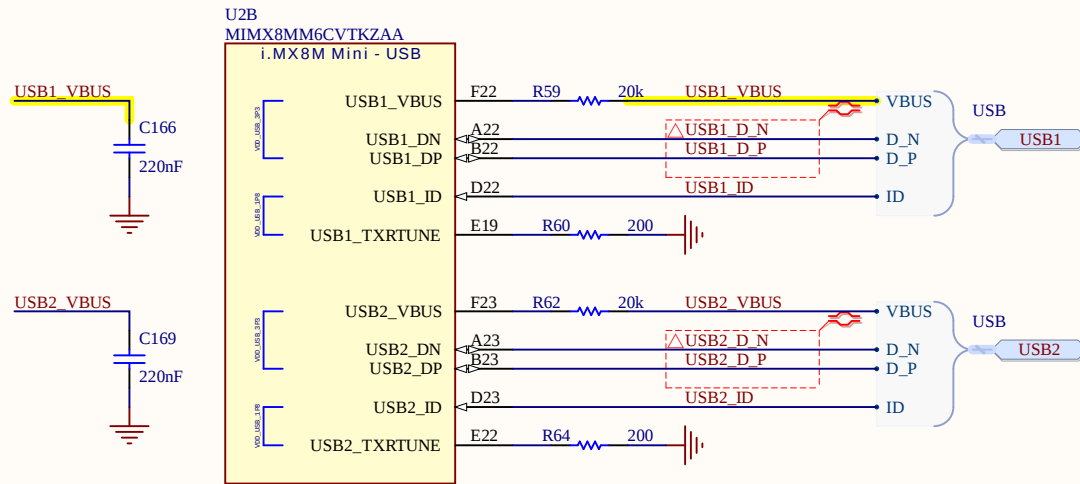
File: **06-Memory.SchDoc**

Revision: **V4.5**

Author: **Dario Pennisi**

RevAuthor: **Silvio Navaretti**

IMX8Mmini PHY



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Title: **PHY**

ID: **8**

Date: **6/3/2025**

File: **07-Phy.SchDoc**

Revision: **V4.5**

Time: **3:40:19 PM**

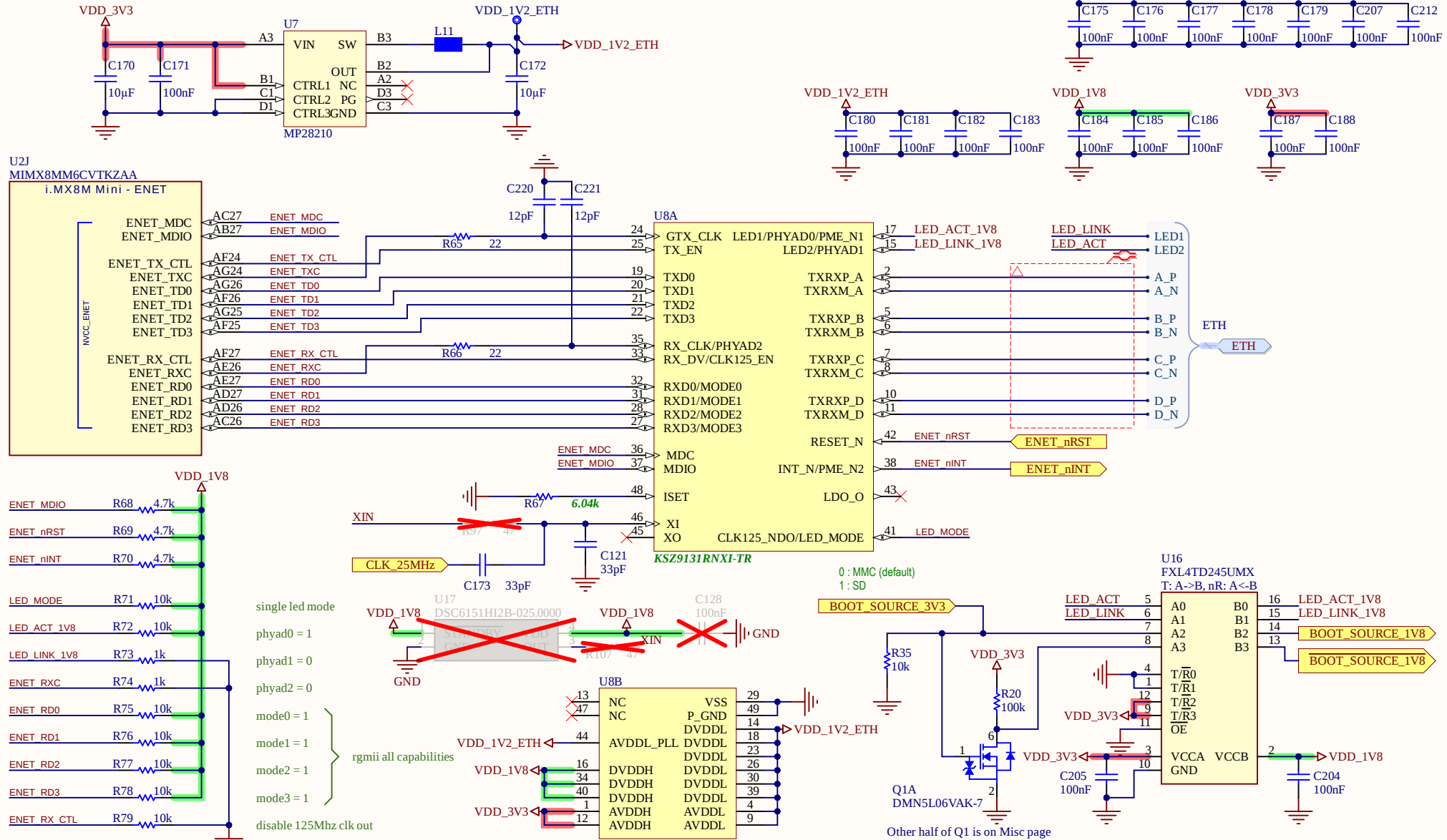
Sheet **8** of **16**

Author: **Dario Pennisi**

RevAuthor: **Silvio Navaretti**



IMX8Mmini ETH



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Title: **ETHERNET**

ID: **9**

Revision: **V4.5**

Date: **6/3/2025**

Time: **3:40:20 PM**

Sheet **9** of **16**

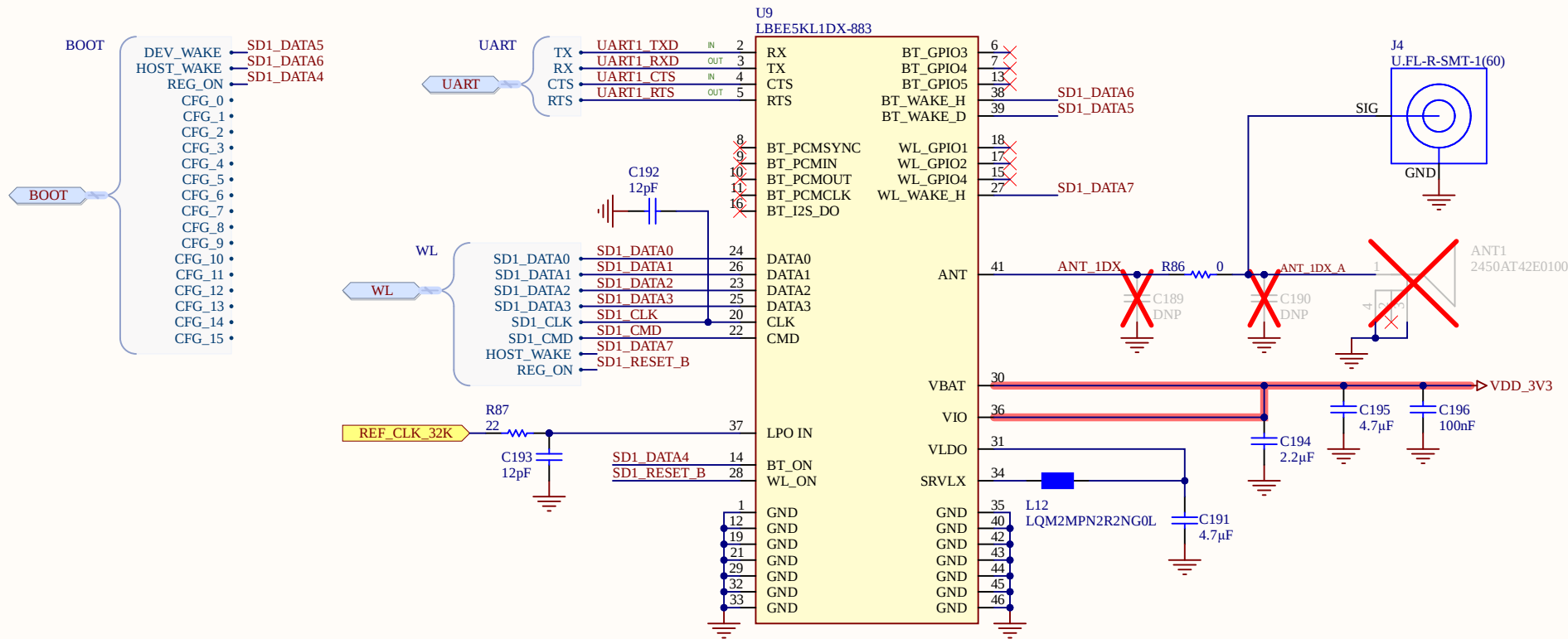
File: **08-Eth.SchDoc**

Author: **Dario Pennisi**

RevAuthor: **Silvio Navaretti**



IMX8Mmini WL/BT



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Title: **WLBT**

ID: **11**

Date: **6/3/2025**

File: **10-WLBT.SchDoc**

Revision: **V4.5**

Time: **3:40:22 PM**

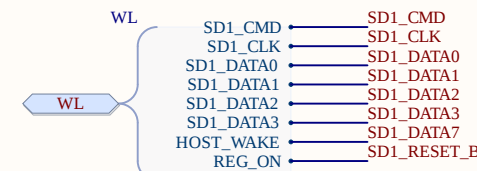
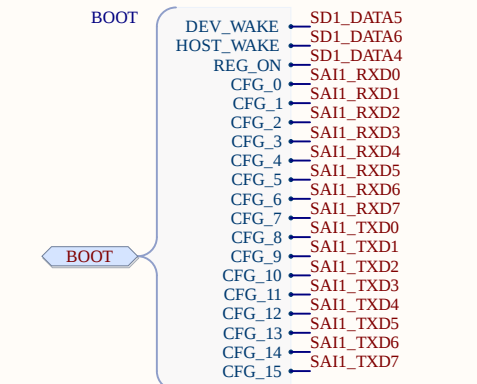
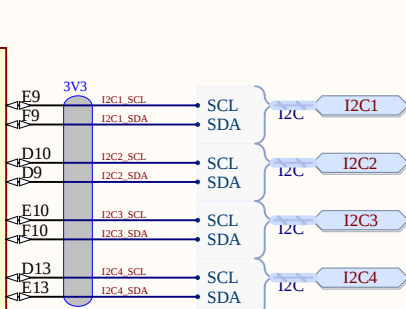
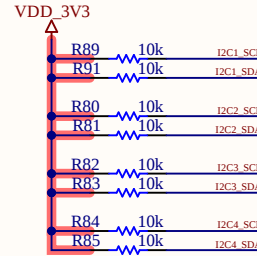
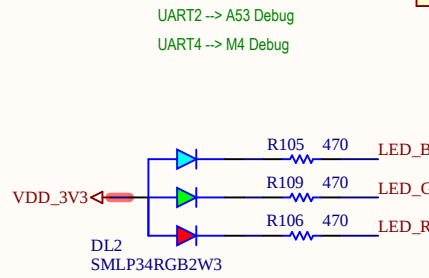
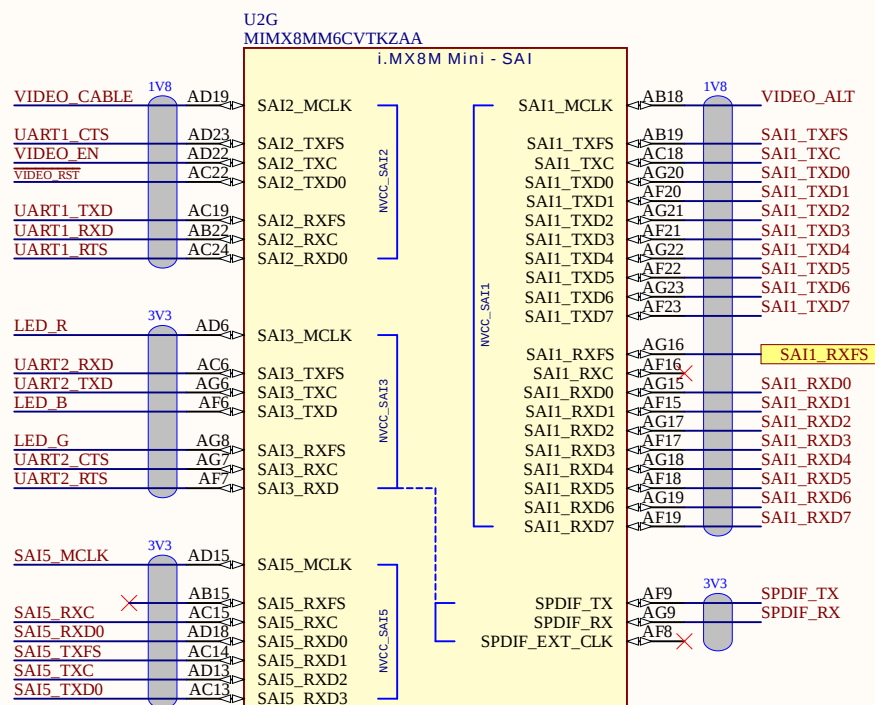
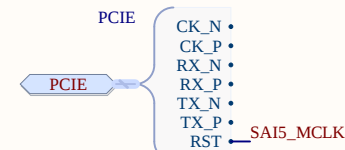
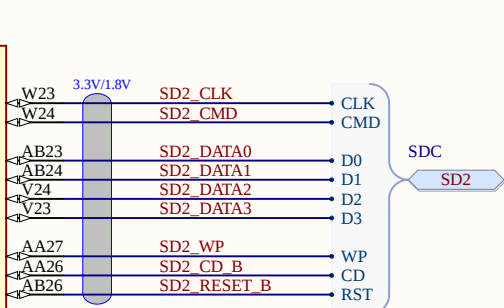
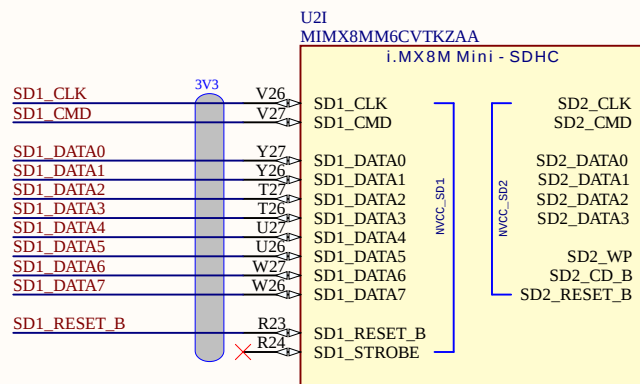
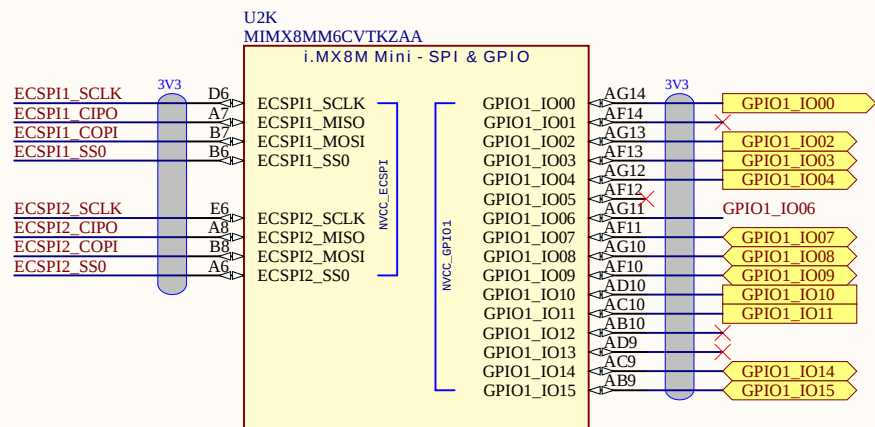
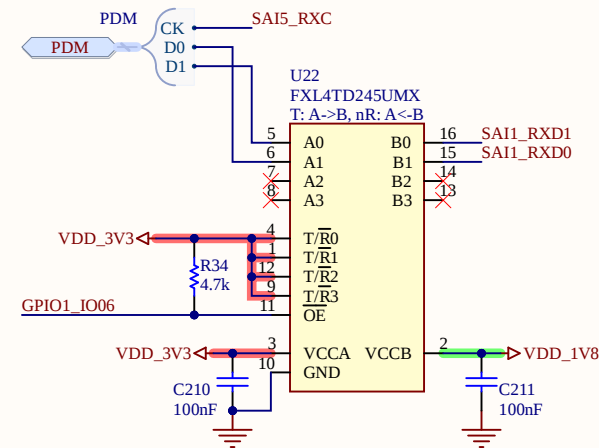
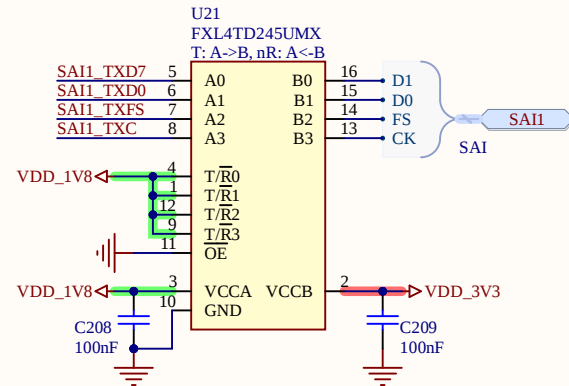
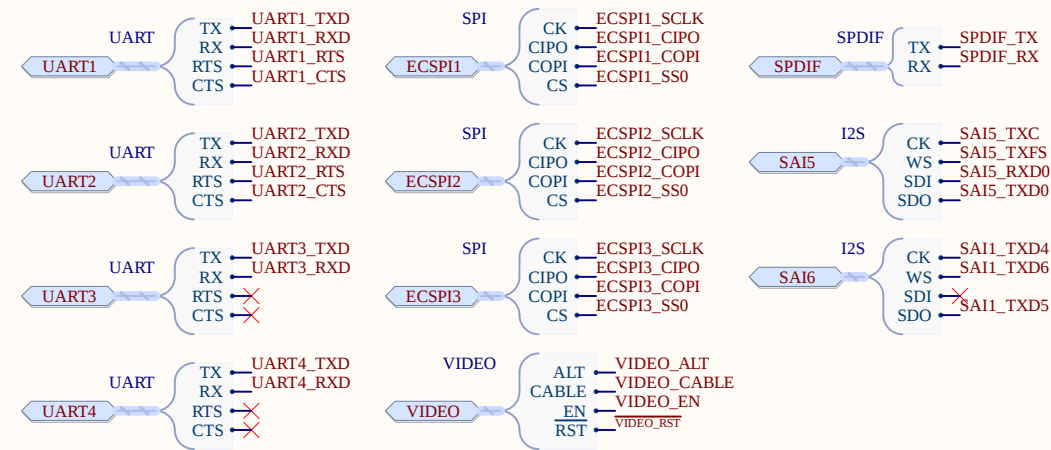
Sheet **10** of **16**

Author: **Dario Pennisi**

RevAuthor: **Silvio Navaretti**



IMX8Mmini IO



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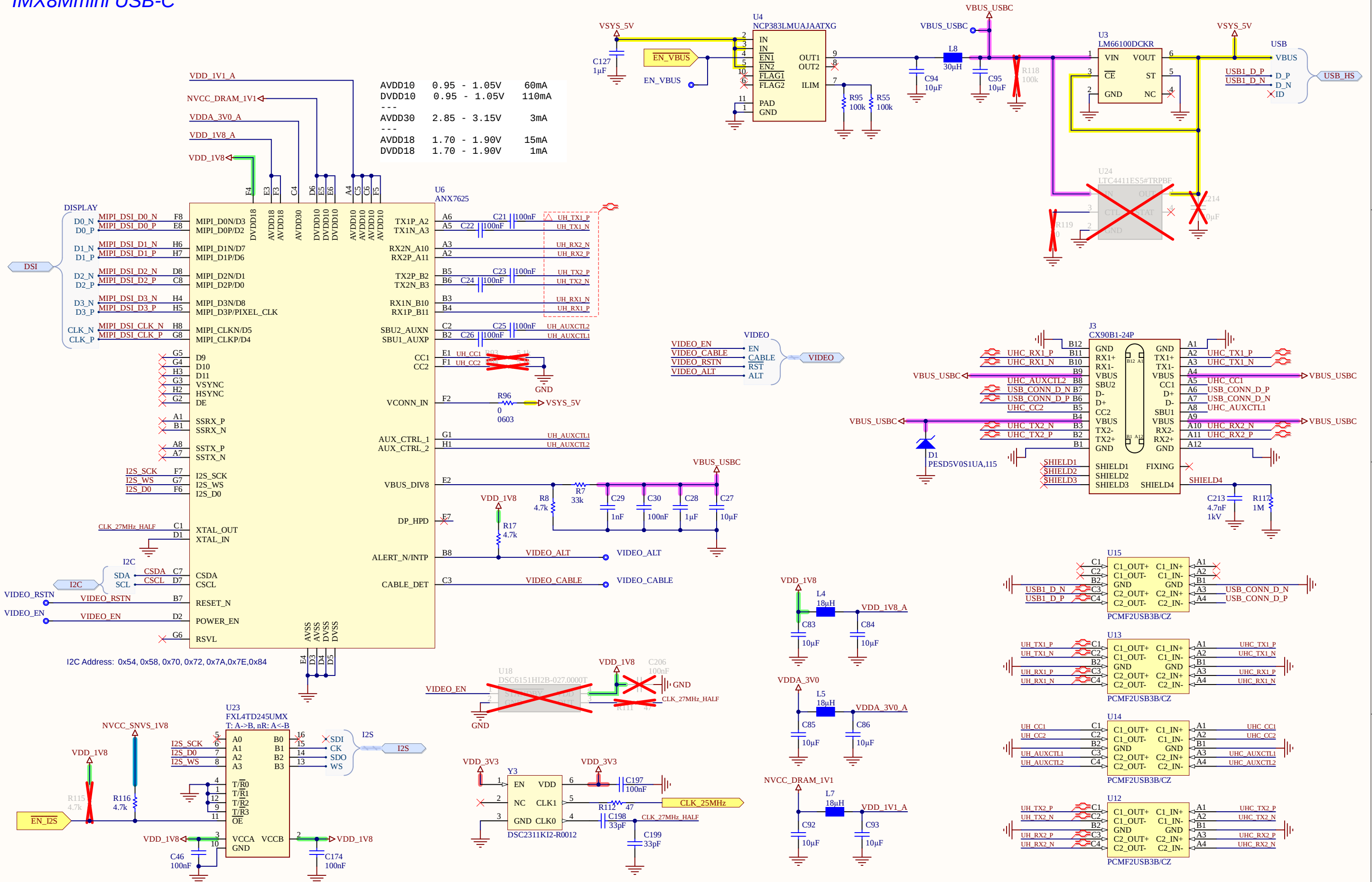
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Title: IO		Revision: V4.5	
ID: 10		Sheet 11 of 16	
Date: 6/3/2025 Time: 3:40:24 PM		Author: Dario Pennisi	
File: 09-IO.SchDoc		RevAuthor: Silvio Navaretti	



IMX8Mmini USB-C



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Title: VIDEO

ID: 12

Date: 6/3/2025

File: 11-Video.SchDoc

Revision: V4.5

Time: 3:40:26 PM

Sheet 12 of 16

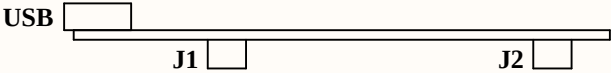
Author: Dario Pennisi



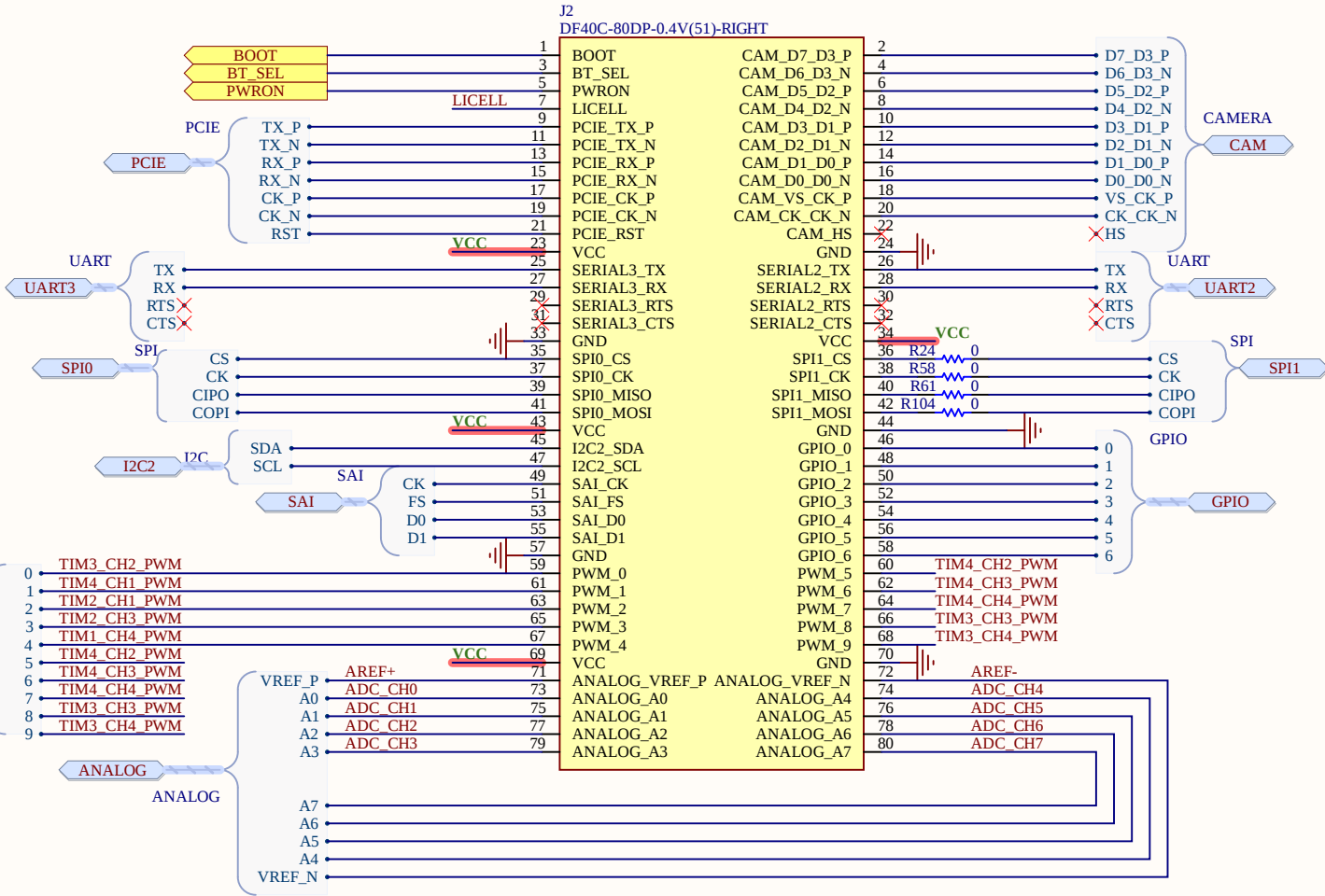
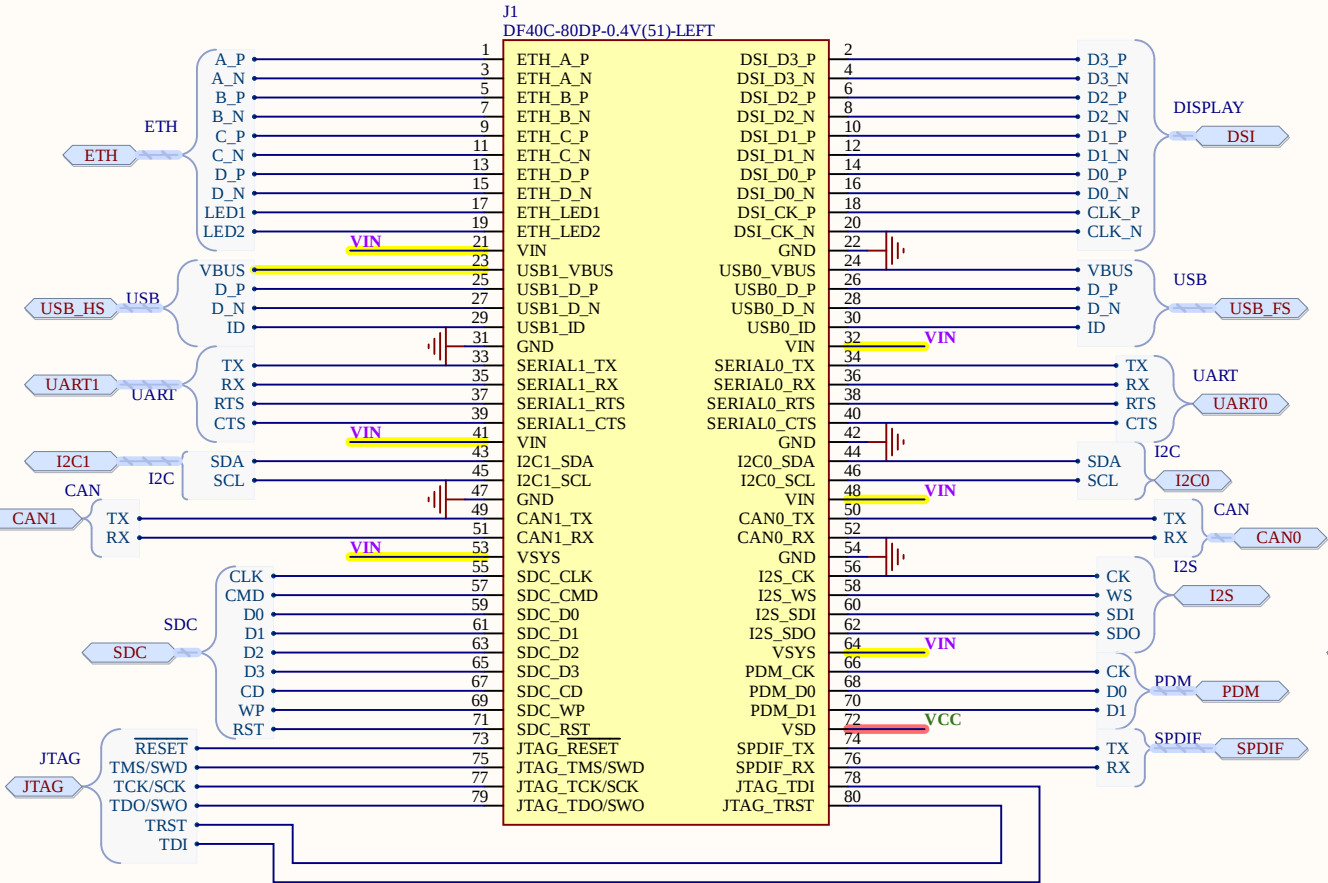
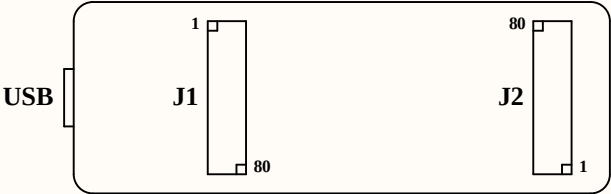
RevAuthor: Silvio Navaretti

IMX8Mmini Connectors

Board side view:



Board BOTTOM view:

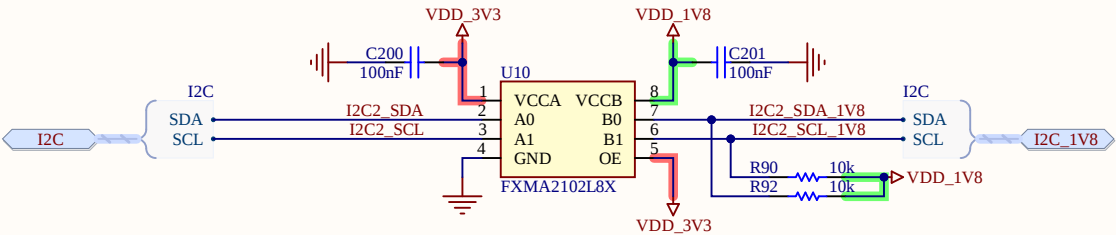


POWER NETS TABLE

NET	TYPE	RANGES	DESCRIPTION
VIN	PORTENTA INPUT	4.1V to 6V.	Default 3.3V, PMIC (U1) programmable output.
VCC	PORTENTA OUTPUT	1.1V to 3.3V in steps, max 1A.	Default 3.3V, PMIC (U1) programmable output.
LICELL	PORTENTA INPUT	Coinc cell max 3.6V, max 46uA.	Max 4uA with PMIC (U1) in coin cell mode, max 46uA with PMIC in standby/suspend mode.

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IMX8Mmini LevelShifter

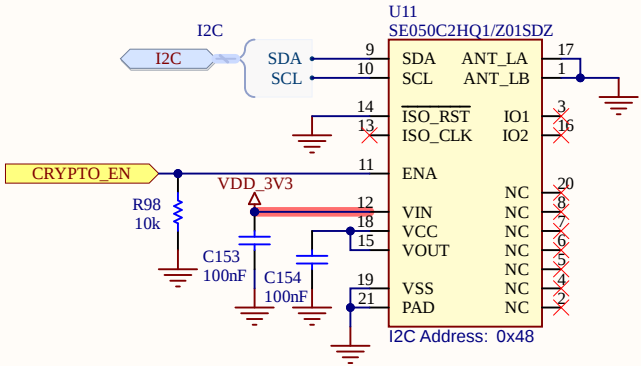


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Title: LEVEL SHIFTER				
ID: 14	Revision: V4.5			
Date: 6/3/2025	Time: 3:40:29 PM	Sheet 14 of 16		
File: 13-LevelShifter.SchDoc		Author: Dario Pennisi	RevAuthor: Silvio Navaretti	



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Title: CRYPTO					
ID: 16	Revision: V4.5				
Date: 6/3/2025	Time: 3:40:33 PM	Sheet 16 of 16			
File: 15-CRYPTO.SchDoc		Author: Dario Pennisi	RevAuthor: Silvio Navaretti		