

Power MOSFET



N-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

PRODUCT SUMMARY	
V _{DS} (V)	600
R _{DS(on)} (Ω)	V _{GS} = 10 V 2.2
Q _g max. (nC)	31
Q _{gs} (nC)	4.6
Q _{gd} (nC)	17
Configuration	Single

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRFBC30PbF
Lead (Pb)-free and halogen-free	IRFBC30PbF-BE3

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	600	V	
Gate-source voltage		V _{GS}	± 20		
Continuous drain current	V _{GS} at 10 V	I _D	T _C = 25 °C	3.6	A
			T _C = 100 °C	2.3	
Pulsed drain current ^a		I _{DM}	14		
Linear derating factor			0.59	W/°C	
Single pulse avalanche energy ^b		E _{AS}	290	mJ	
Repetitive avalanche current ^a		I _{AR}	3.6	A	
Repetitive avalanche energy ^a		E _{AR}	7.4	mJ	
Maximum power dissipation	T _C = 25 °C	P _D	74	W	
Peak diode recovery dV/dt ^c		dV/dt	3.0	V/ns	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) ^d	For 10 s		300		
Mounting torque	6-32 or M3 screw		10	lbf · in	
			1.1	N · m	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V_{DD} = 50 V, starting T_J = 25 °C, L = 41 mH, R_g = 25 Ω, I_{AS} = 3.6 A (see fig. 12)
- I_{SD} ≤ 3.6 A, di/dt ≤ 60 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C
- 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	1.7	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.62	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	100	μA
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	500	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 2.2\text{ A}^b$	-	-	2.2	Ω
Forward transconductance	g_{fs}	$V_{DS} = 100\text{ V}, I_D = 2.2\text{ A}^b$		2.5	-	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5		-	660	-	μF
Output capacitance	C_{oss}			-	86	-	
Reverse transfer capacitance	C_{rss}			-	19	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 3.6\text{ A}, V_{DS} = 360\text{ V}$, see fig. 6 and 13 ^b	-	-	31	nC
Gate-source charge	Q_{gs}			-	-	4.6	
Gate-drain charge	Q_{gd}			-	-	17	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 3.6\text{ A}, R_g = 12\text{ }\Omega, R_D = 82\text{ }\Omega$, see fig. 10 ^b		-	11	-	ns
Rise time	t_r			-	13	-	
Turn-off delay time	$t_{d(off)}$			-	35	-	
Fall time	t_f			-	14	-	
Gate input resistance	R_g	$f = 1\text{ MHz}$, open drain		0.5	-	4.9	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	3.6	A
Pulsed diode forward current ^a	I_{SM}			-	-	14	
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 3.6\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.6	V
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 3.6\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	370	810	ns
Body diode reverse recovery charge	Q_{rr}			-	2.0	4.2	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

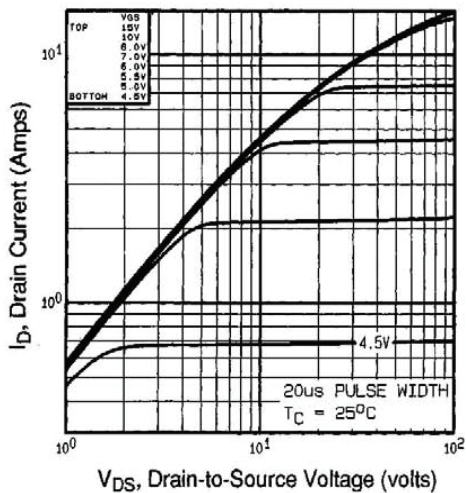


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

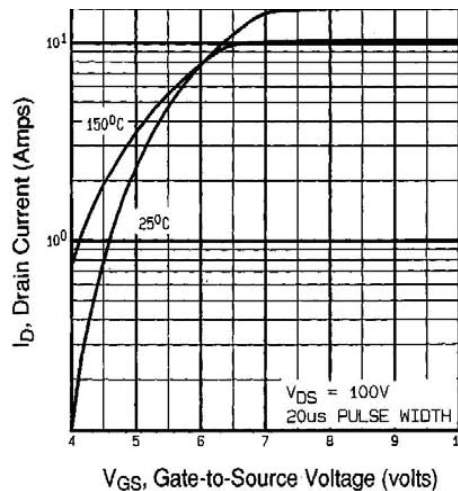


Fig. 3 - Typical Transfer Characteristics

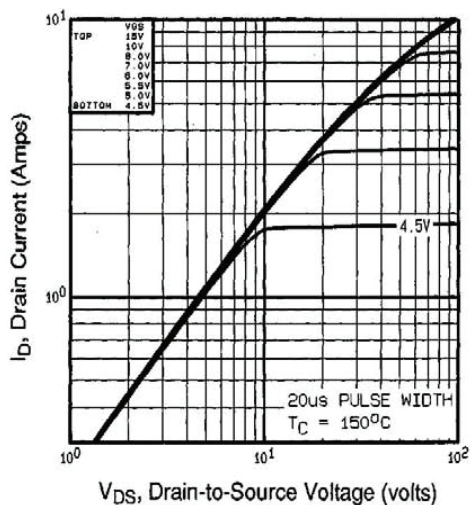


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

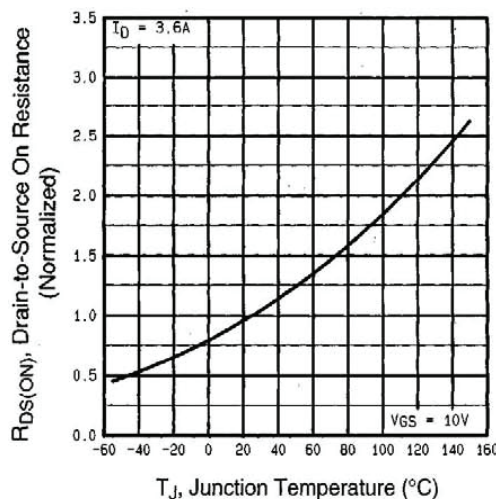


Fig. 4 - Normalized On-Resistance vs. Temperature

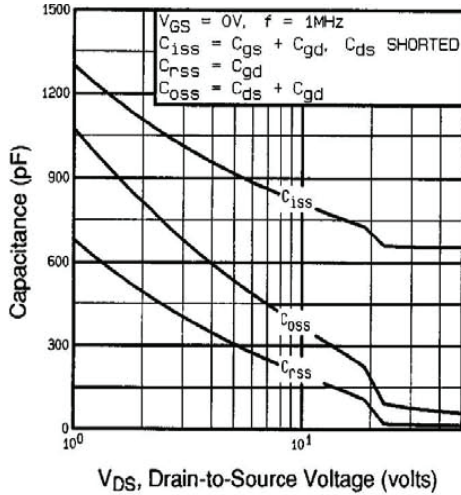


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

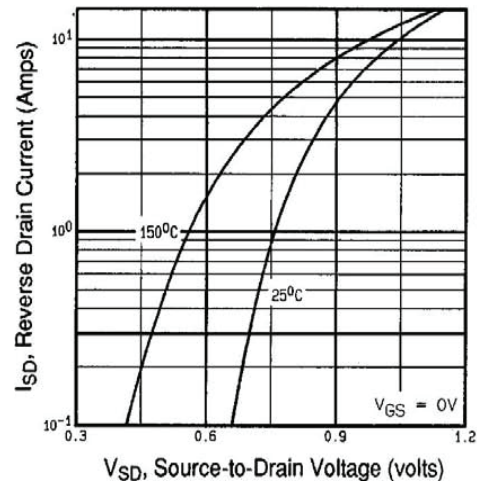


Fig. 7 - Typical Source-Drain Diode Forward Voltage

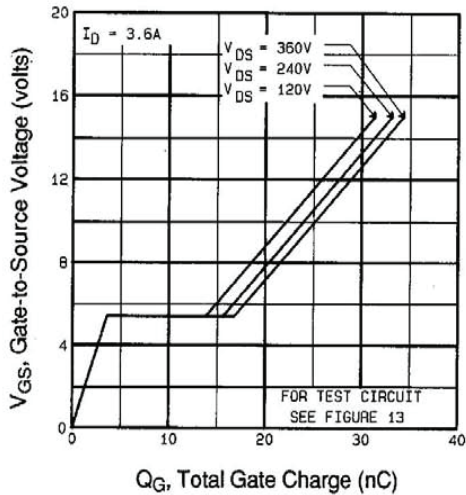


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

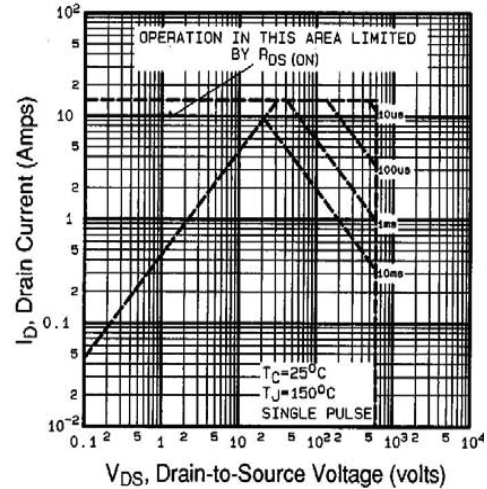


Fig. 8 - Maximum Safe Operating Area

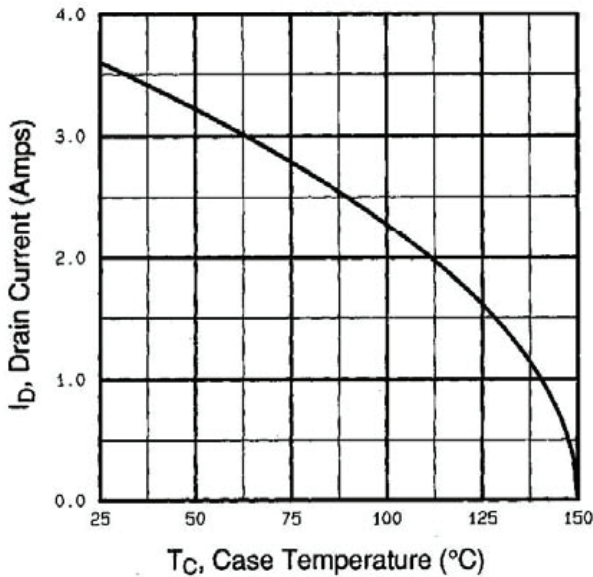


Fig. 9 - Maximum Drain Current vs. Case Temperature

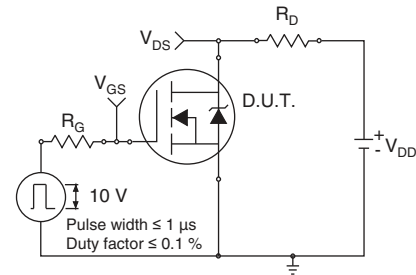


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

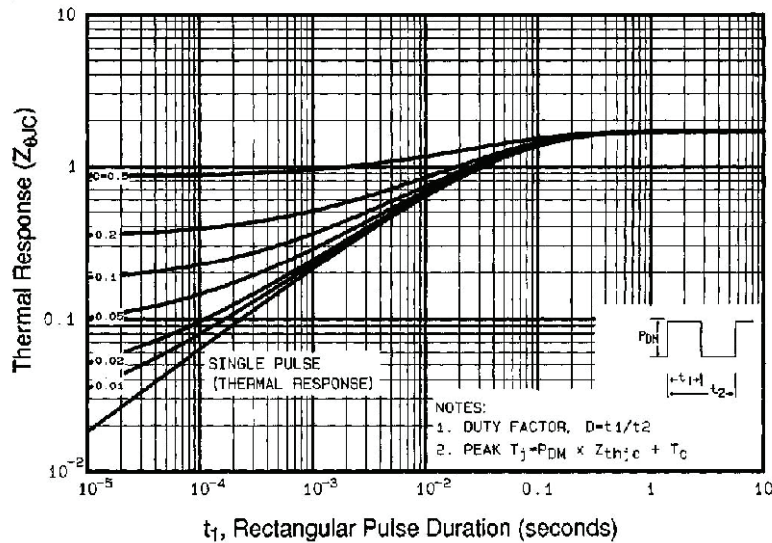


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

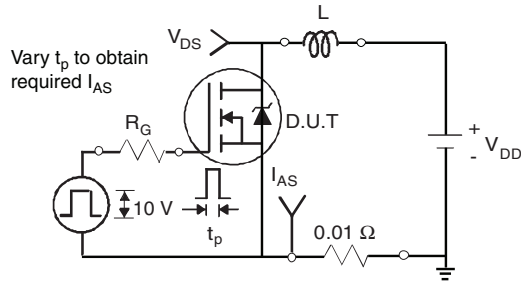


Fig. 12a - Unclamped Inductive Test Circuit

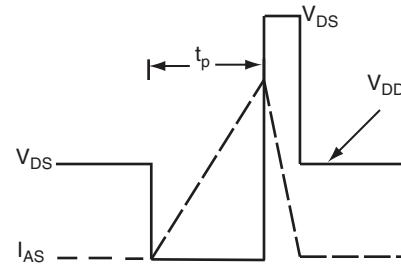


Fig. 12b - Unclamped Inductive Waveforms

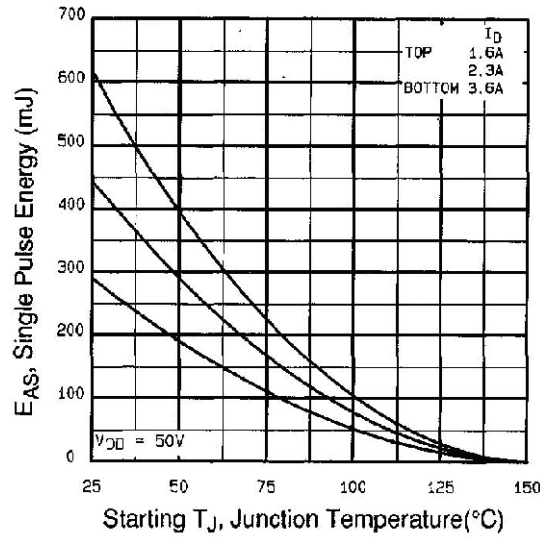


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

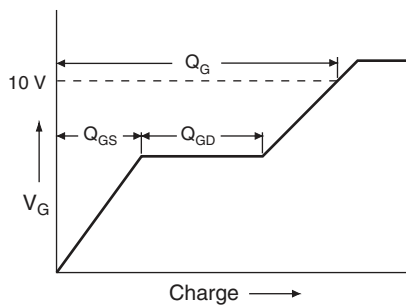


Fig. 13a - Basic Gate Charge Waveform

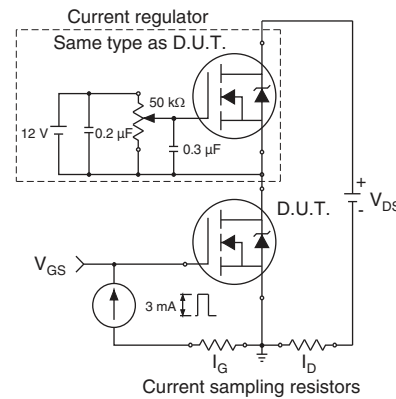
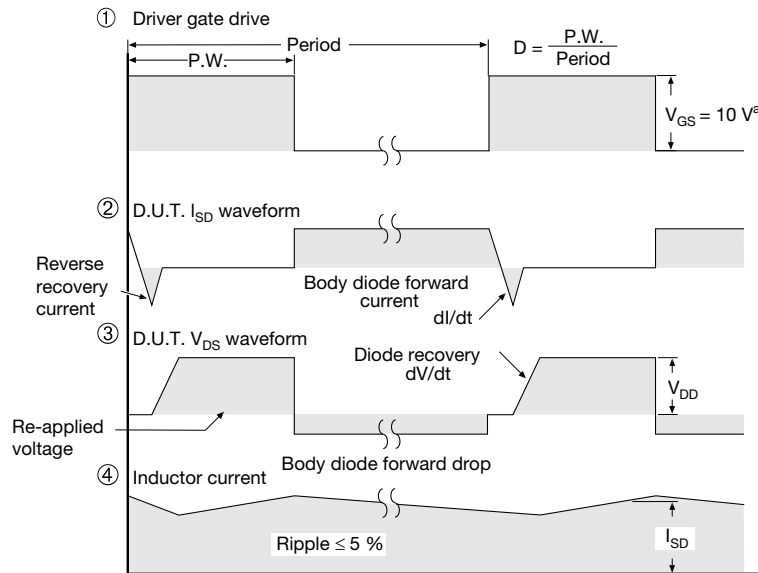
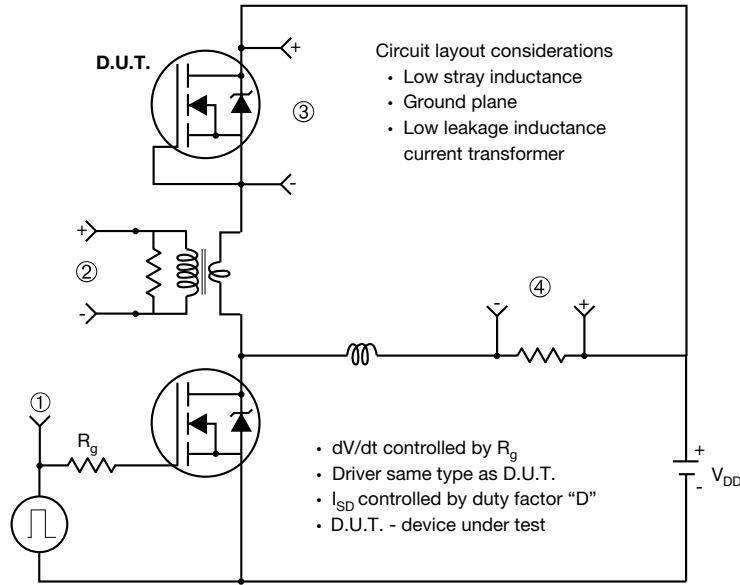


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

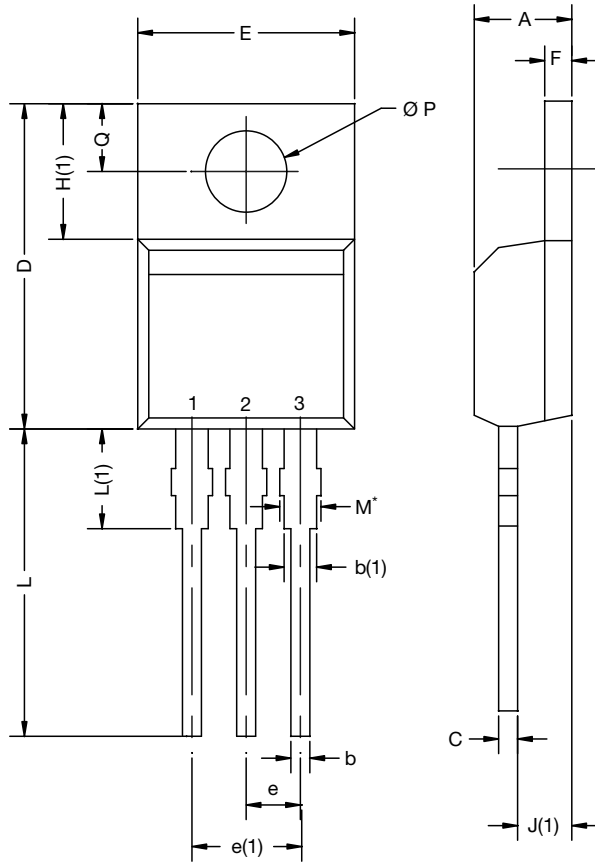
a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: E21-0621-Rev. D, 04-Nov-2021
DWG: 6031

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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