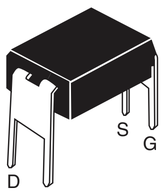
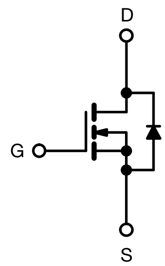
# Power MOSFET

HVMDIP




N-Channel MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | 200 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = 10 V | 0.80 |
| $Q_g$ (Max.) (nC) | 14 | |
| $Q_{gs}$ (nC) | 3.0 | |
| $Q_{gd}$ (nC) | 7.9 | |
| Configuration | Single | |

## FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- For automatic insertion
- End stackable
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

## DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

| ORDERING INFORMATION | |
|---|---|
| Package | HVMDIP |
| Lead (Pb)-free | IRFD220PbF |

**ABSOLUTE MAXIMUM RATINGS** ($T_A$ = 25 °C, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-source voltage | | | $V_{DS}$ | 200 | V |
| Gate-source voltage | | | $V_{GS}$ | ± 20 | |
| Continuous drain current | $V_{GS}$ at 10 V | $T_A$ = 25 °C | $I_D$ | 0.80 | A |
| | | $T_A$ = 100 °C | | 0.50 | |
| Pulsed drain current [a] | | | $I_{DM}$ | 6.4 | |
| Linear derating factor | | | | 0.0083 | W/°C |
| Single pulse avalanche energy [b] | | | $E_{AS}$ | 260 | mJ |
| Repetitive avalanche current [a] | | | $I_{AR}$ | 5.2 | A |
| Repetitive avalanche energy [a] | | | $E_{AR}$ | 0.10 | mJ |
| Maximum power dissipation | $T_A$ = 25 °C | | $P_D$ | 1.0 | W |
| Peak diode recovery dV/dt [c] | | | dV/dt | 5.0 | V/ns |
| Operating junction and storage temperature range | | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Soldering recommendations (peak temperature) | For 10 s | | | 300[d] | |

**Notes**

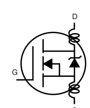
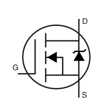
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. $V_{DD}$ = 50 V, starting $T_J$ = 25 °C, L = 152 mH, $R_g$ = 25 Ω, $I_{AS}$ = 1.6 A (see fig. 12)

c. $I_{SD} \leq 5.2$ A, dI/dt ≤ 95 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C

d. 1.6 mm from case

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | 120 | °C/W |

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 200 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | | - | 0.29 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = 250 μA | | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 20 V | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 200 V, $V_{GS}$ = 0 V | | - | - | 25 | μA |
| | | $V_{DS}$ = 160 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V | $I_D$ = 0.48 A[b] | - | - | 0.80 | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 50 V, $I_D$ = 0.48 A[b] | | 0.60 | - | - | S |
| **Dynamic** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1.0 MHz, see fig. 5 | | - | 260 | - | pF |
| Output Capacitance | $C_{oss}$ | | | - | 100 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | - | 30 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 10 V | $I_D$ = 4.8 A, $V_{DS}$ = 160 V, see fig.6 and 13[b] | - | - | 14 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | - | - | 3.0 | |
| Gate-Drain Charge | $Q_{gd}$ | | | - | - | 7.9 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 100 V, $I_D$ = 4.8 A, $R_g$ = 18 Ω, $R_D$ = 19 Ω, see fig. 10[b] | | - | 7.2 | - | ns |
| Rise Time | $t_r$ | | | - | 22 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 19 | - | |
| Fall Time | $t_f$ | | | - | 13 | - | |
| Internal Drain Inductance | $L_D$ | Between lead, 6 mm (0.25") from package and center of die contact |  | - | 4.0 | - | nH |
| Internal Source Inductance | $L_S$ | | | - | 6.0 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode |  | - | - | 0.80 | A |
| Pulsed Diode Forward Current[a] | $I_{SM}$ | | | - | - | 6.4 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 0.80 A, $V_{GS}$ = 0 V[b] | | - | - | 1.8 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = 4.8 A, dI/dt = 100 A/μs[b] | | - | 150 | 300 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | | - | 0.91 | 1.8 | μC |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

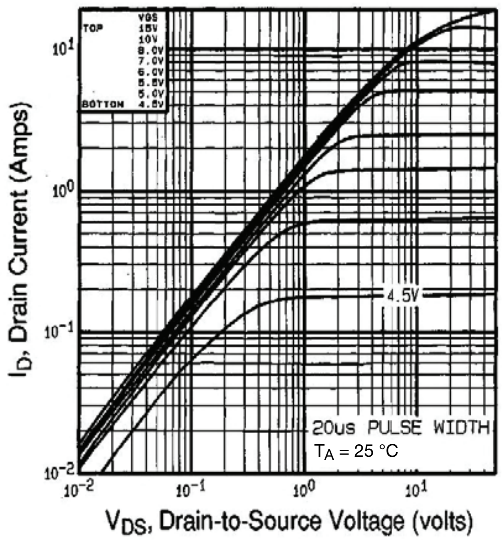



**Fig. 1 - Typical Output Characteristics, $T_A$ = 25 °C**

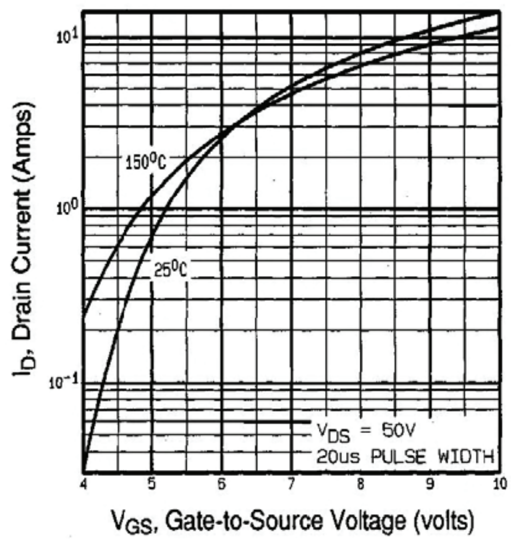



**Fig. 2 - Typical Transfer Characteristics**

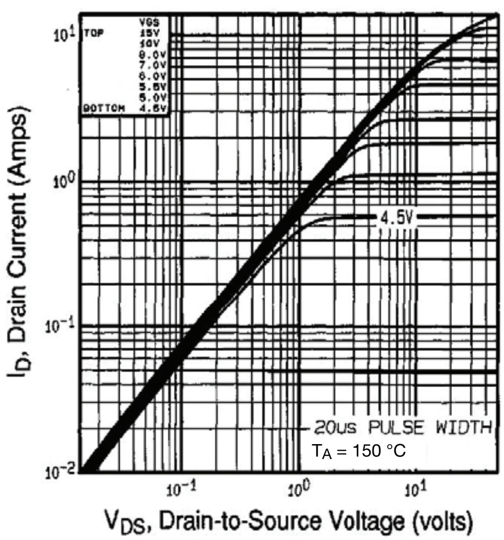



**Fig. 1 - Typical Output Characteristics, $T_A$ = 150 °C**

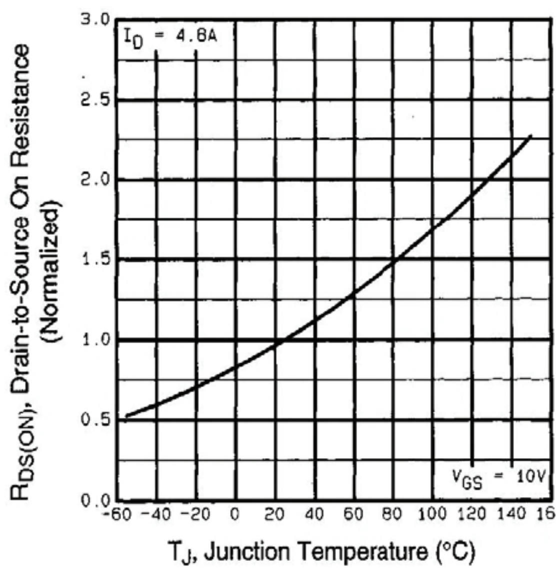



**Fig. 3 - Normalized On-Resistance vs. Temperature**


For technical questions, contact: hvm@vishay.com

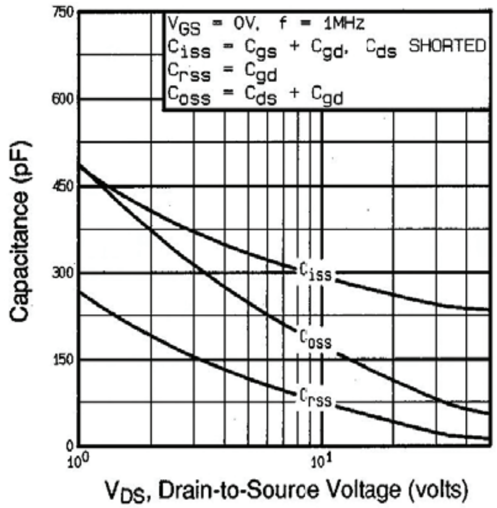



Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

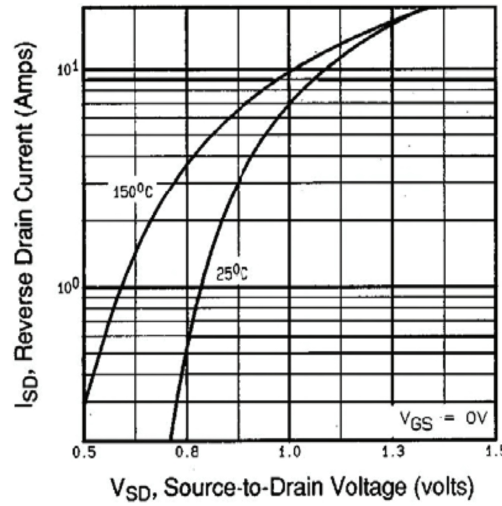



Fig. 6 - Typical Source-Drain Diode Forward Voltage

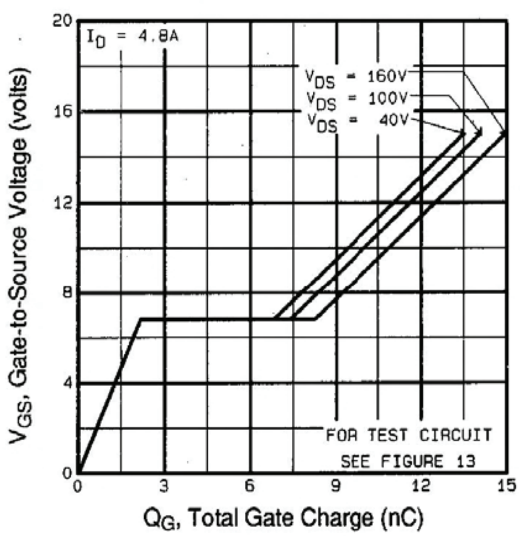



Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage

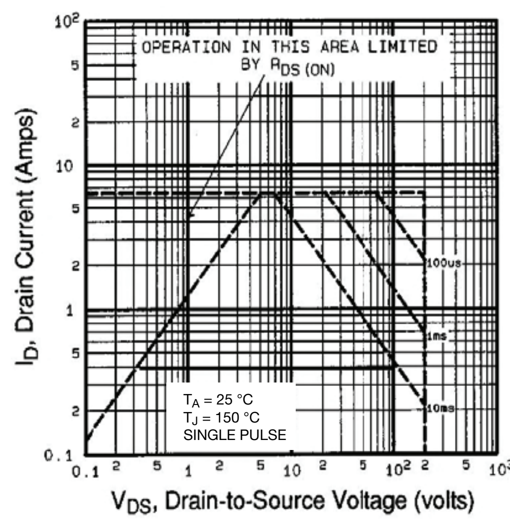



Fig. 7 - Maximum Safe Operating Area

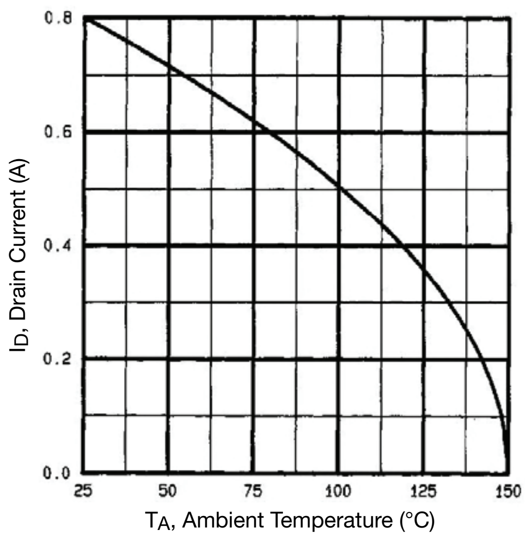



**Fig. 8 - Maximum Drain Current vs. Ambient Temperature**

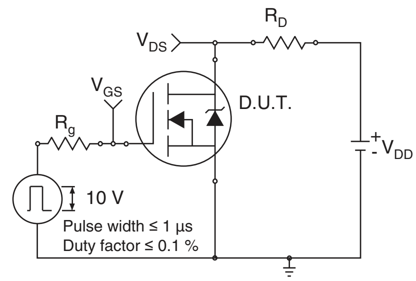



**Fig. 10a - Switching Time Test Circuit**

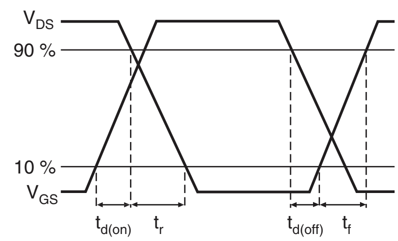



**Fig. 10b - Switching Time Waveforms**

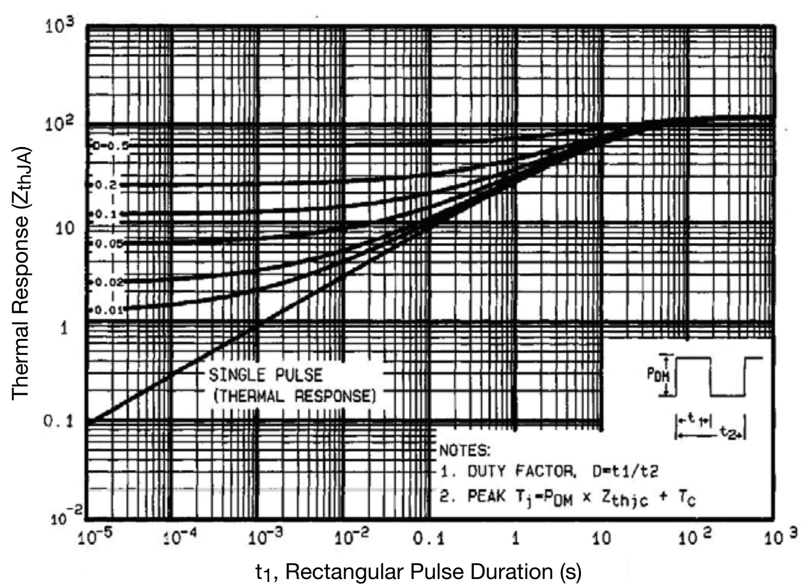
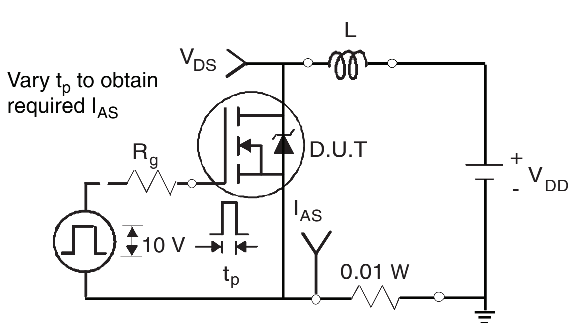



**Fig. 9 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient**

**Fig. 12a - Unclamped Inductive Test Circuit**



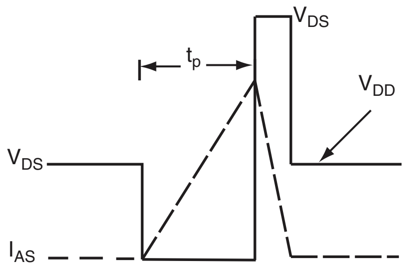



**Fig. 12b - Unclamped Inductive Waveforms**

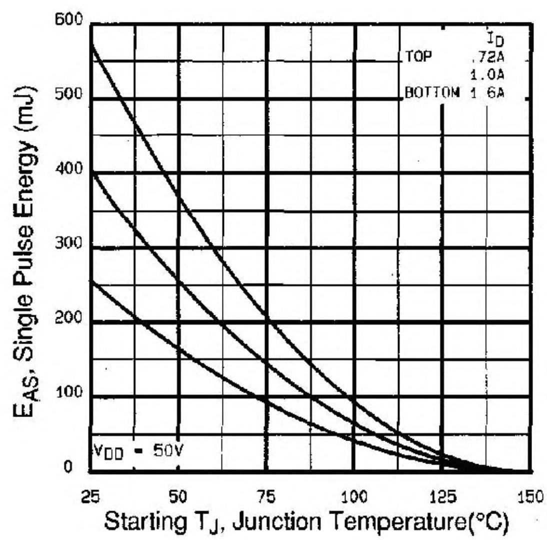



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

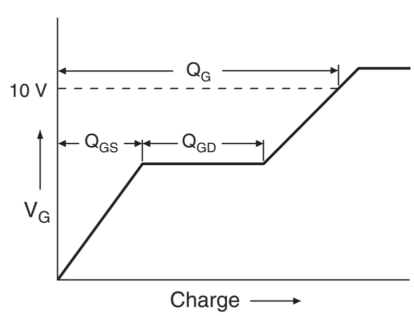



**Fig. 13a - Basic Gate Charge Waveform**

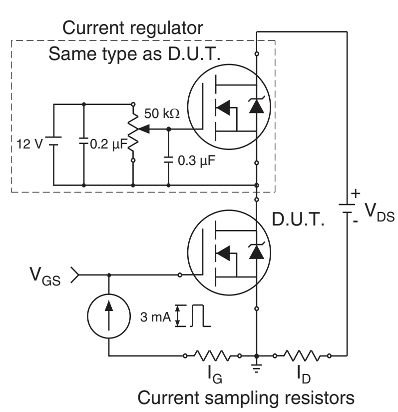



**Fig. 13b - Gate Charge Test Circuit**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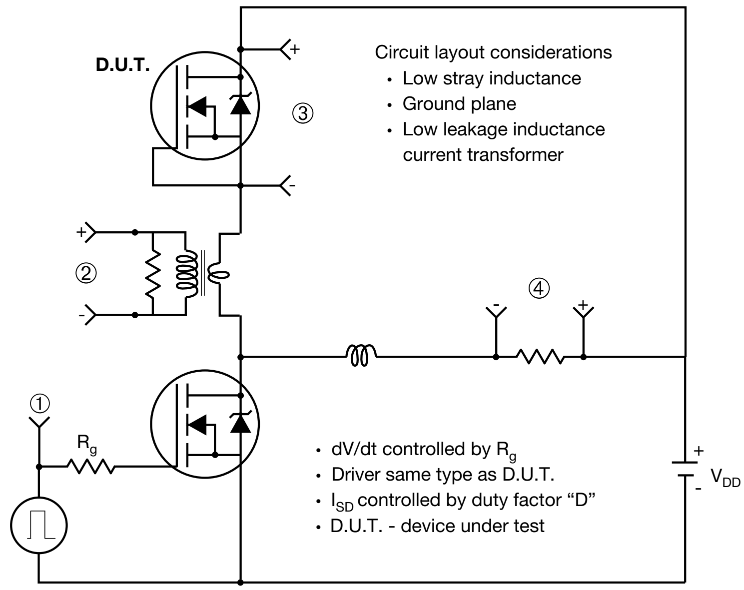
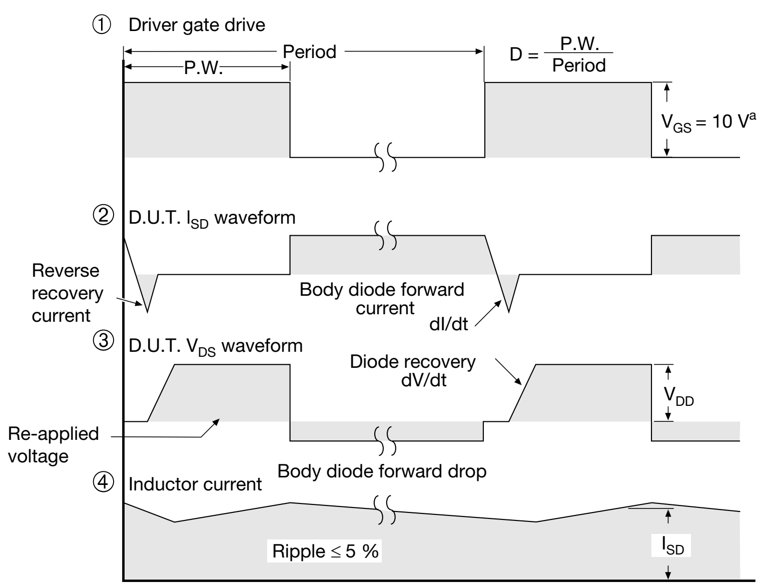
**Peak Diode Recovery dV/dt Test Circuit**




**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 10 - For N-Channel**

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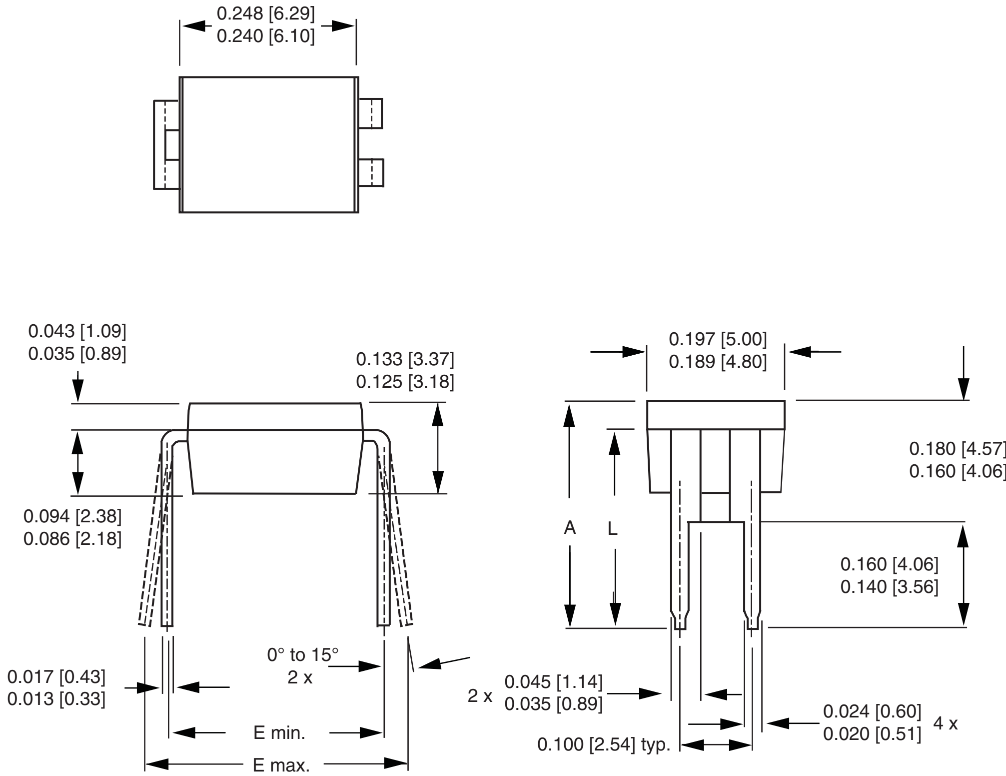
**HVM DIP** (High voltage)




| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 0.310 | 0.330 | 7.87 | 8.38 |
| E | 0.300 | 0.425 | 7.62 | 10.79 |
| L | 0.270 | 0.290 | 6.86 | 7.36 |
| ECN: X10-0386-Rev. B, 06-Sep-10<br>DWG: 5974 | | | | |

**Note**

1. Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.

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