Zeppelinstrasse 19 D-82205 Gilching Fon +49-8105-778090 *info@lcd-module.de* http://www.lcd-module.com

SPECIFICATION

CUSTOMER :

MODULE NO.: EA TFT050-84BTS

APPROVED BY: (FOR CUSTOMER USE ONLY)	PCB VERSION: DATA:

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
			葉虹蘭
ISSUED DATE: 2023/02/14			

Content

1. Summary

EA TFT050-84BTS is a TN transmissive type color active matrix TFT liquid crystal display that use amorphous silicon TFT as switching devices. This module is a composed of a TFT_LCD module, It is usually designed for industrial application and this module follows RoHS. Touchpanel controller ILI2130 is included.

1.1. Accessories

ZIF connector for display, bottom contact	**EA WF050-40S**
ZIF connector for display, top contact	**EA WF050-40ST**
ZIF connector for touch panel, top contact	**EA WF050-10T**

2. General Specifications

Item	Dimension	Unit
Size	5.0	inch
Dot Matrix	800× 3(RGB) × 480	dots
Module dimension	120.7(W) ×75.8(H) ×4.475mm	mm
Active area	108(W) ×64.8 (H) mm	mm
Dot pitch	0.135(W) ×0.135(H) mm	mm
LCD type	TFT, Normally White, Transmissive	
View Direction	12 o'clock	
Gray Scale Inversion Direction	6 o'clock	
Aspect Ratio	5:3	
Backlight Type	LED, Normally White	
Brightness	750 cd/m² (typ.)	
PCAP IC	ILI2130 or Equivalent	
PCAP Interface	I²C	
I²C Address	0x41 (0x82/0x83)	
PCAP FW Version	0x07.0x00.0x00.0x00.0xA1.0x25.0x50.0x00	
PCAP Resolution	16384*16384	
Surface	Glare	

*Color tone slight changed by temperature and driving voltage.

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-30	—	+80	℃
Storage Temperature	TST	-30	—	+80	℃

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. ≦60℃, 90% RH MAX. Temp.＞60℃, Absolute humidity shall be less than 90% RH at 60℃

4. Electrical Characteristics

4.1. Typical Operation Conditions

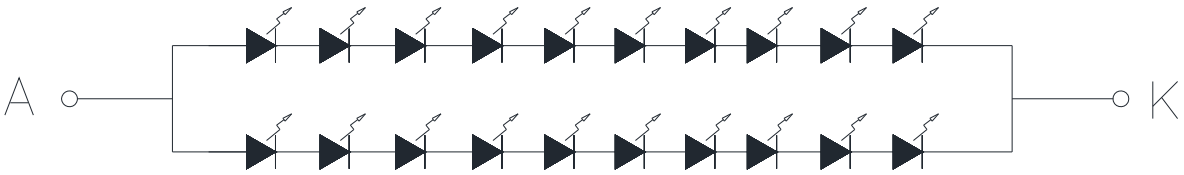
Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	VDD	3.1	3.3	3.6	V	
Current for Driver(Black)	IDD	-	65	98	mA	VDD=3.3V
Input logic high voltage	VIH	0.7 VDD	-	VDD	V	Note 1
Input logic low voltage	VIL	0	-	0.3 VDD		
Supply CTP	VDDT	3.1	3.3	3.6	V	
	ICTP	—	51	77	mA	

Note1: CLK, DE,R0~R7, G0~7, B0~7.

4.2. Backlight Driving Conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Voltage for LED backlight	VL	27	30	34	V	Note 1
Current for LED backlight	IL	--	40	--	mA	
LED life time	-	--	50,000	-	Hr	Note 2

Note 1: The LED Supply Voltage is defined by the number of LED at Ta=25℃ and IL =20ma/pcs.
Note 2: The "LED life time" is defined as the module brightness decrease to 50% Original brightness at Ta=25℃ and IL =20mA/pcs. The LED lifetime could be decreased if operating IL is lager than 25mA/pcs.

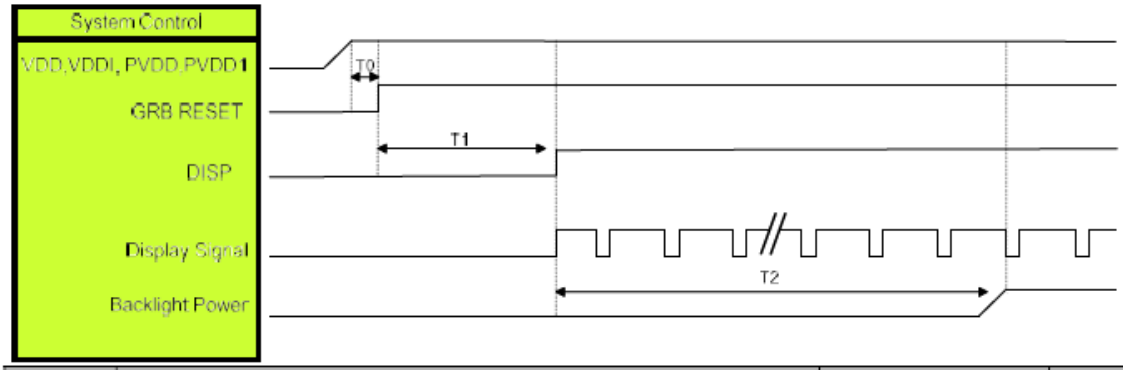


CIRCUIT DIAGRAM

4.3. Power On/Off Sequence

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as the diagram below.

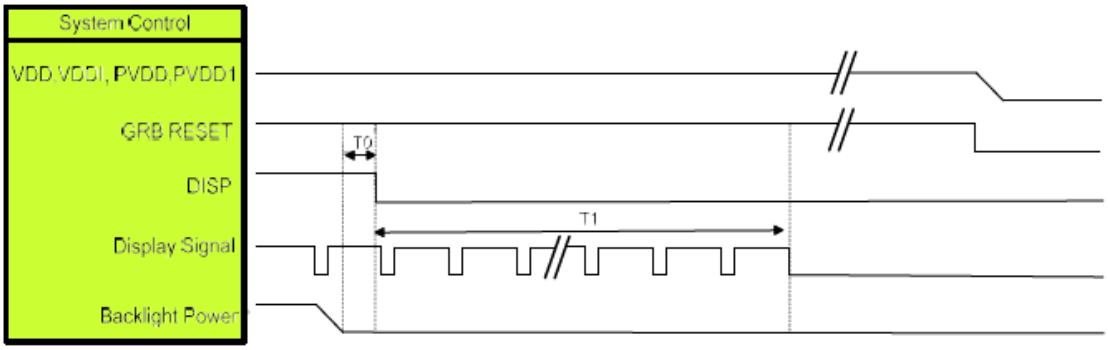
4.3.1. Power On Sequence



Symbol	Description	Min. Time	Unit
T0	System power stability to GRB RESET signal	0	ms
T1	GRB RESET= "High" to DISP="High"	10	ms
T2	Display Signal output to Backlight Power on	250	ms

Note:
1. When DISP pull "H" or "L", IC will execute the internal power on or power off procedures. Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.
2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; R[7:0]; G[7:0]; B[7:0]

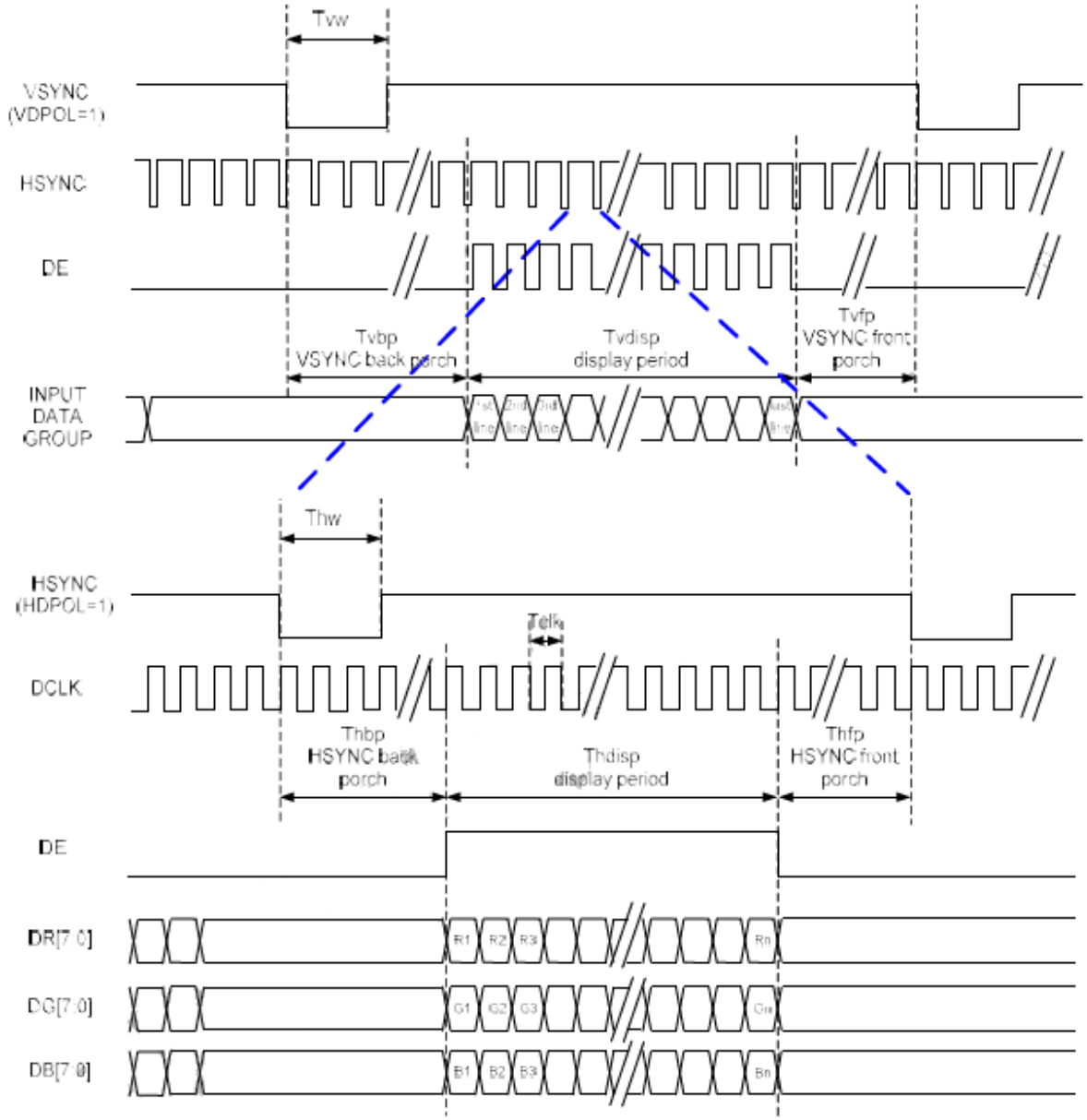
4.3.2 Power Off Sequence



Symbol	Description	Min. Time	Unit
T0	Backlight Power off to DISP="Low"	5	ms
T1	DISP="Low" to IC internal voltage discharge complete	100	ms

Note:
1. When DISP pull "H" or "L", IC will execute the internal power on or power off procedures. Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.
2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; R[7:0]; G[7:0]; B[7:0]

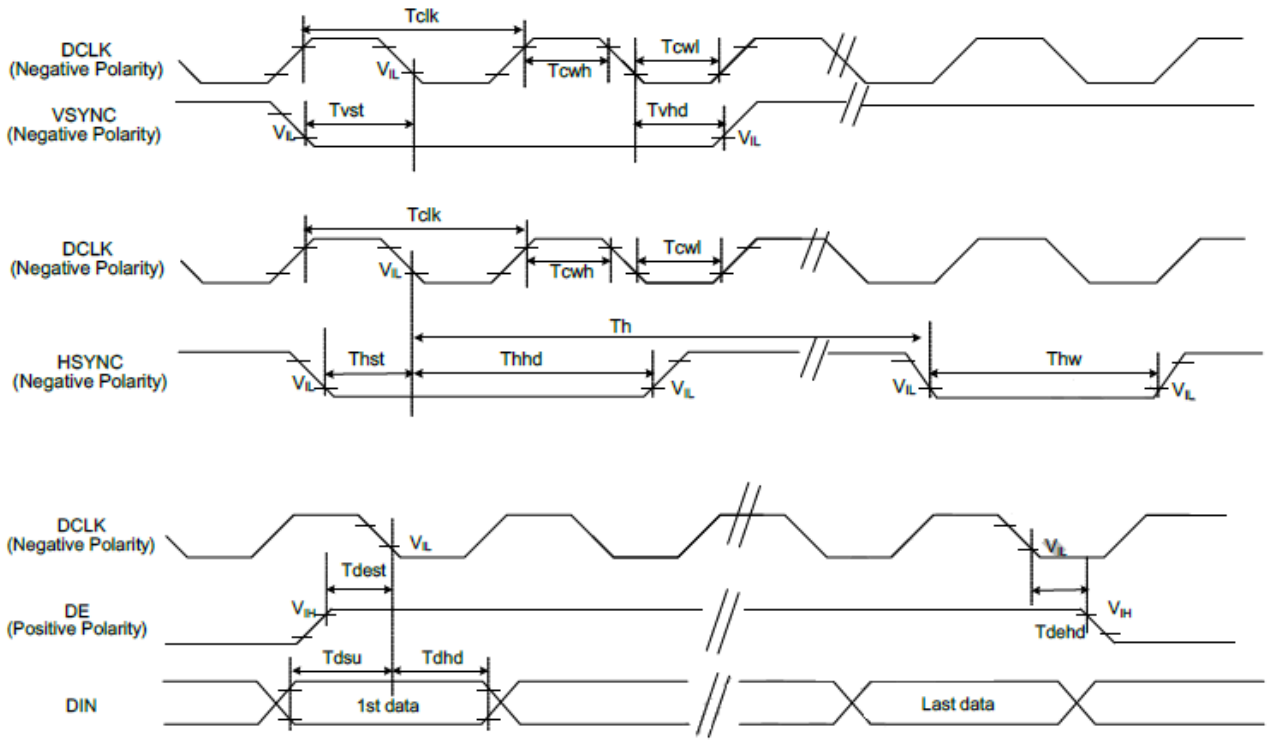
4.4. System Bus Timing for SYNC-DE-Mode



Parallel 24-bit RGB Interface Timing Table							
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	23	25	27	MHz	
HSYNC	Period Time	Th	808	816	896	DCLK	
	Display Period	Thdisp		800		DCLK	
	Back Porch	Thbp	4	8	48	DCLK	
	Front Porch	Thfp	4	8	48	DCLK	
	Pulse Width	Thw	2	4	8	DCLK	
VSYNC	Period Time	Tv	492	496	504	HSYNC	
	Display Period	Tvdisp		480		HSYNC	
	Back Porch	Tvbp	6	8	12	HSYNC	
	Front Porch	Tvfp	6	8	12	HSYNC	
	Pulse Width	Tvw	2	4	8	HSYNC	

Note: 1. The minimum blanking time depends on the GIP timing of the panel specification
2. To ensure the compatibility of different panels, it is recommended to use the typical setting.
3. It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

4.5. System Bus Timing for RGB Interface



Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK Pulse Duty	Tclk	40	50	60	%	
VSYNC Setup Time	Tvst	10	-	-	ns	
VSYNC Hold Time	Tvhd	10	-	-	ns	
HSYNC Setup Time	Thst	10	-	-	ns	
HSYNC Hold Time	Thhd	10	-	-	ns	
Data Setup Time	Tdsu	10	-	-	ns	
Data Hold Time	Tdhd	10	-	-	ns	
DE Setup Time	Tdest	10	-	-	ns	
DE Hold Time	Tdehd	10	-	-	ns	

5.Optical Characteristics

Item		Symbol	Condition.	Min	Typ.	Max.	Unit	Remark
Response time		Tr	θ=0°、Φ=0°	-	10	20	.ms	Note 3
		Tf		-	15	30	.ms	
Contrast ratio		CR	At optimized viewing angle	800	1000	-	-	Note 4
Color Chromaticity	White	Wx	θ=0°、Φ=0	0.27	0.32	0.37		Note 2,6,7
		Wy		0.295	0.345	0.395		
Viewing angle (Gray Scale Inversion Direction)	Hor.	ΘR	CR≧10	70	80	-	Deg.	Note 1
		ΘL		70	80	-		
	Ver.	ΦT		70	80	-		
		ΦB		70	80	-		
Brightness		-	-	650	750	-	cd/m^2	Center of display
Uniformity		(U)	-	75	-	-	%	Note5

Ta=25±2℃

Note 1: Definition of viewing angle range

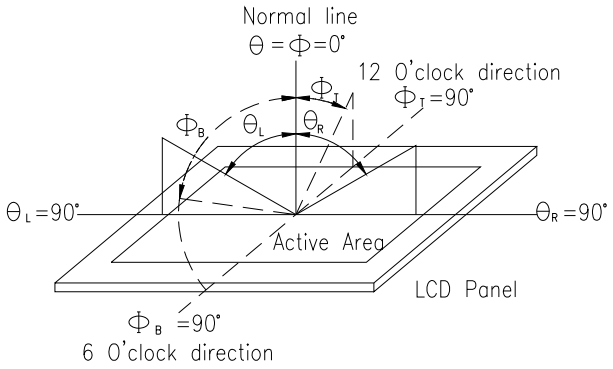


Fig. 6.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7or BM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

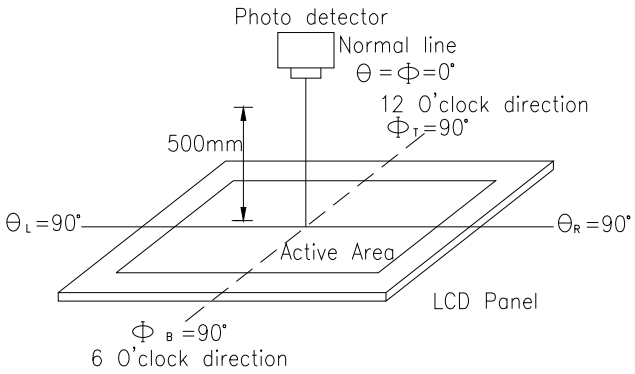
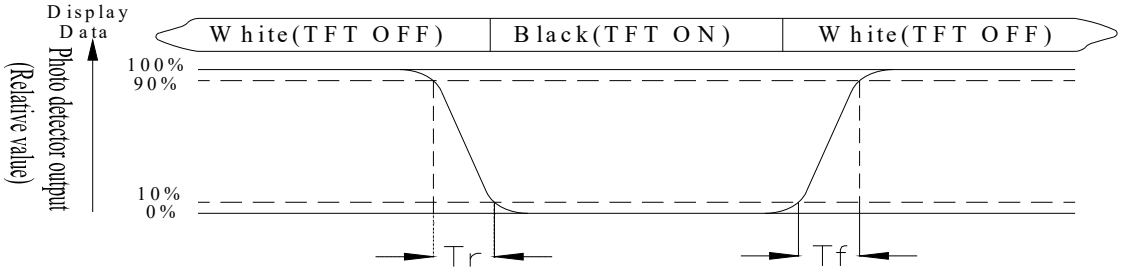


Fig. 6.2. Optical measurement system setup

Note 3: Definition of Response time:
The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time, Tr, is the time between photo detector output intensity changed from 90%to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10%to 90%



Note 4: Definition of contrast ratio:
The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.
Luminance Uniformity (U) = Lmin/Lmax x100%
L = Active area length
W = Active area width

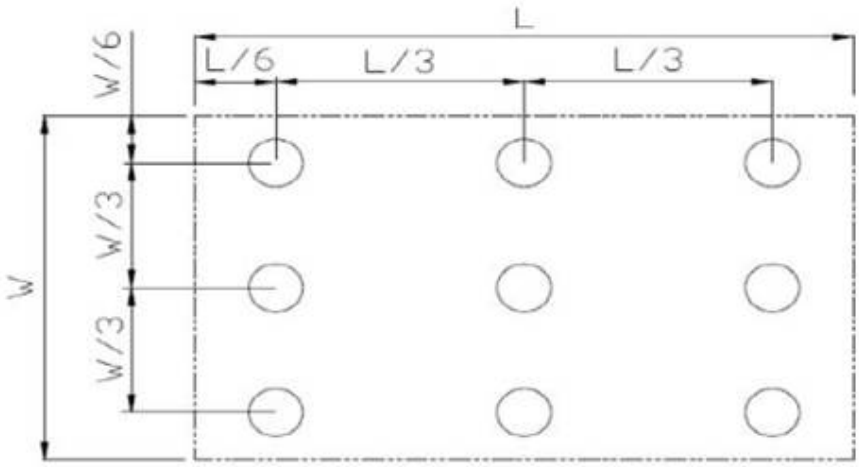


Fig6.3. . Definition of uniformity

Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

6. Interface

6.1. Display Pin Definition

FPC Connector is used for the module electronics interface. The recommended model is FH19SC-40S-0.5SH manufactured by HIROSE or EA WF050-40S/-40ST.

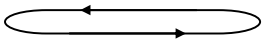
Pin	Symbol	Function	Remark
1	VLED-	Power for LED backlight (Cathode)	
2	VLED+	Power for LED backlight (Anode)	
3	GND	Power Ground	
4	VDD	Power voltage	
5	R0	Red data (LSB)	
6	R1	Red data	
7	R2	Red data	
8	R3	Red data	
9	R4	Red data	
10	R5	Red data	
11	R6	Red data	
12	R7	Red data(MSB)	
13	G0	Green data(LSB)	
14	G1	Green data	
15	G2	Green data	
16	G3	Green data	
17	G4	Green data	
18	G5	Green data	
19	G6	Green data	
20	G7	Green data(MSB)	
21	B0	Blue data(LSB)	
22	B1	Blue data	
23	B2	Blue data	
24	B3	Blue data	
25	B4	Blue data	
26	B5	Blue data	
27	B6	Blue data	
28	B7	Blue data(MSB)	
29	GND	Power Ground	
30	CLK	Sample clock	
31	DISP	Display on/off	
32	NC	No connection	
33	NC	No connection	
34	DE	Data input enable	
35	NC	No connection	
36	GND	Power Ground	
37	NC	No connection	
38	NC	No connection	
39	NC	No connection	
40	NC	No connection	

6.2. PCAP Pin Definition

Pin	Symbol	Function	Remark
1	VSS	Ground for analog circuit	
2	VDDT	Power Supply +3.3V	
3	SCL	I²C clock input	
4	NC	No connect	
5	SDA	I²C data input and output	
6	NC	No connect	
7	/RST	External Reset, Low active	
8	NC	No connect	
9	/INT	External interrupt to the host	
10	VSS	Ground for analog circuit	

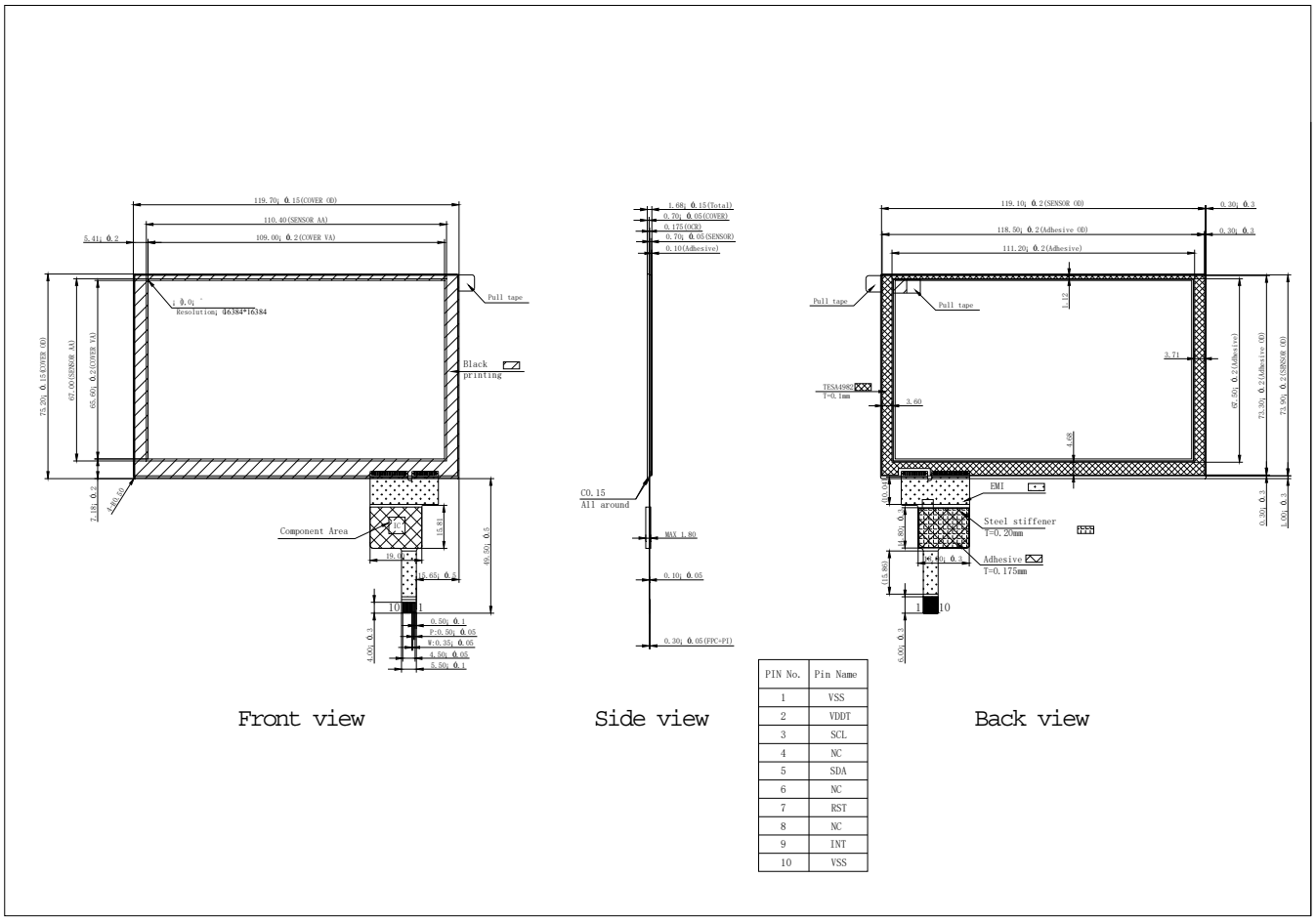
7.Reliability

Content of Reliability Test (Wide temperature, -30℃~80℃)

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	80℃ 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-30℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -30℃ 25℃ 80℃  30min 5min 30min 1 cycle	-30℃/80℃ 10 cycles	——
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±600V(contact), ±800v(air), RS=330Ω CS=150pF 10 times	——

Note1: No dew condensation to be observed.
Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.
Note3: The packing have to including into the vibration testing.

8.Touch Panel Information



PIN No.	Pin Name
1	VSS
2	VDDT
3	SCL
4	NC
5	SDA
6	NC
7	RST
8	NC
9	INT
10	VSS

8.1 PCAP controller ILI2130

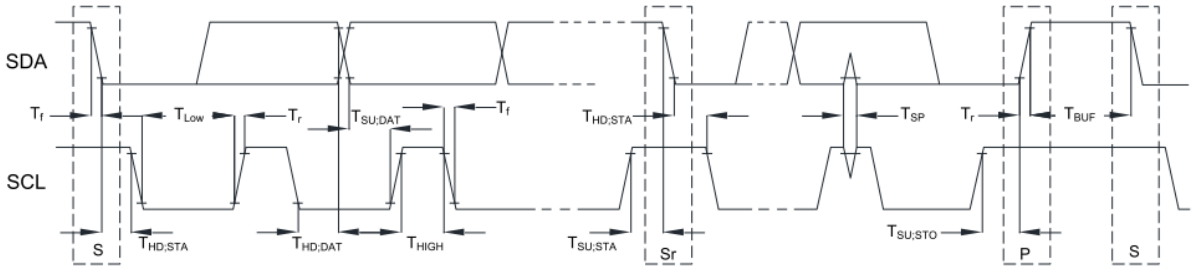
8.1.1 Device address

The device addresses are 7-binary bits long and are conventionally expressed as 4 bits followed by 3 bits followed by the letter ‘b’, 1000 001b. These addresses occupy the high seven bits of an eight-bit field on the bus.

MSB							LSB
1	0	0	0	0	0	1	0/1
7-bit Device Address							R/W

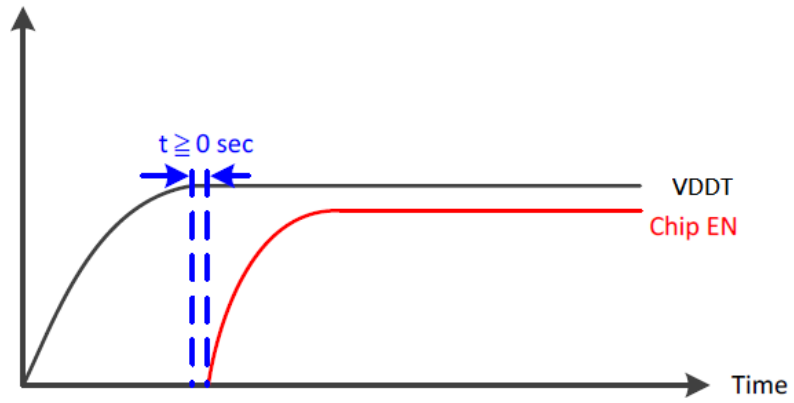
7-bit Device Address: 0x41
8-bit Device Address Read: 0x83/ Write :0x82

8.1.2 I²C AC Characteristics

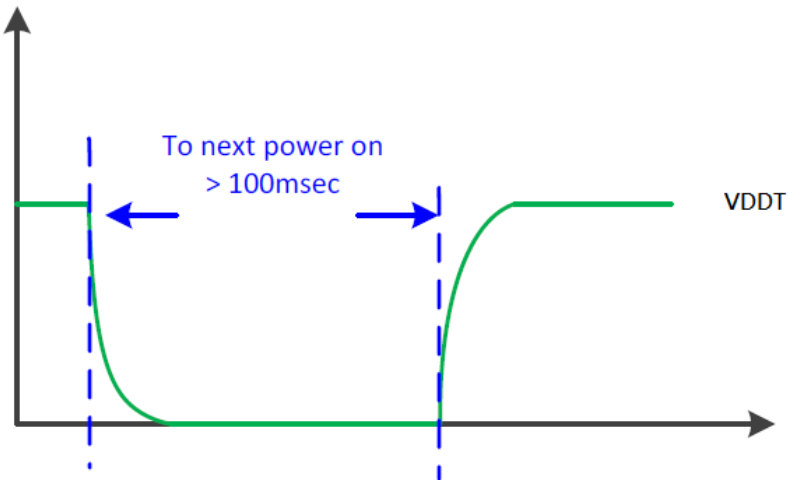


Item	Symbol	100kHz		400kHz		Unit
		Min.	Max.	Min.	Max.	
SCL standard mode clock frequency	FSCL	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock is generated.	THD;STA	4	--	0.6	--	us
LOW period of the SCL clock	TLOW	4.7	--	1.3	--	us
HIGH period of the SCL clock	THIGH	4	--	0.6	--	us
Setup time for a repeat START condition.	TSU;STA	4.7	--	0.6	--	us
Data hold time	THD;DAT	0	3.45	0	0.9	us
Data setup time	TSU;DAT	250	--	100	--	ns
Rising time of both SDA and SCL signals	Tr	--	1000	--	300	ns
Falling time of both SDA and SCL signals	Tf	--	300	--	300	ns
Setup time for STOP condition.	TSU;STO	4	--	0.6	--	us
Free time between STOP and START condition	TBUF	4.7	--	1.3	--	us
Pulse width of spikes which must be suppressed by input filter	TSP	--	--	0	50	ns

8.2. Power On Sequence



8.3. Power Off to Power On Sequence



8.4 Code example for PCAP

```
#include "main.h"
//================= By IC ===========
unsigned char ILI2130_buf[11];
/***************************************
 * if touch point add 3~10 finger
 * u can add buf size for add finegr
 * 1 finger point add bufsize[5]
 * finger 1 buf[2~5]
 * finger 2 buf[7-10]
 * finger 3 buf[12~15]
 * finger 4 buf[17~20]
 * finger 5 buf[22~25]
 * finger 6 buf[27~30]
 * finger 7 buf[32~35]
 * finger 8 buf[37~40]
 * finger 9 buf[42~45]
 * finger 10 buf[47~50]
 * 10 finger total 51 buf
***************************************/

void CTP_initial_ILI2130(void)
{
    TRISCbits.TRISC4 = 0;    //CTP_SCL
    TRISGbits.TRISG7 = 0;    //CTP_SDA
    TRISAbits.TRISA2 = 1;    //CTP_INT
    CNPU3bits.CN35PUE = 1;  //INT_Internal Pull High
}

void I2C_SrCondition(void)
{
   CTP_SCL = 0;
    delay(T4);
   CTP_SDA = 1;
   delay(T4);

    CTP_SCL = 1;
    delay(T4);
    CTP_SDA = 0;
    delay(T4);
}

void I2C_CLK_ILI2130(void)// I2C SCL Timing
{
     CTP_SCL = 1;  //SCL High
     delay(T4);    //delay(4)

     CTP_SCL = 0;  //SCL Low
     delay(T4);    //delay(4)
}
//================================================
unsigned char ILI2130_DataRead(void)
{
    unsigned char Data;

    Data = LCD_GetData_I2C();

    return Data ;
}
```

```
//=============================================
void ILI2130_received_data(void)
{
    unsigned int i;

   //TOUCH DATA
    for(i=0;i<11;i++)
    {
         ILI2130_buf[i]=ILI2130_DataRead();
         CTP_SDA = 0;
         delay(T4);
         I2C_CLK_ILI2130();
    }
    I2C_StopCondition();
}

//================================================
unsigned int ILI2130_Get_X1_Value_16bit(void)
{
  unsigned int temp,temp1;

  temp=0;
  if(ILI2130_buf[1]==0x40)
  {
      temp|=ILI2130_buf[3];
      temp1=(temp<<8);
      temp= temp1|ILI2130_buf[2];
  }
  return temp;
}

unsigned int ILI2130_Get_Y1_Value_16bit(void)
{
  unsigned int temp2,temp3;

  temp2=0;
  if(ILI2130_buf[1]==0x40)
  {
      temp2|=ILI2130_buf[5];
      temp3=(temp2<<8);
      temp2= temp3|ILI2130_buf[4];
  }
  return temp2;
}

unsigned int ILI2130_Get_X2_Value_16bit(void)
{
  unsigned int temp,temp1;
  temp=0;
  if(ILI2130_buf[6]==0x41)
  {
      temp|=ILI2130_buf[8];
      temp1=(temp<<8);
      temp= temp1|ILI2130_buf[7];
  }
  return temp;
}

unsigned int ILI2130_Get_Y2_Value_16bit(void)
{
  unsigned int temp2,temp3;

  temp2=0;
  if(ILI2130_buf[6]==0x41)
  {
```

```
        temp2|=ILI2130_buf[10];
        temp3=(temp2<<8);
        temp2= temp3|ILI2130_buf[9];
    }

    return temp2;
}

void ILI2130_Communication(void)
{
    I2C_StartCondition();              //s
    LCD_SendAddress(0x82);              //A            write to slave 8
    Slave_ack();//1

    LCD_SendAddress(0x10); //8
    Slave_ack();//1
    //I2C_StopCondition();

    I2C_SrCondition();
    LCD_SendAddress(0x83);              //   read slave data
    Slave_ack();
}
//=======================================================
```

8.5 Programming guide for PCAP

More information on getting touch data and programming is written here:
https://www.lcd-module.de/eng/pdf/zubehoer/ILI2130_Programming_Guide_V1_50.pdf

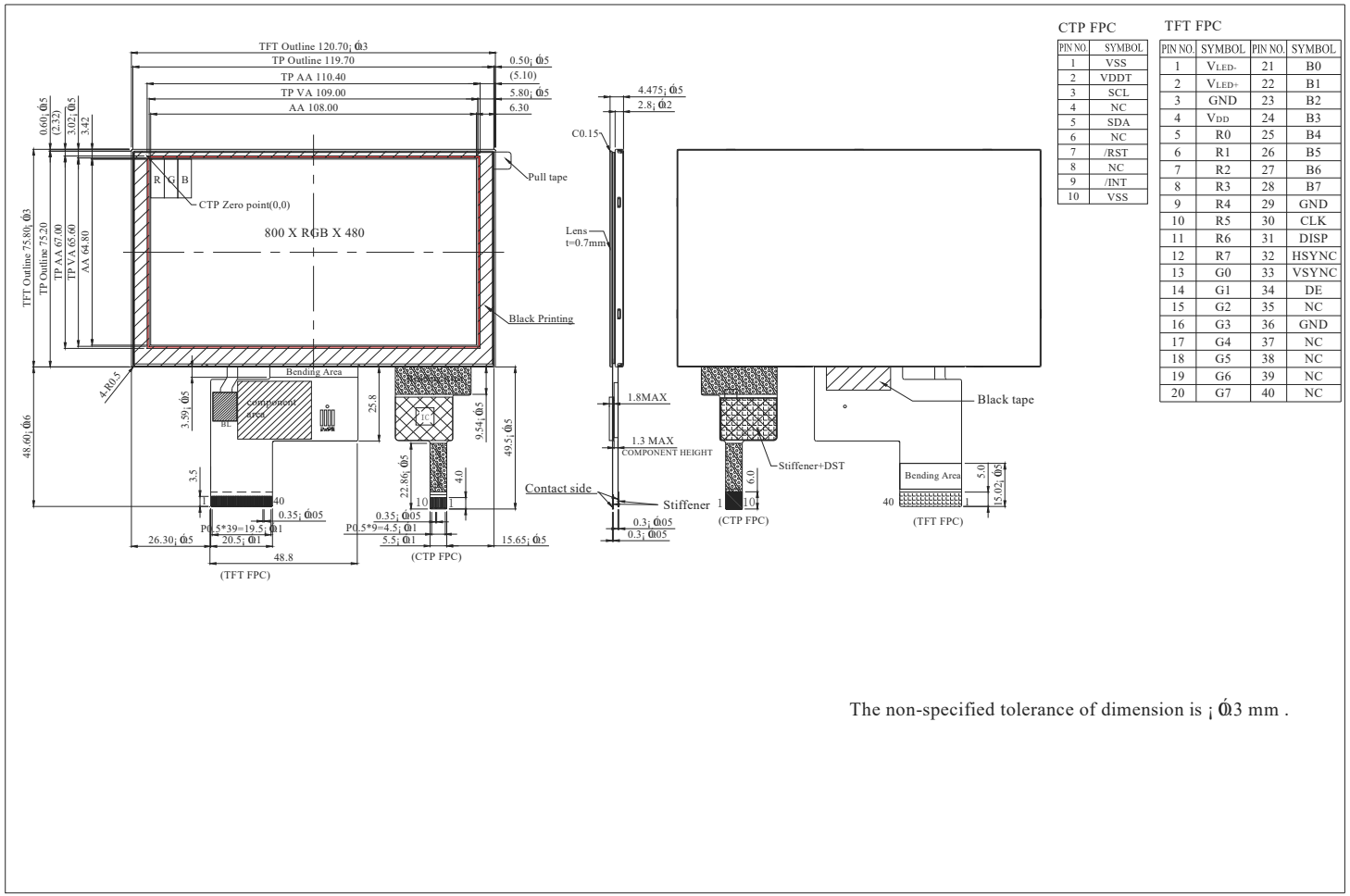
8.6 Comparsion between ILI2130 and FT5426 (EA TFT050-84ATS)

https://www.lcd-module.de/eng/pdf/zubehoer/ILI2130_comparsion_FT5426.pdf

9. History

Date	Page	Item	Old	New
2022/02/25		First version		
2023/02/14	5	Operating Temperature	$T_{op.}$ -20..+70°C	$T_{op.}$ -30..+80°C
2023/02/14	6	Current for Driver	110mA (typ.)	65mA (typ)
2023/02/14	7	Power On/Off Sequence		
2023/02/14	9	System Bus Timing SYN-DE		
2023/02/14	12	Contrast ratio	500 (typ.)	1000 (typ.)
2023/02/14	12	Viewing angle	50/70 (typ.)	80 (typ.)
2023/02/14	17	Reliability	-20°C~70°C	-30°C~80°C

10. Contour Drawing



CTP FPC

PIN NO.	SYMBOL
1	VSS
2	VDDT
3	SCL
4	NC
5	SDA
6	NC
7	/RST
8	NC
9	/INT
10	VSS

TFT FPC

PIN NO.	SYMBOL	PIN NO.	SYMBOL
1	V_{LED-}	21	B0
2	V_{LED+}	22	B1
3	GND	23	B2
4	V_{DD}	24	B3
5	R0	25	B4
6	R1	26	B5
7	R2	27	B6
8	R3	28	B7
9	R4	29	GND
10	R5	30	CLK
11	R6	31	DISP
12	R7	32	HSYNC
13	G0	33	VSYNC
14	G1	34	DE
15	G2	35	NC
16	G3	36	GND
17	G4	37	NC
18	G5	38	NC
19	G6	39	NC
20	G7	40	NC

The non-specified tolerance of dimension is ¡ Ó3 mm .