PIC12(L)F1840 Family
Silicon Errata and Data Sheet Clarification

The PIC12(L)F1840 family devices that you have received conform functionally to the current Device Data Sheet (DS41441**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC12(L)F1840 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A5**).

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC12(L)F1840 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A4	A5
PIC12F1840	01 1011 100	0 0100	0 0101
PIC12LF1840	01 1011 110	0 0100	0 0101

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC16F/LF1847/PIC12F/LF1840 Memory Programming Specification"* (DS41439) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A4	A5
Oscillator	HFINTOSC Ready/Stable bit	1.1	Bits remained set to '1' after initial trigger	X	
Oscillator	Clock Switching	1.2	Clock switching fails	X	
Oscillator	Oscillator Start-up Timer (OST) bit	1.3	OST bit remains set	X	
Resets	Low-Power Sleep	2.1	$\overline{\text{MCLR}}$ Reset during low-power Sleep will be reported as a POR Reset (PIC12F1840 device only).	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A5**).

1. Module: Oscillator

1.1 OSCSTAT bits: HFIOFR and HFIOFS

When HFINTOSC is selected, the HFIOFR and HFIOFS bits will become set when the oscillator becomes ready and stable. Once these bits are set they become “stuck”, indicating that HFINTOSC is always ready and stable. If the HFINTOSC is disabled, the bits fail to be cleared.

Work around

None.

Affected Silicon Revisions

A4	A5						
X							

1.2 Clock Switching

When switching clock sources between INTOSC clock source and an external clock source operating at a different power mode, one corrupted instruction may be executed after the switch occurs.

This issue does not affect Two-Speed Start-up or the Fail-Safe Clock Monitor operation.

Work around

When clock switching from an external oscillator clock source, first switch to 16 MHz HFINTOSC. Once running at 16 MHz HFINTOSC, configure IRCF to run at desired frequency.

When clock switching from an INTOSC to an external oscillator clock source, first switch from desired INTOSC frequency to HFINTOSC High-Power mode (8 MHz or 16 MHz). Once running from HFINTOSC, switch to the external oscillator clock source.

Affected Silicon Revisions

A4	A5						
X							

1.3 Oscillator Start-up Timer (OST) bit

During the Two-Speed Start-up sequence, the OST is enabled to count 1024 clock cycles. After the count is reached, the OSTS bit is set, the system clock is held low until the next falling edge of the external crystal (LP, XT or HS mode), before switching to the external clock source.

When an external oscillator is configured as the primary clock and Fail-Safe Clock mode is enabled (FCMEN = 1), any of the following conditions will result in the Oscillator Start-up Timer (OST) failing to restart:

- $\overline{\text{MCLR}}$ Reset
- Wake from Sleep
- Clock change from INTOSC to Primary Clock

This anomaly will manifest itself as a clock failure condition for external oscillators which take longer than the clock failure time-out period to start.

Work around

None.

Affected Silicon Revisions

A4	A5						
X							

2. Module: Resets

2.1 Low-Power Sleep (PIC12F1840 device only)

When the device is in low-power Sleep (VREGPM = 1 and SLEEP instruction is executed), a $\overline{\text{MCLR}}$ Reset will be reported as a POR Reset:

- $\overline{\text{PD}}$ = 1
- $\overline{\text{POR}}$ = 0
- $\overline{\text{RDMCLR}}$ = 1

Work around

Use Normal-Power Sleep mode (VREGPM = 0).

Affected Silicon Revisions

A4	A5						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41441**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Specifications

The maximum VSS and VDD currents have been updated.

30.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on VDD with respect to VSS, PIC12F1840 ..... -0.3V to +6.5V
Voltage on VDD with respect to VSS, PIC12LF1840 ..... -0.3V to +4.0V
Voltage on $\overline{\text{MCLR}}$ with respect to Vss ..... -0.3V to +9.0V
Voltage on all other pins with respect to VSS ..... -0.3V to (VDD + 0.3V)
Total power dissipation(1) ..... 800 mW
Maximum current out of VSS pin, -40°C ≤ TA ≤ +85°C for industrial ..... **170** mA
Maximum current out of VSS pin, -40°C ≤ TA ≤ +125°C for extended ..... **70** mA
Maximum current into VDD pin, -40°C ≤ TA ≤ +85°C for industrial ..... **170** mA
Maximum current into VDD pin, -40°C ≤ TA ≤ +125°C for extended ..... **70** mA
Clamp current, IK (VPIN < 0 or VPIN > VDD) ..... ± 20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (02/2012)

Initial release of this document.

Rev B Document (02/2013)

Added MPLAB X IDE; Added Silicon Revision A5; Added Module 2, Resets.

Data Sheet Clarifications: Removed Module 1 (Oscillator); Added new Module 1, Electrical Specifications.

NOTES:

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